# Develop SPICE High Frequency Small Signal Transistor Models from Data Sheets

Here is a method for creating SPICE models for transistors that are not included in a device library

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This paper presents a simple procedure for SPICE high frequency small signal variational modeling of a transistor from the information contained in its data sheets. This is useful when the transistor is not listed in the Spice model library and only the variation-



**Figure 1.** [y] parameter variational model of a quadripole.

al analysis is required. Instead of trying to find the best substitute from the library, we show how one can build its own model. The derived model gives better simulation results than any one that can be obtained by using an "equivalent" transistor model from the library.

The proposed model can be used for modeling not only transistors but any quadripole whose *y* parameter values are known as function of frequency.

#### The four current controlled model

Let us start by considering the well known variational *y* parameter model of a quadripole illustrated in Figure 1.

This model uses two voltage controlled-current sources and two admittances. At high frequencies, the value of each *y* parameter is a frequency dependent complex number. As we will show, the two controlled sources can be modeled directly with a PSpice model. This is not the case for the two admittances  $y_{11}$  and  $y_{22}$ . Certainly, one can consider that the values of the R, L or C element constituting those two admittances are frequency independent and we can model them with fixed values elements. This could work well for a narrow band circuit but surely not for a broad band circuit. In order to take into account the frequency dependent nature of the two admittances  $y_{11}$  and  $y_{22}$ , we suggest to replace each one of them by a voltage controlled current source as shown in Figure 2.

It is easy to verify that the terminal's V-I relations of the four controlled-current sources



Figure 2. A four controlled current sources variational model of a quadripole.

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Figure 3. SPICE A/D symbolic representation of a frequency dependent voltage controlled current source.

model is the same ones as those of the y parameters model shown in Figure 1:

 $\begin{array}{l} I_1 = y_{11} \, V_1 + y_{12} \, V_2 \\ I_2 = y_{21} \, V_1 + y_{22} \, V_2 \end{array}$ 

With this four controlled-current sources model, we can now use the full potential of SPICE.

#### **SPICE** modeling

The Analog Behavioral Modeling (ABM) feature provided in the circuit analysis program SPICE A/D allows one to easily transpose the four controlled-current source model of Figure 2 into a SPICE model. Indeed, each source can be represented by a frequency dependent voltage controlled current source (GFREQ), shown in Figure 3.

The GFREQ attributes are defined as follows [1]:

- EXP Value used for table lookup defaults to V(%IN+,%IN-) if left blank.
- TABLE Series of either (input frequency, magnitude, phase) triplets, or (input frequency, real part, imaginary part) triplets describing a complex value — defaults to (0, 0, 0) (1 MEG, -10, 90) if left blank.

highest order. Interpolation is performed between entries. For frequencies outside the table's range, 0 (zero) magnitude is used.

DELAY Group delay increment — defaults to 0 if left blank.

R\_I

- I Table type If left blank, the frequency table is interpreted in the (input frequency, magnitude, phase) format. If defined with any value (such as YES), the table is interpreted in the (input frequency, real part, imaginary part) format.
- MAGUNITS Units for magnitude where the value can be DB (decibels) or MAG (raw magnitude) — defaults to DB if left blank.
- PHASEUNITS Units for phase where the value can be DEG (degree) or RAD (radians) defaults to DEG if left blank.

The output current for each frequency is then equal to the control voltage applied between inputs IN+ and IN- (if EXP attribute is left blank) times the complex value of the table at that frequency.

The transition from the four controlled-current sources model of a quadripole illustrated in Figure 2 to a SPICE model of the same quadripole is straightforward. One only needs to use four GFREQ controlled sources (like the one previously discussed) and connect them as illustrated in Figure 4.

Each one of the controlled current sources takes into account one of the y parameters. The model shown in Figure 4 is general. When used for modeling a three terminals device like a transistor, we simply connect together the common terminal of the input and output ports.

#### **Application example**

To illustrate how easy it is to use the proposed model and show its validity, let us consider the single transis-



The table's frequency must be in lowest to

Figure 4. SPICE model of a quadripole having known [y] parameters.

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Figure 5. Variational circuit of an untuned wide band amplifier.

tor untuned wideband amplifier whose variational schematic appears in Figure 5.

Suppose that we are interested to find the value of the voltage gain of this amplifier over the frequency range of 100 MHz to 300 MHz. A straightforward theoretical analysis of the variational circuit shown in Figure 5 yields the following general exact expression for the voltage gain:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-y_{fe}}{\left(y_{oe} + \frac{1}{R_2}\right)\left(1 + R_1 y_{ie}\right) - y_{fe} y_{re} R_1}$$

Let us assume that the transistor is DC biased as follows:  $I_{DC} = 1.5$  mA.;  $V_{CE} = 6$  V. From the manufacturer's data sheets, We can extract the values shown in Table 1 for each of the *y* parameters at some points within the band of interest, including the two boundary points. For each of the five selected frequency points, this yields the theoretical exact voltage gains, as summarized in Table 2.

Now, let us simulate the same circuit whose model appears in Figure 6 with the PSpice program. The corresponding Netlist is shown in Table 3. The simulation result appears in Figure 7.

Comparing the results obtained by simulation with the theoretical ones, it appears that the proposed transistor SPICE model is a valid one.

If, in order to simplify the modeling, we decide to model the two admittances  $y_{11}$  and  $y_{22}$  with passive constant value elements, say those prevailing at midband (in this case, 200 MHz), the simplified SPICE model of the circuit will be the one shown in Figure 8. A PSpice simulation of this model yields the voltage gain illustrated in Figure 9.

Comparing the results obtained with the simplified model of Figure 9 with the results obtained with the exact model of Figure 6, we can conclude that the simplified model is valid only over a narrow frequency band around the frequency at which it was constructed (200 MHz, in our example). On the other hand, the range of validity of the exact model depends solely on the number and the distribution of frequency points considered (within the bandwidth used for the simulation) for characterizing each voltage controlled current source of the transistor model.

#### Conclusion

The procedure presented in this paper for variational modeling of a frequency dependent quadripole, such as a transistor, can be extended to any four port device whose y parameters are known. Obviously, if the four port



Figure 6. SPICE model of the circuit illustrated in Figure 5.

f	$y_{ie}$	$y_{oe}$	$y_{fe}$	$y_{re}$	
$100 \mathrm{~MHz}$	(0.5 + j 4)	(0.1 +j 1.2)	(41 – j 7)	$(-0.1 - j \ 0.4)$	mmho
$150 \mathrm{~MHz}$	(1.5 + j 6)	(0.1 +j 1.5)	(41 – j 15)	$(-0.1 - j \ 0.5)$	mmho
$200 \mathrm{~MHz}$	(2.5 + j 7.5)	$(0.2 + j \ 1.8)$	$(40 - j \ 20)$	$(-0.1 - j \ 0.7)$	mmho
$250 \mathrm{~MHz}$	(3.6 + j 8.5)	$(0.4 + j \ 2.2)$	$(40 - j \ 23)$	$(-0.1 - j \ 0.8)$	mmho
$300 \mathrm{~MHz}$	(5 + j 10)	$(0.5 + j \ 2.6)$	$(36 - j \ 26)$	$(-0.1 - j \ 1.1)$	mmho

Table 1. y parameters extracted from manufacturer's data sheets.

f	
$100 \mathrm{~MHz}$	-0.13 + j3.52
$150 \mathrm{~MHz}$	0.4 + j2.74
$200 \mathrm{~MHz}$	0.48 + j1.97
$250 \mathrm{~MHz}$	0.51 + j1.59
$300 \mathrm{~MHz}$	0.47 + j 1.14

▲ Table 2. Resulting voltage gains.

## TRANSISTOR MODELING

\* Schematics Netlist \*

Reference

8.0. June 1997.

```
V V1
                                                                                                             $N 0001 0 DC 0V AC 1V
R R2
                                                                                                             0 $N 0002 1k
R R1
                                                                                                             $N 0001 $N 0003 500
G G1
                                                                                                                 N 0003 0 FREQ \{ V(N 0003, 0) \} = R I (
 + (100 MegHz, 5E-04, 4E-3) (150 MegHz, 1.5E-3, 6E-3) (200 MegHz, 2.5E-3, 7.5E-3) (250 MegHz, 3.6E-3, 8.5E-3) (300 MegHz, 5E-3, 10E-3) (250 MegHz, 3.6E-3, 8.5E-3) (250 MegHz, 3.6E-3, 8.5E-3) (250 MegHz, 5E-3, 10E-3) (250 MegHz, 3.6E-3, 8.5E-3) (250 MegHz, 5E-3, 10E-3) (250 MegHz, 3.6E-3, 8.5E-3) (250 MegHz, 3.6E-3) (250 MegHz,
 + )
G G2
                                                                                                                   N 0003 0 FREQ \{ V(N 0002, 0) \} = R I (
 + (100 MegHz, -1E-4, -4E-4) (150 MegHz, -1E-4, -5E-4) (200 MegHz, -1E-4, -7E-4) (250 MegHz, -1E-4, -8E-4) (300 MegHz, -1E-4, -1.1E-3) (250 MegHz, -1E-4, -8E-4) (250 MegHz, -1E-4) (2
 + )
G_G3
                                                                                                                 N 0002 0 FREQ \{ V(N 0003, 0) \} = R I (
 + (100 MegHz, 41E-3, -7E-3)(150 MegHz, 41E-3, -15E-3)(200 MegHz, 40E-3, -20E-3)(250 MegHz, 40E-3, -23E-3)(300 MegHz, 36E-3, -26E-3)(250 MegHz, 40E-3, -26E-3)(250 MegHz, 40E-3)(250 MegH
 + )
G_G4
                                                                                                                   N 0002 0 FREQ \{ V(N 0002, 0) \} = R I (
 + (100 MegHz, 1E-4, 1.2E-03) (150 MegHz, 1E-4, 1.5E-3) (200 MegHz, 2E-4, 1.8E-3) (250 MegHz, 4E-4, 2.2E-3) (300 MegHz, 5E-4, 2.6E-3) (250 MegHz, 4E-4, 2.2E-3) (250 MegHz, 4E-4, 2.2E-4) (250 MegHz, 4E-4, 2.2E-4) (250 MegHz, 4E-4) (250 MegH
 + )
```

▲ Table 3. Netlist for the PSpice simulation of the circuit shown in Figure 6.

device is characterized by another set of parameters, we can convert those into *y* parameters or build an appropriate model by following a procedure similar to the one presented here.

1. MicroSim PSpice A/D reference manual, Version

#### **Author information**

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▲ Figure 8. Simplified SPICE model of the circuit of Figure 5.



Figure 7. Simulation results of the circuit model shown in Figure 6.



Figure 9. Simulation results of the circuit model shown in Figure 8.