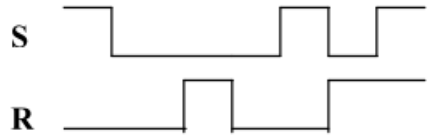
Sheet # 3

Flip Flops

1. The S and R waveforms provided in the following figure are applied to the inputs of the NOR SR latch. Write the mode of operation for each time period and draw the Q output waveform that results.



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2. Repeat prob.1 when NOR gates are replaced with NAND gates.

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3. Construct a gated D latch using NOR and AND gates instead of using NAND gates.

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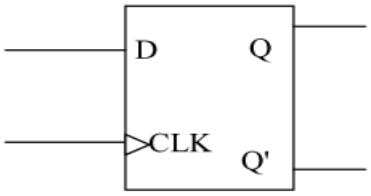
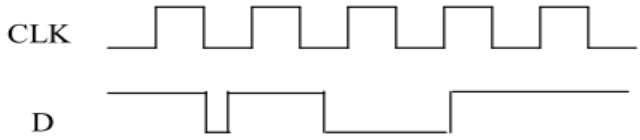
4. The D and CLK waveforms shown are applied to the inputs of the controlled D-FF shown. Draw the Q output waveform that results.





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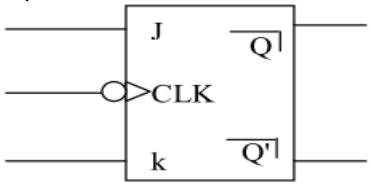
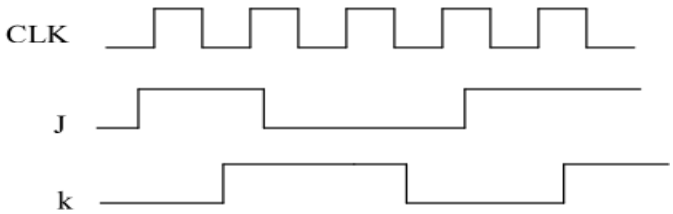
5. For the Master-Slave JK flip-flop shown, draw the output Q and write the mode of operation for each time period.





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6. How to use the JK flip-flop as a D flip-flop and vice versa. Use any additional gates you need.

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7. A set-dominate flip-flop has a set and a reset input. It differs from a conventional RS flip-flop in that an attempt to simultaneously set and reset results in setting the flip-flop.

a) Obtain the characteristic table and characteristic equation for the set-dominate flip-flop.

b) Obtain a logic diagram for an asynchronous set-dominate flip-flop.

Best Wishes of Success