Digital Lec (1)   27/9/2016

150 → 30 (oral
             Experiment)
             Project
     → 30 → 20 (mid-term)
          → 10 (Class - work)
     ↘ 90 Final

* Course Contents :

- Logic families and its characteristics.

- Encoder / Decoder
  Multiplexer / Demultiplexer } Combinational Logic
                                       circuits

- Sequential logic circuit ⇒ flipflop

- counters

- Shift Registers

* Types of logic families : (Based on its Basic elements)

    - TTL (transistor - Transistor Logic)
            - Basic element BJT   (0 → 5v)

    - ECL   (Emitter coupled Logic)
            - Basic element BJT   (negative Power - supply)

    - CMOS (complementary MOS (Metal-oxide-semiconductor))
            - Basic element ⇒ Both PMOS, NMOS

* Integrated circuits (ICs)

- SSI (Small Scale Integration)

  12 gate / chip

- MSI (medium scale Integration)

  12 ~ 99 gate / chip

- LSI (large scale Integration)

  1000 gate / chip

- VLSI (very-large scale Interation)

  100,000 gate / chip

  $\Rightarrow$ More development chips $\Longrightarrow$ faster, cheaper

  $\Rightarrow$ 7400 , NAND , 4 gate / chip

* Subfamily TTL

* Low Power

* Fast TTL

* Advanced TTL As TTL

* Als TTL

(Advanced Low Power schotlky)

SN 74 ALS XXX A

TTL   family type
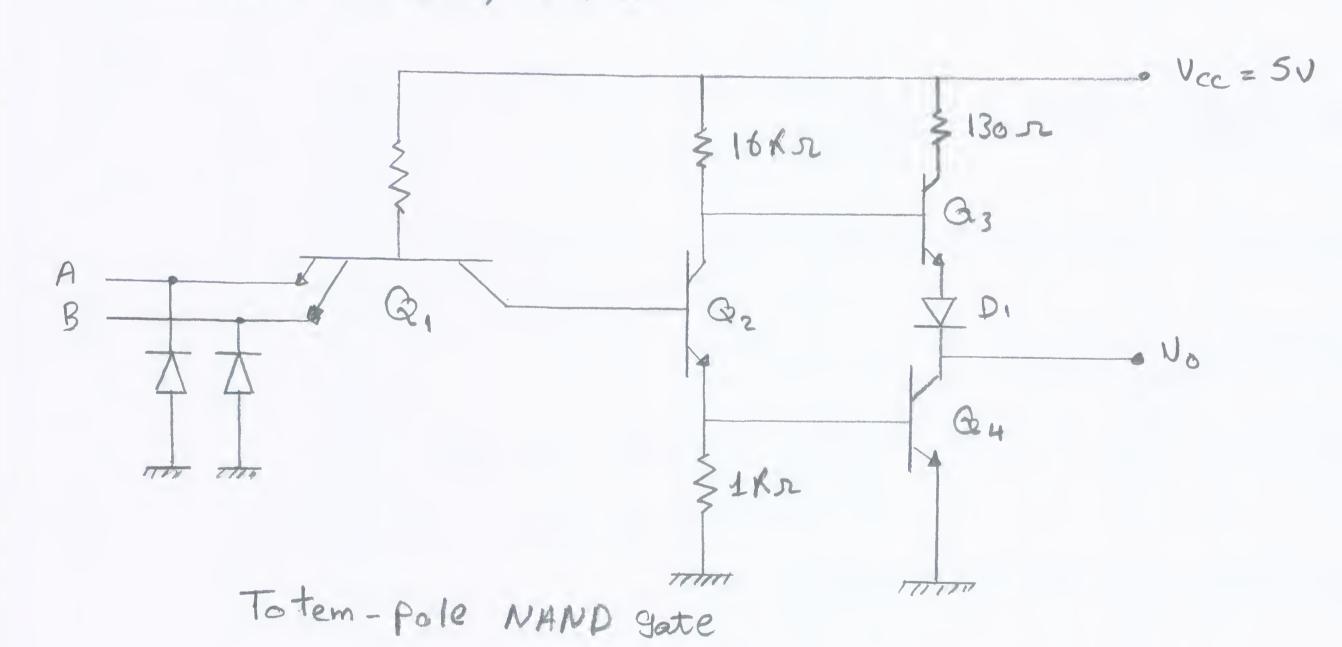
(74) $\longrightarrow$ Ic Max temp.

$0 \longrightarrow 70°$

74f $\longrightarrow$ TTL

74 Cf $\longrightarrow$ CMOS

(54) $\longrightarrow$ TTL used for $\rightarrow$ military applications

(max temp. 55° $\longrightarrow$ 125°)

(SN) $\longrightarrow$ manfcature الشركة المُصَنعة
- SN $\longrightarrow$ Texas instrument
- S $\longrightarrow$ signetics
- DM $\longrightarrow$ national instrument

(A) $\longrightarrow$ أخر رمز
(نوع Package)

ناخذ نفصّله ← بل نأخذ نفضّله

N $\longrightarrow$ Plastic - dual - in - line
W $\longrightarrow$ Ceramic Package

(XXX) $\longrightarrow$ رقم الـ IC
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, ويُعبّر عن نوع الـ gate

* 7400 (NAND Gate)
fundamental (Basic) TTL

Totem - pole NAND gate

$Q_1 \longrightarrow$ Multi-emitter transistor

$Q_3, Q_4 \longrightarrow$ totem pole transistors

$Q_2 \longrightarrow$ control of Q_3 & Q_4

(*)   A = 0   B = 0

$Q_1 \rightarrow$ ON   (Saturation stat) $\longrightarrow V_{CE_1} = 0.2$ V

$Q_2 \rightarrow$ off

                current flow through Q_3 to V_{out}

    $Q_3 \rightarrow$ ON
    $Q_4 \rightarrow$ off   (No Base current)

* $V_0 = V_{cc} - V_R - V_{sat} - V_{D_1} = V_{cc} - I * (130\Omega) - V_{D_1} - V_{CE_{sat}}$

                    $\cong 3.4$ v (Logic high)

(*)   A $\rightarrow$ high , B $\rightarrow$ low $\Big\}$ Same analysis as the previous
  or A $\rightarrow$ Low , B $\rightarrow$ high   stat

  – Note : D_2 , $D_3 \Rightarrow$ Protection from high negative voltage

(*) A $\rightarrow$ high , B $\rightarrow$ high

  $Q_2 \rightarrow$ oN (Saturation stat $V_{CE_2} \rightarrow 0.2$ v)

  $Q_4 \rightarrow$ ON   , $Q_3 \rightarrow$ off

  – Q_3 needs $V_{B_3} > 1.4$ v ($V_{BE_3} + V_{D_1}$) to be oN
                    $\underline{\qquad\qquad}$
                         $\searrow$ around 1v

  * $V_0 = V_{CE_4} = 0.2$ v (low state)

  note :
    $D_1 \rightarrow$ Makes only one of "Q_3 , Q_4" $\rightarrow$ ON while the other
        one $\rightarrow$ off