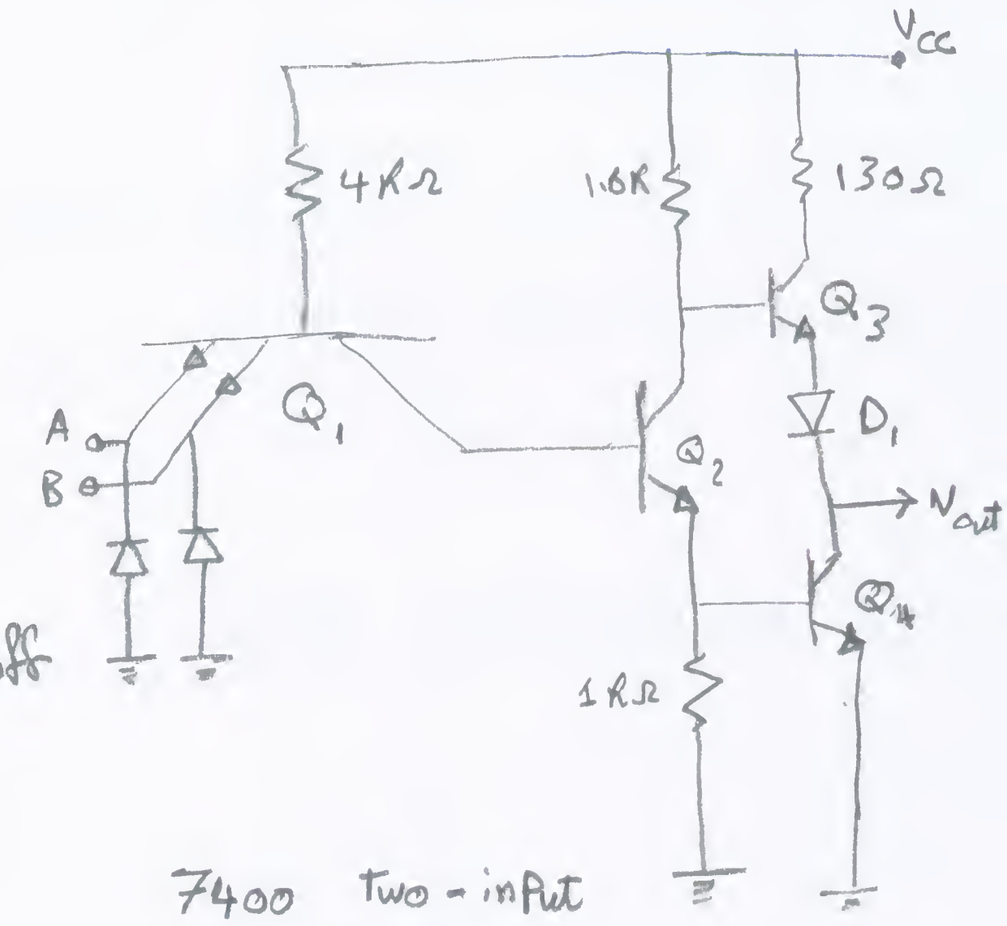
Digital Lec (2) 4/10/2016

(*) TTL family :

- TTL Voltage / Current Rating



7400 Two-input NAND gate

A = 0
B = 0 or each is 0 ⟹ Vout = high stat

$Q_3 \rightarrow$ ON $\quad Q_4 \Rightarrow$ off

Source current (I_{OH})

$= -400\ \mu A$

A = 1
B = 1 ⟹ Vout = Low stat (logic 0)

$Q_3 \rightarrow$ off $\quad Q_4 \rightarrow$ ON

Sink current (I_{OL})

$= 16\ mA$

$I_{ih} = 40\ \mu A$

$I_{iL} = -1.6\ mA$

* Fan-out (Low-stat) $= \dfrac{|I_{OL}|}{|I_{IL}|} = \dfrac{16\ mA}{1.6\ mA} = 10$ gates

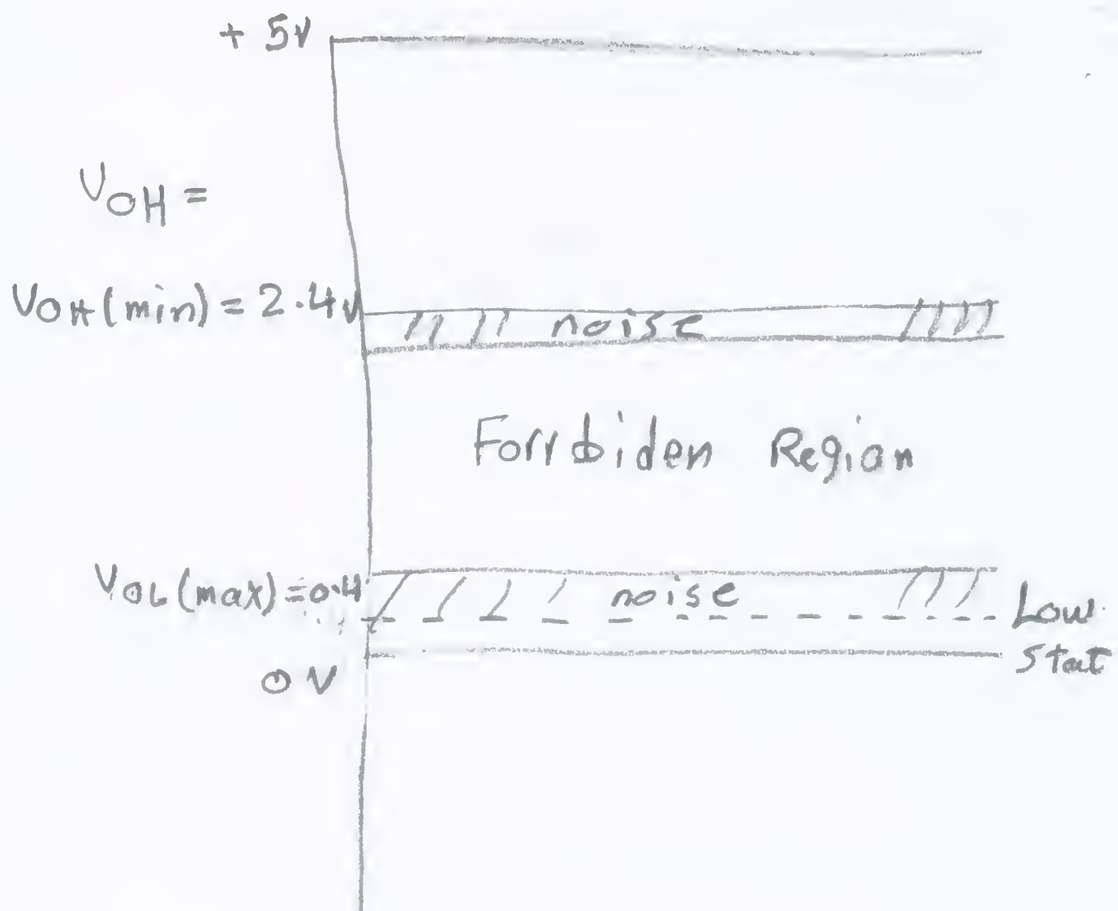
* Fan-out (high-stat) $= \dfrac{|I_{OH}|}{|I_{IH}|} = \dfrac{400\ \mu}{40\ \mu} = 10$ gates

* Noise Margin

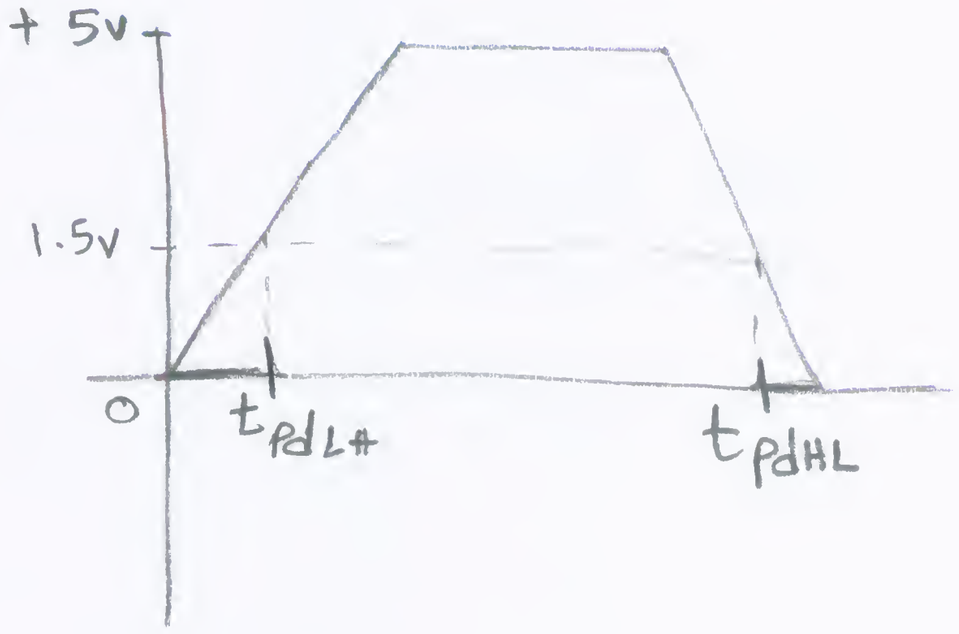
= 0.4 V

up Low - stat voltage (0v: 0.8v)

down high stat voltage (2v: 5v)



* Propagation delay :



$t_{pdLH} = t_{pdHL}$ = 10 n sec

* Rise time t_r

Time of 10% : 90%
of full voltage
0.5 V : 4.5 V

* Fall time t_f

Time of 90% : 10% of full volage
4.5 V : 0.5 V

Power Dissipation :

$P_D = V_{cc} * I_{cc}(av)$

$I_{cc}(av) = \frac{I_{ccH} + I_{ccL}}{2}$