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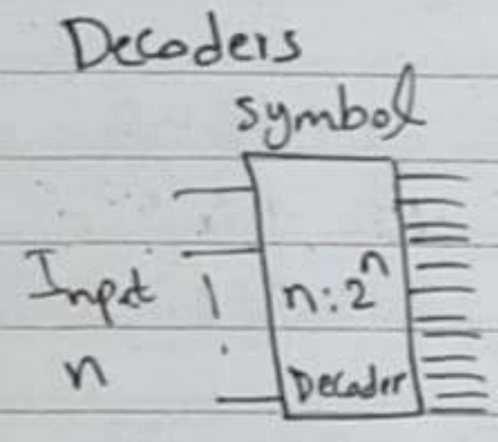
Data processing Circuits

Decoders

symbol



3bit Code word

$2^3 = 8$ bit Code word

3:8 decoder

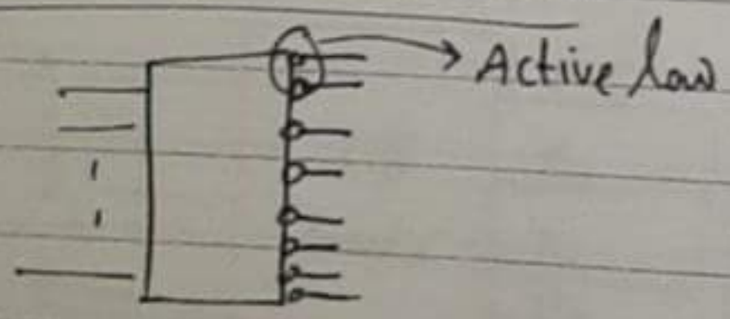
* Table f^n of decoder:- "Active high decoder"

A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Active high decoder ⇝ output corresponding to minterm of input.

D_0 corresponding to "minterm" $\bar{A}\bar{B}\bar{C}$.

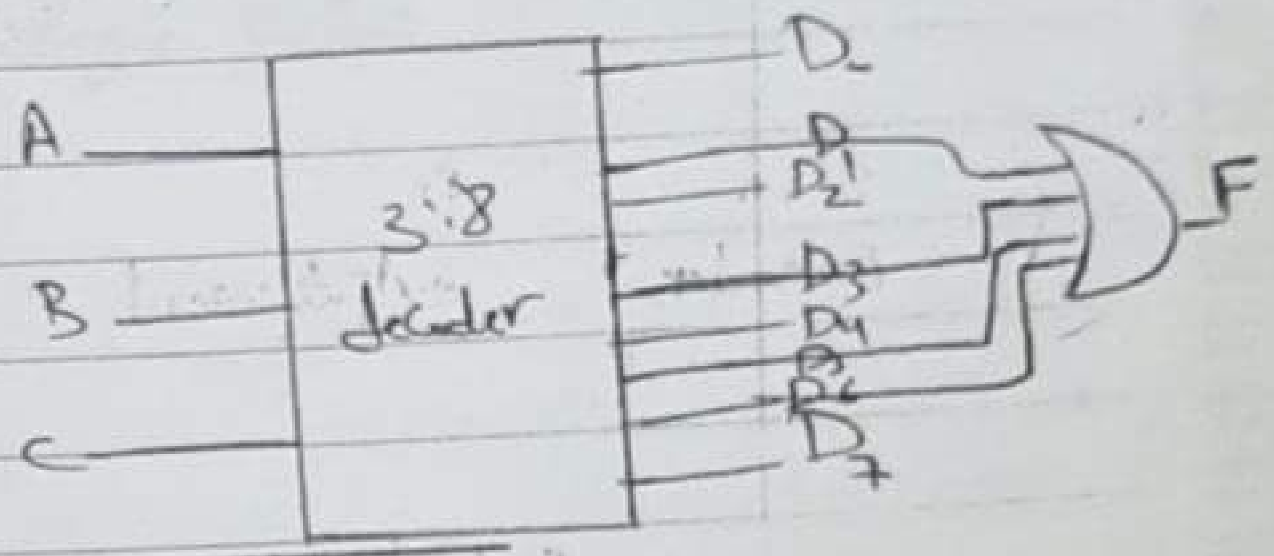
* Symbol of Active low:-



* Realization of Multiple output function using decoder :-

1. Active high output 74138

* $F = \sum m(1,3,5,6)$

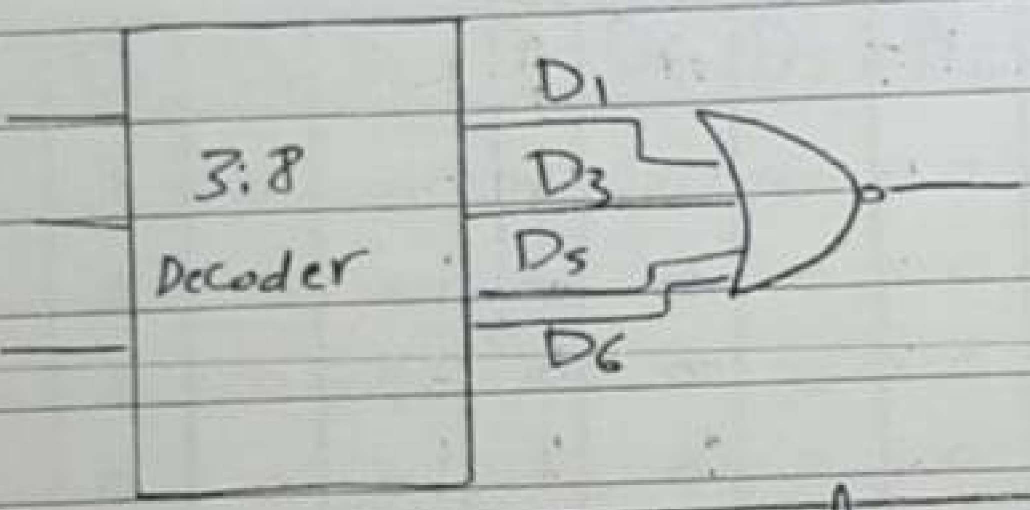


$= \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$

$= m_1 + m_3 + m_5 + m_6$

* $F = \prod M(1,3,5,6)$

$= (\bar{A}+\bar{B}+C) \cdot (\bar{A}+B+C) \cdot (A+\bar{B}+C) \cdot (A+B+\bar{C}) = M_1 M_3 M_5 M_6$



$F = \overline{(m_1+m_3+m_5+m_6)}$

$= \bar{m_1} \cdot \bar{m_3} \cdot \bar{m_5} \cdot \bar{m_6}$

$= M_1 M_3 M_5 M_6$

Active low decoder

* $F = \sum m(1,3,5,6)$

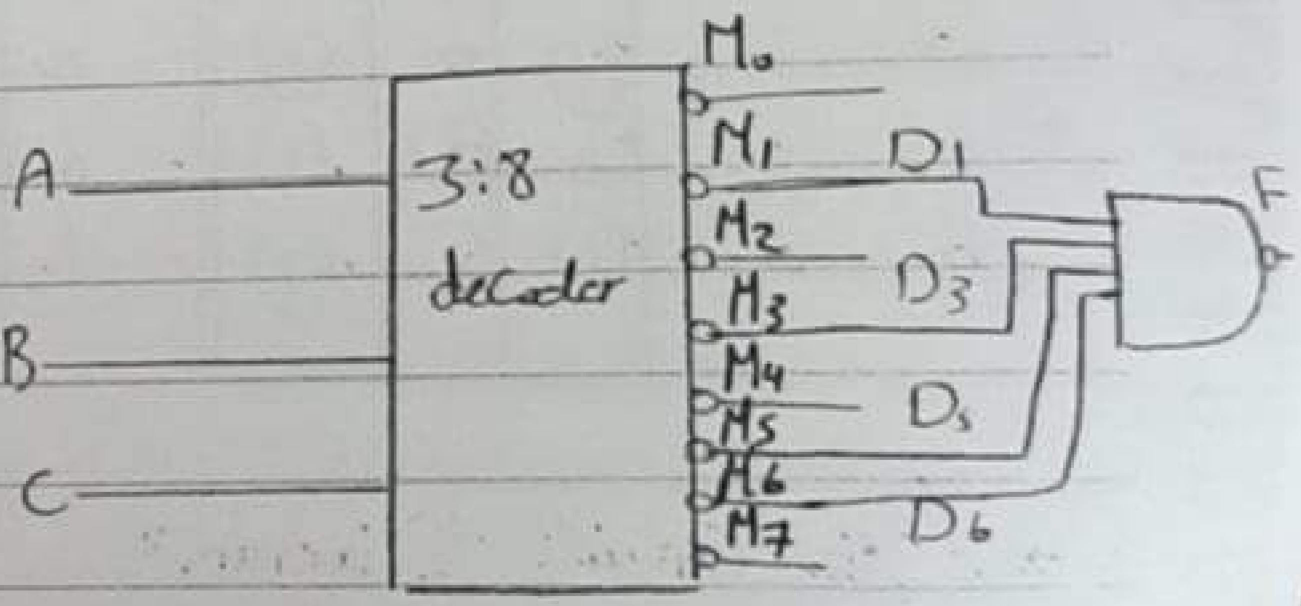
↳ $= \prod M(0,2,4,7)$

$\overline{(M_1 M_3 M_5 M_6)} =$

$\bar{M_1} + \bar{M_3} + \bar{M_5} + \bar{M_6}$

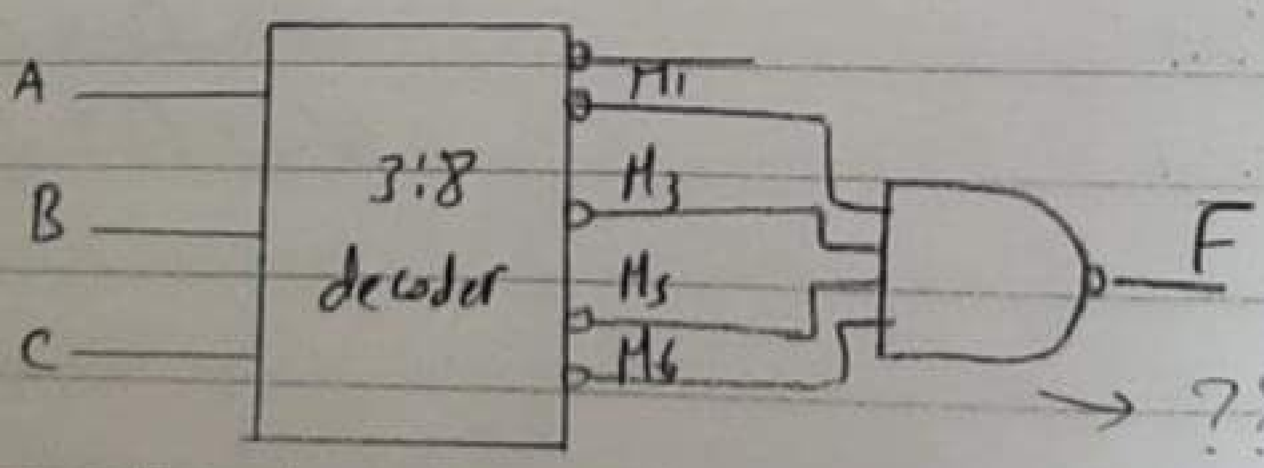
$= m_1 + m_3 + m_5 + m_6$

$\bar{F} = \sum m(0,2,4,7)$



أوضد الادغام المكوع OR ??

* $F = \prod M(1,3,5,6)$

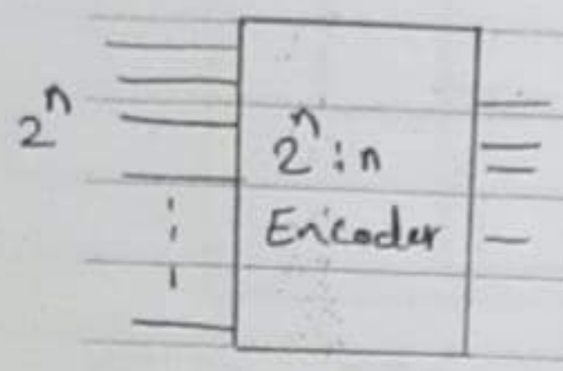


→ ?? AND?

0 → 9

* BCD (Binary coded Decimal) to 7-segment.

* Encoder :- Multiple i/p, Multiple o/p Combinational logic Circuit.



* Octal to Binary Encoder * 8x3 Encoder

"Code word of length 8 to code word of length 3"

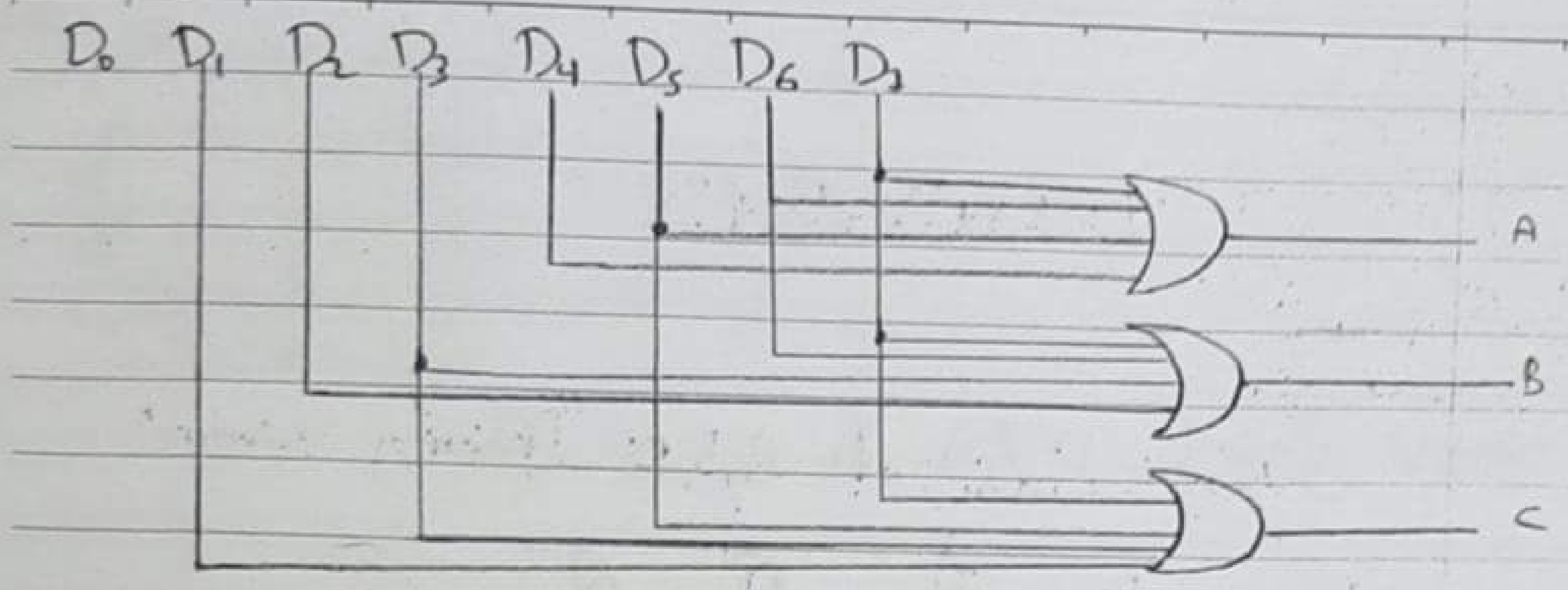
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

* logic circuit "Diagram"

$A = D_4 + D_5 + D_6 + D_7$

$B = D_2 + D_3 + D_6 + D_7$

$C = D_1 + D_3 + D_5 + D_7$



(Zero) $\bar{A}\bar{B}\bar{C}$ * حسب هذه الدائرة أن D_0 غير موصله وبالتالي لما يعبر عن

* لو آلترم واحد داخل الـ Zero "خطأ" undermined output

* حل هذه المشاكل Periority encoder

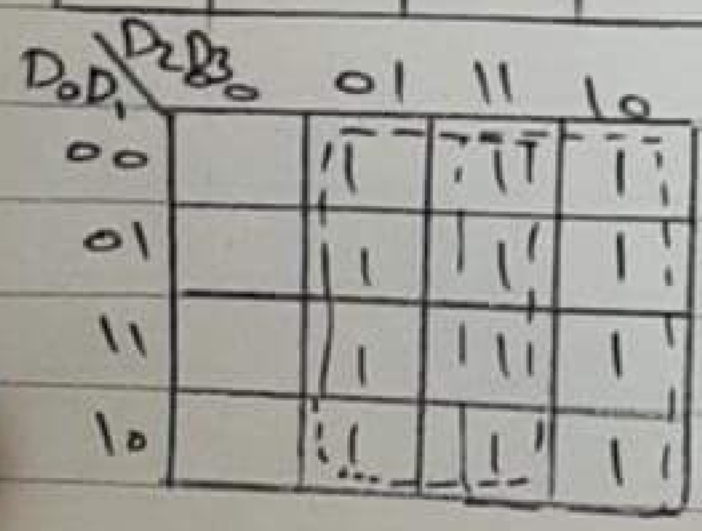
* Periority encoder * → is a practical form of an encoder

(4bit Periority encoder)

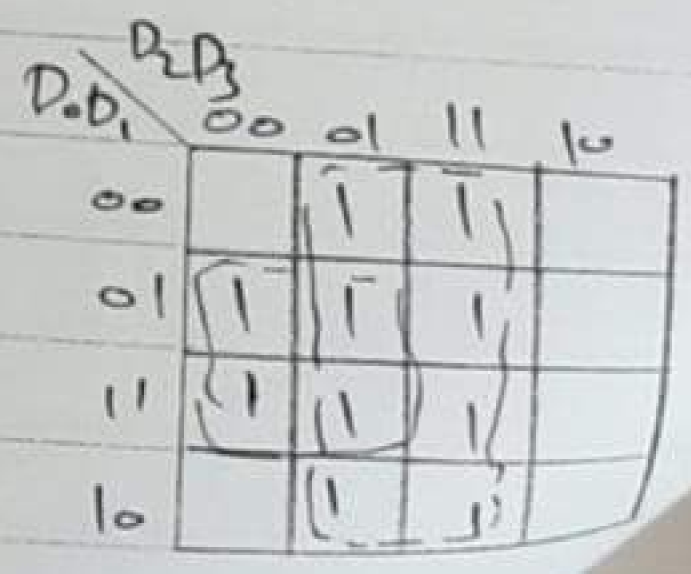
D_0	D_1	D_2	D_3	A	B	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

(input: D_0–D_3; output: A, B, V)

* 8bit نفس الطريقة



→ $A = D_2 + D_3$



← $B = D_3 + D_1 D_2'$

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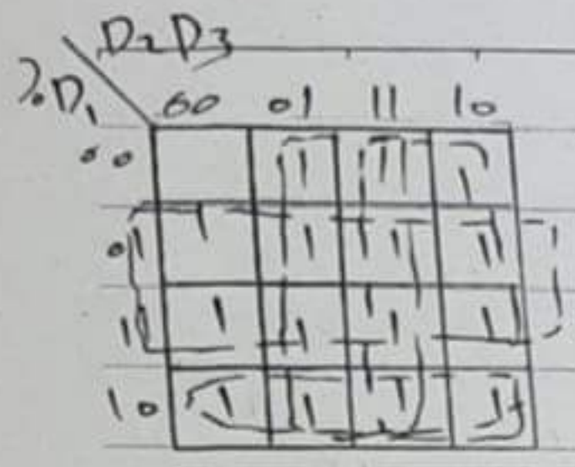

$V = D_2 + D_3 + D_1 + D_0$

* Logic Circuit of A, B, V "Peniority Encoder"