Practical Spread Spectrum: An Experimental Transmitted-Reference Data Modem

By André Kesteloot N4ICK
ARRL Technical Advisor
6915 Chelsea Road
McLean, VA 22101

Introduction

Direct-sequence spread-spectrum systems may be classified into two broad categories: stored-reference and transmitted-reference systems. The circuits I have described so far in these columns[1,2,3,4] have all been of the stored-reference kind, in that a replica of the pseudonoise sequence used at the transmitter site was also stored at the receiver. The main problem then facing the designer was to build into the receiver a circuit which would (a) extract the clock from the transmitted signal, and (b) synchronize the two identical, but out of phase, sequences.

A radically different approach consists in transmitting simultaneously on a frequency F1 the PN sequence XORed with the data, and on a frequency F2 the PN sequence alone. If the receiver uses a second intermediate frequency (2nd IF) equal to (F1-F2), it is possible to modulo-2 add the two signals and recover the original data[5]. This approach has a major advantage: its simplicity. It also has two main drawbacks for military applications: It is easy to either jam the receiver by transmitting a carrier equal to the IF, or for unauthorized listeners to decode the signal with a very simple receiver. Neither of these problems is of concern to the radio amateur, and it was therefore decided to design a simple data link using the transmitted reference approach. The description of the circuitry used will be brief, as most of its elements have already been described in some of my previous articles. (This paper does not aim to be a "construction article," but to give enough pointers to the interested that they may decide to use this information as a starting point, and try their hands at experimenting with spread spectrum.)

Specifications

The equipment described, an experimental modem operating around 70 MHz, can transmit and receive ASCII data at rates higher than 38 kilobauds. The 70-MHz output, about 7 MHz wide, can be up-converted to 440 MHz or any other amateur band of interest.

[1]Notes appear on page 11.

General Description

Referring to Fig 1, the transmitter consists of two oscillators, one on 69.8 MHz, the other on 73 MHz. The 73-MHz carrier is also divided and used as a clock for the pseudonoise (PN) generator. The output of this PN generator is mixed in a doubly balanced mixer with the 69.8-MHz carrier to create a BPSK signal, while the same PN sequence is XORed with the data and then applied in a similar manner to the 73-MHz carrier. The resultant BPSK signals, one centered on 69.8 MHz, the other around 73 MHz, are then *summed* (not mixed) in a hybrid combiner, the output of which, in the time domain, looks like a "double hump" centered on 71.4 MHz as shown in Fig 2. This output, 6.85 MHz wide between the two first nulls, is then up-converted to the 440-450 MHz band. At the receiver, a similar 374-MHz local oscillator creates an IF centered on 71.4 MHz. This signal is split through a hybrid and applied to two identical bandpass amplifiers, one broadly tuned to 69.8 MHz, the other to 73 MHz. The outputs of these two bandpass amplifiers are then fed to the two input ports of an active doubly balanced mixer, the output of which is our baseband data. It is then filtered, amplified and regenerated through a Schmitt-trigger stage.

Transmitter Circuit

As shown in Fig 3, the transmitter consists of two identical frequency synthesizers, one functioning on 73 MHz, the other on 69.8 MHz. (Only one, the 73 MHz, is shown for simplicity.) The circuit is comprised of an MC1648 voltage-controlled oscillator tuned to the frequency of interest, an MC3396 divide-by-20 stage, and a MC145151 synthesizer chip. (The operation of this synthesizer was described in more detail in the November 1988 *AMRAD Newsletter*, Vol XV, No. 5.) The output of the MC3396 divider-by-20 stage is a clock at 3.65 MHz. This clock is buffered by four sections of U4, a 4049 hex-inverter, and used for three separate functions. After another division by two in U9B, a 7474 flip-flop, the resulting 1.825-MHz square wave clocks a 7-stage PN generator comprised of U5, a 74164 shift register, and U6, a 7486 XOR chip. This PN generator arrangement has already been described previously.[6] The PN sequence is used directly to drive the IF port of an SBL-1 passive doubly balanced mixer (only one of two shown on this diagram).

The PN sequence is also XORed with data. This data can be either an internally generated test square wave, or some external signal. The square wave is the clock divided by 100 (in U7 and U8), while the external signal is whatever is fed to the RS-232 port. Either signal, selected by S1, is then resynchronized via U9A, a 7474 flip-flop. The output of the flip-flop is then XORed with the PN sequence in U6D, which then drives the IF port of a second doubly balanced mixer (see Fig 1). This output is shown as point "A" on Fig 1.

Two separate frequency synthesizers were used so that I could easily adjust, for experimental purposes, the frequencies of the two carriers, and hence, the IF. Should the reader wish to duplicate this setup, it would be much simpler to use two straightforward crystal oscillators.

The outputs of the two doubly balanced mixers are then added in a summing network, here a TV antenna coupler/hybrid combiner (Radio Shack® part #15-1141). One could also manufacture one's own by winding a few turns of trifilar wire on a ferrite core, but the Radio Shack part is perfectly satisfactory, and comes already shielded and fitted with F connectors.

The output of the summing hybrid is centered on 71.4 MHz, and occupies a minimum bandwidth of about 6.9 MHz. As shown in Fig 1, the output of the summing hybrid feeds yet another doubly balanced mixer, wherein is mixed the 374-MHz local oscillator signal, thus heterodyning the whole band, from 67.975 to 74.825 MHz to the 440-MHz band.

Although the heterodyning and amplification process are by no means trivial, they are not novel and have already been covered in the literature. This article concentrates on the spread-

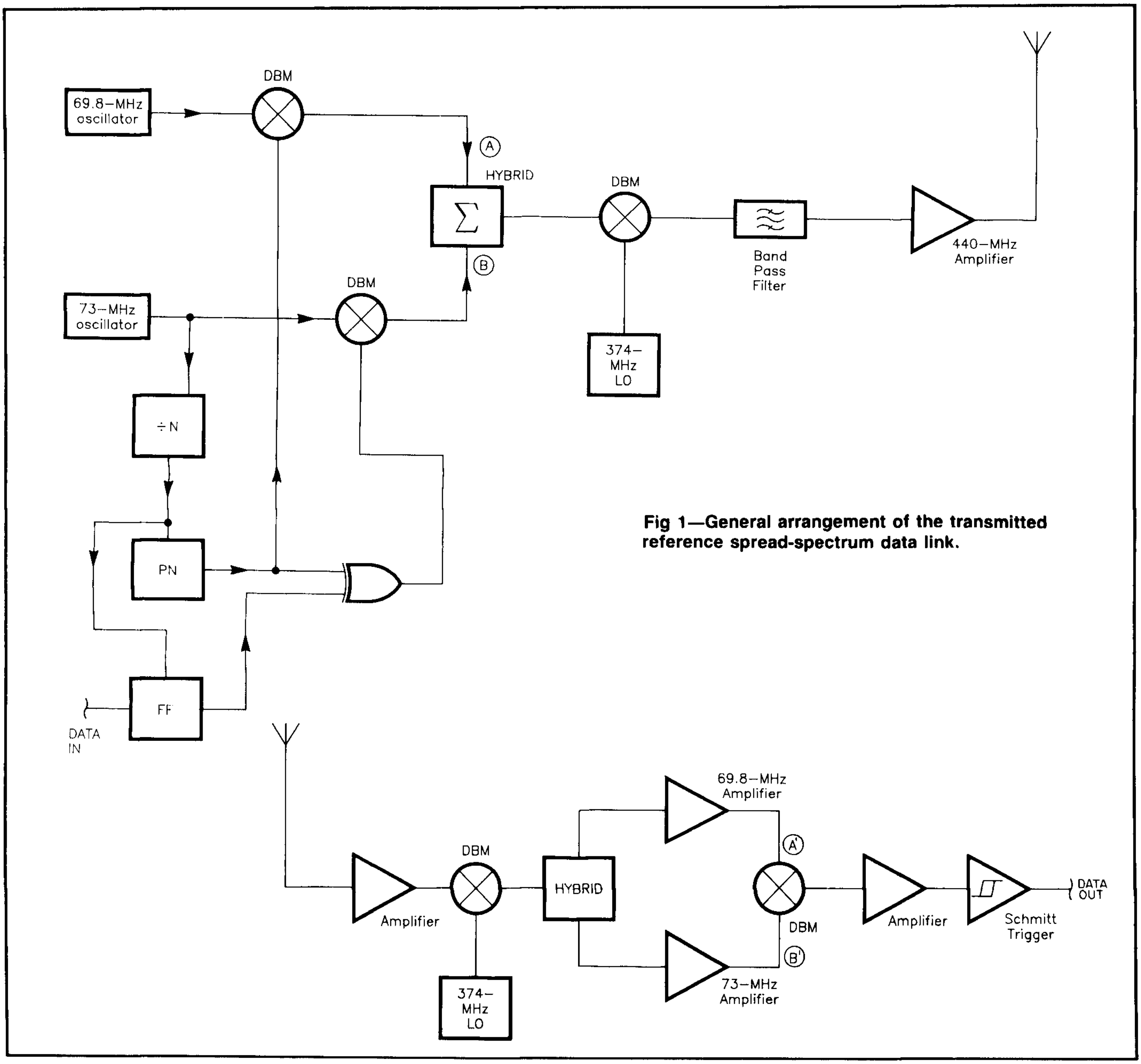


Fig 1—General arrangement of the transmitted reference spread-spectrum data link.

spectrum aspect of the project.

The Receiver

Fig 1 shows the general arrangement, while Fig 4 shows the details. After mixing with a local 374-MHz oscillator, the incoming signal is once again centered on a 71.4-MHz intermediate frequency. This signal is then split into two paths, each fed to a band pass amplifier, one centered on 69.8 MHz, the other around 73 MHz. The outputs of those two amplifiers are shown as A and B in Figs 1 and 4. These outputs are now fed to the two input ports of U101, an MC1496P active doubly balanced mixer. In the absence of an input signal at the transmitter, the two PN streams are in phase, but if data is applied, that portion of the PN sequence which corresponds to a "data high" will be inverted. (See reference 1 for additional details of a similar data recovery scheme.)

A replica of the data is thus available at the output of the MC1496P DBM. After passing through a lowpass filter, the data is amplified through U102 a CMOS op-amp, and finally regenerated through U103, a 4093 Schmitt trigger. RS-232 level conversion and buffering is then accomplished with U104, an MC1488 IC.

Operation

Testing was conducted as shown in Fig 5, with the data used being ASCII characters generated by the computer. A test program was written by Lawrence Kesteloot, N4NTL, and is available on the

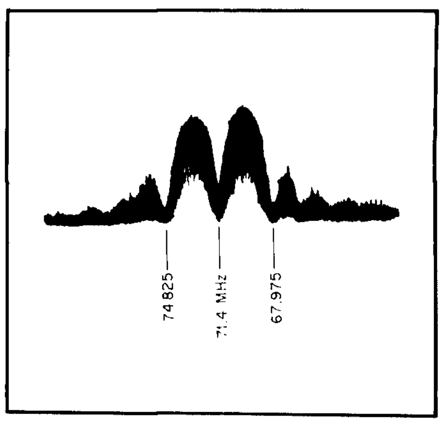
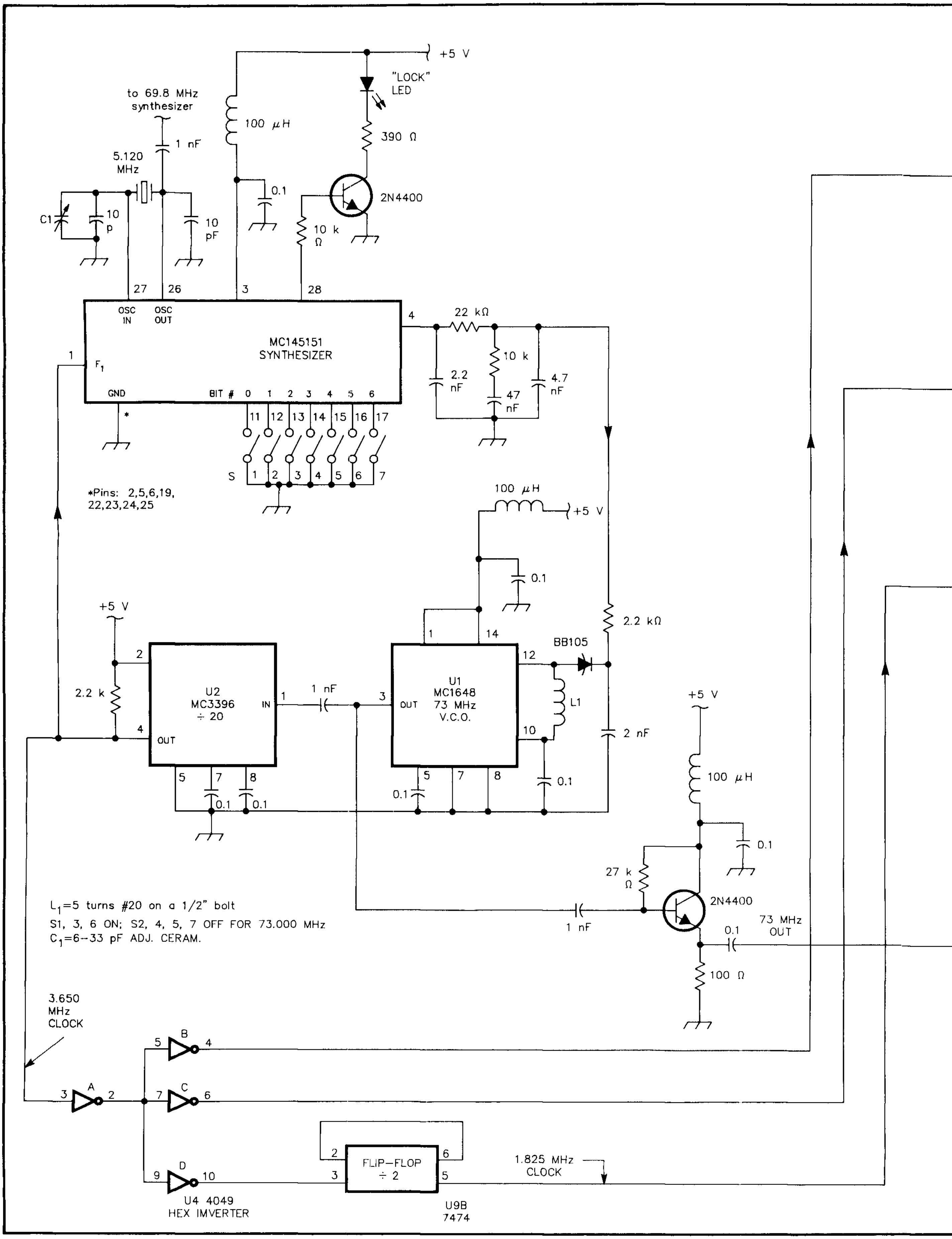


Fig 2—Output of transmitter summing hybrid.


+5 V
"LOCK" LED
to 69.8 MHz synthesizer
1 nF
5.120 MHz
100 μH
390 Ω
0.1
2N4400
C1
10 p
10 pF
10 k Ω
27
26
3
28
OSC IN
OSC OUT
4
22 kΩ
MC145151 SYNTHESIZER
10 k
2.2 nF
4.7 nF
47 nF
1
F_1
GND
BIT # 0 1 2 3 4 5 6
11 12 13 14 15 16 17
S 1 2 3 4 5 6 7
*Pins: 2,5,6,19, 22,23,24,25
100 μH
+5 V
0.1
+5 V
2.2 k
2
U2 MC3396 ÷ 20
IN
1
1 nF
3
OUT
4
U1 MC1648 73 MHz V.C.O.
OUT
1
14
12
BB105
L1
10
2.2 kΩ
2 nF
5
7
8
0.1
0.1
0.1
0.1
+5 V
100 μH
0.1
27 k Ω
2N4400
1 nF
0.1
73 MHz OUT
100 Ω
L_1=5 turns #20 on a 1/2" bolt
S1, 3, 6 ON; S2, 4, 5, 7 OFF FOR 73.000 MHz
C_1=6–33 pF ADJ. CERAM.
3.650 MHz CLOCK
5 B 4
3 A 2
7 C 6
9 D 10
U4 4049 HEX IMVERTER
FLIP–FLOP ÷ 2
2
6
3
5
U9B 7474
1.825 MHz CLOCK

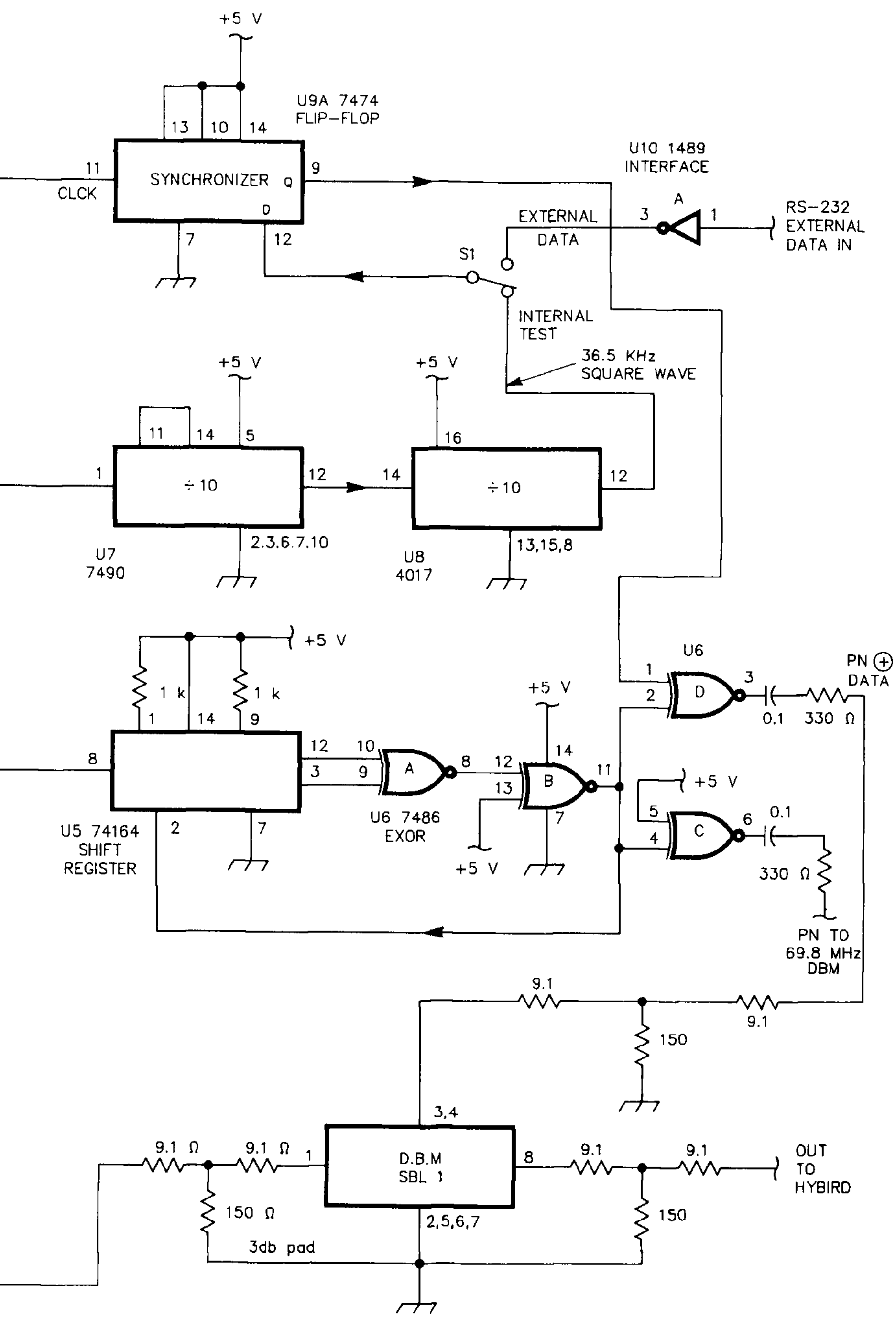


Fig 3—Transmitter circuit.

AMRAD BBS in the spread-spectrum area[7]. The program continuously sends, in ASCII format, all the letters of the alphabet, and after each letter, checks whether the letter coming back from the receiver is the same as the one just sent. The highest speed (easily) available at the RS-232 port of my IBM® clone is 38 kilobauds, and Fig 6 shows on the upper trace, the signal at the input of the transmitter, while the lower trace shows the receiver output. The two signals are essentially indistinguishable from each other, and we may infer from these preliminary results that much higher speeds are attainable. (The final version of the hardware will probably include a more sophisticated data interface, such as NRZ, etc.) At 38 kilobauds, during tests repeated over several days, the error rate was always 0 (zero) error for over 2,000,000 (two million) letters of transmitted data. This kind of error rate is due, at least in part, to the fact that this was an ideal bench setup without any interference at the IF. In a practical realization, one would obviously benefit from the addition of an LC circuit tuned to the IF of interest, at the output of U101 (between pin 12 and ground). Another circuit which would need to be added is an automatic gain control (AGC) for the IF strip, something not exactly trivial for direct sequence.

Acknowledgements

Some of the ideas implemented in this design were originally discussed with two other members of the AMRAD core group: Glenn Baumgartner, KAØESA, and Chuck Phillips, N4EZV. Their support is gratefully acknowledged.

Figures 4-6 appear on the next page.

References

[1]A. Kesteloot, "Experimenting with Direct Sequence Spread Spectrum," *QEX* Dec 1966, pp 5-9.

[2]A. Kesteloot, '"Practical Spread Spectrum: A Simple Clock Synchronization Scheme," *QEX* Oct 1986, pp 4-7.

[3]A. Kesteloot, "Practical Spread Spectrum: Achieving Synchronization with the Slip-Pulse Generator," *QEX* May 1988, pp 6-11.

[4]A. Kesteloot, "A Direct Sequence Spread Spectrum UHF Link," *QST* May 1989.

[5]R. Dixon, *Spread Spectrum Systems*, (New York, Wiley) 2nd ed, 1984 pp 224-225.

[6]*The 1989 ARRL Handbook*, Bruce Hale, Ed, (ARRL, Newington, CT), 1988, Chap 21, p 12.

[7]The AMRAD BBS: 703-734-1387. (300/1200/2400 baud, 8 bits, 1 stop bit, no parity.)

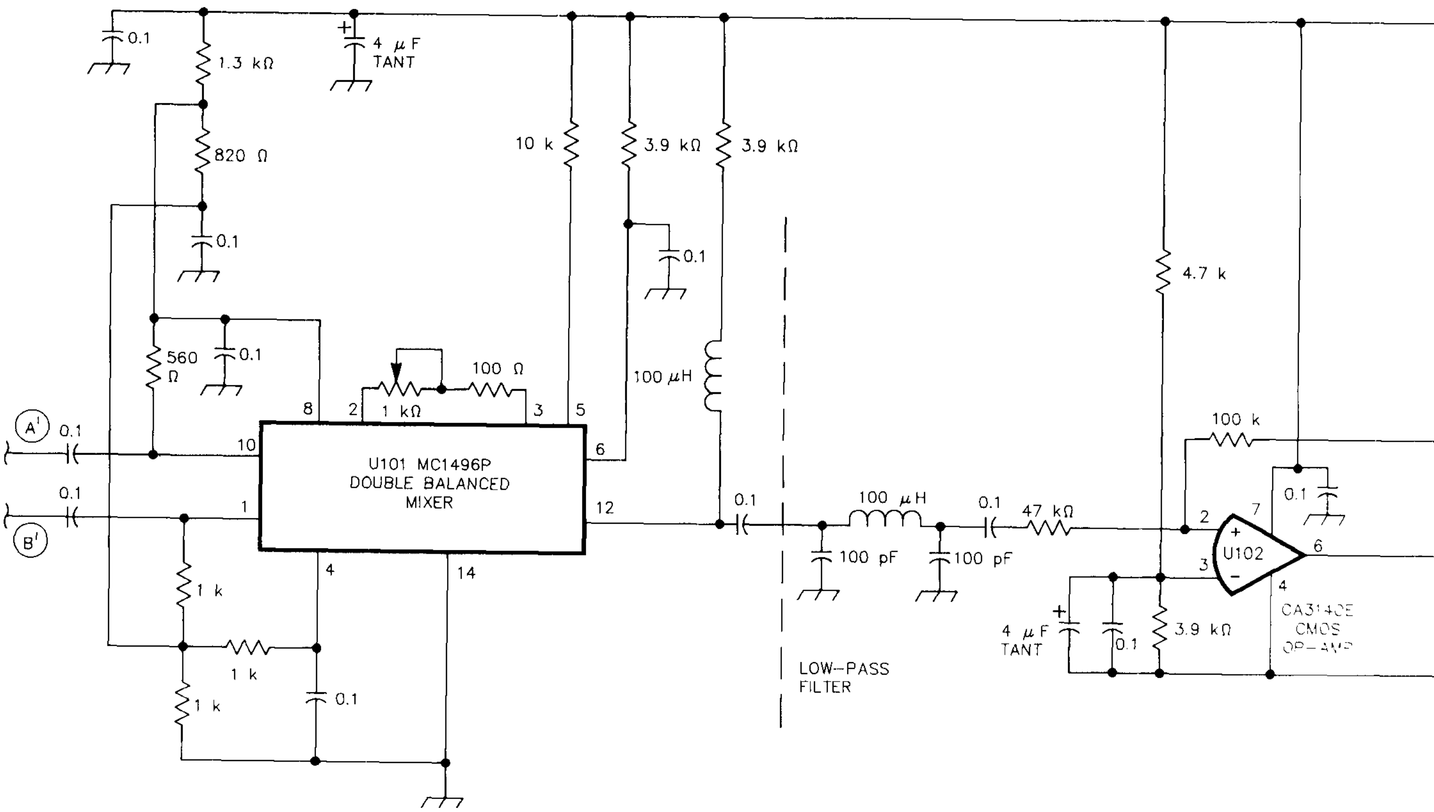


Fig 4—Demodulator circuit.

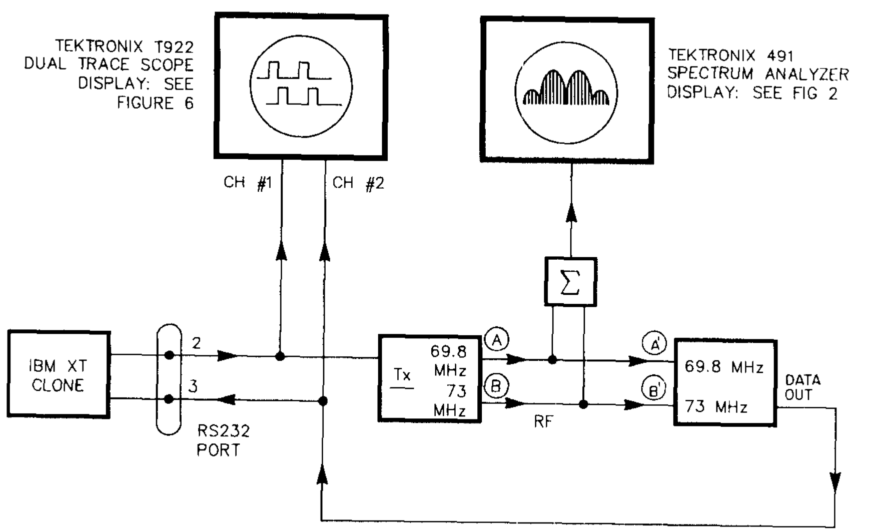


Fig 5—Test set-up transmitted reference spread-spectrum data link.

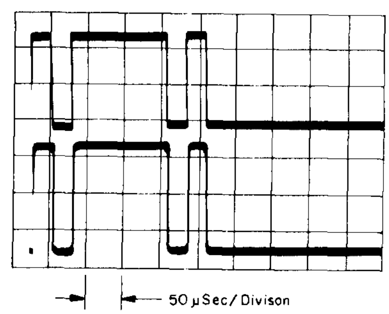
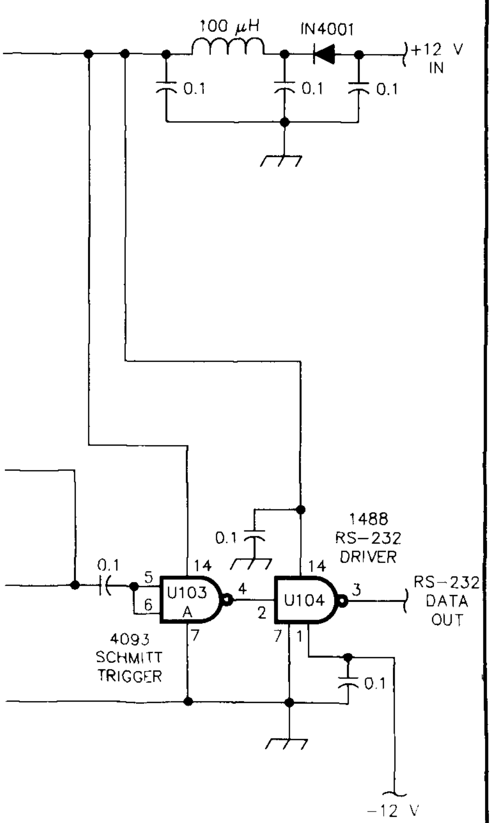


Fig 6—The letter "A" at 38 kilobauds. Upper trace is the transmitter input, lower trace is the receiver output.



Bits

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PLAN-13 is available on disk for the C-64®, C-128® (in the C-64 mode), TRS-80® (I/III), IBM-PC®, Apple® IIe and IIc, and for PC compatibles. All disks are 5¼ inch. C/PM or 3½-inch disks are available on special order (and additional donation). To order PLAN-13, send a minimum donation of $25 to PLAN-13, Project OSCAR, Inc. (All donations for PLAN-13 will be put back into the Amateur Satellite Program.)

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Commodore C-64 Version: Provided on a 5¼-inch diskette in compiled form. The user will find their own QTH data in addition to Keplarian data stored on the disk. Information can be updated using utility programs provided. Output may be sent to the screen or printer.

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