

Design of PHEMT Frequency Triplers with Conversion Gain at 6 GHz

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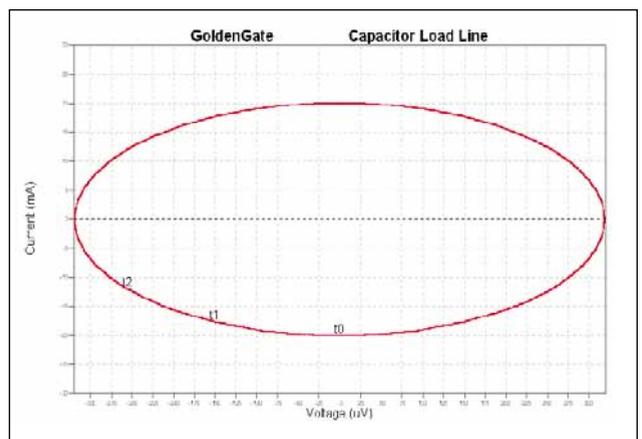
Since the early 1960s, varactor frequency multipliers have been built with nonlinear low-loss diodes using the nonlinear properties of the PN junction. These classic designs typically have a conversion loss approaching 3 dB [1]. With microwave nonlinear transistors, the frequency multipliers may be built with conversion gain.

The nonlinearity of the drain current source is the most effective element in the generation of harmonics. Because of the inherent gain of the PHEMT, frequency multipliers with gain are now possible. Computer simulation of nonlinear circuits using nonlinear PHEMTs will provide invaluable insight to the performance and reliability of the design by revealing the dynamic load line and other features of the design, which are immeasurable with normal instrumentation.

Using a new CAD package for nonlinear circuit design from Xpedion Design Systems, Inc., the design of a PHEMT tripler for 2 to 6 GHz with essentially zero dB gain and 0 dBm power will be presented. The best result was 4.1 dB gain measured with an input power of -1 dBm. Calculations predicted gains of 6 to 10 dB, but the device was biased high and operating in regions of possible burnout, which can easily be observed with the nonlinear CAD analysis. The circuit uses the LP6836-P70 packaged PHEMT from Filtronic Solid State, which is a 360 μm perimeter 0.3 μm gate transistor. The optimum bias was found both in the lab and on the computer to be in the range of:

$$V_{ds} = 1.2 \text{ to } 2.6 \text{ V}$$

$$V_{gs} = -0.70 \text{ to } -2.7 \text{ V}$$



▲ Figure 1. Clockwise load line of a capacitor.

$$I_{ds} = 20 \text{ to } 40 \text{ mA}$$

which is a rather low drain voltage and low drain current ($I_{dss} = 100 \text{ mA}$).

The design procedures for even and odd harmonic multipliers are different [2]. For odd harmonic multipliers, the odd harmonics should see a high impedance at the drain while the even harmonics should see a short circuit (low impedance) at the drain. For even harmonic multipliers, the opposite is true. The amount of output harmonic power is based upon the size and bias of the transistor. The design procedure used here should work equally well for BJTs, HBTs, MESFETs or any other 3-terminal device.

Nonlinear CAD

Envelope simulation is an advanced form of harmonic balance analysis, where the harmonics may be modulated or varied in such a way to increase the accuracy and speed of the calcula-

tion [3]. The time domain transient solutions that may be obtained from both harmonic balance and envelope simulations will lead to QL and hence phase noise performance [4]. The envelope-transient technique, used in conjunction with harmonic-balance and linear-RF simulation, is the best-suited technique (and the only practical one) for all present wireless communication designs. Using envelope simulation, one can analyze circuits where inputs are simulated by RF carriers with complex, time-varying envelopes such as amplitude and phase modulations. Their spectra can represent transient signals or pseudo-random digital modulation, and can include periodic signals having discrete spectral lines, such as those from a mixer or amplifier under multi-tone excitation.

Before proceeding to the output design, the dynamic load line of any one-port (or two-port at the output port) needs to be understood in detail. It will be shown that a clock-wise rotation represents nonlinear capacitance performance (voltage leads current by 90 degrees), and the other direction represents nonlinear inductance performance. These “dynamic load lines” have been available from harmonic balance simulators since the late 1980s. In a power amplifier, the load line may be inductive over a portion of the cycle and capacitive over another portion of the cycle. This seems to imply that the load line is more resistive (a straight line) over the cycle and thus delivers more power at a higher efficiency.

The study of frequency multiplier load lines is in its infancy, but some preliminary results will be included in this article. Different CAD products seem to predict different load lines; the result included in this paper uses the Xpedion nonlinear CAD tools primarily in the harmonic balance mode.

A simple capacitive load line (CW) is shown in Figure 1, where the voltage and current of an ideal capacitor have been plotted in the time domain, and the resulting load line, a circle in the CW direction, is illustrated. By following the location of points, the dynamic load line can be better understood. This is an extremely important tool in understanding all nonlinear circuits: oscillators, mixers, amplifiers, frequency multipliers and other related circuits.

Tripler design

The PHEMT tripler was designed using Xpedion CAD for nonlinear circuits. The frequencies were $f_0 = 2.125$ GHz at the input and $3f_0 = 6.375$ GHz at the output, with a nominal input and output power of 0 dBm. The LP6836-P70 PHEMT was selected for its good microwave gain, 12 dB at 15 GHz. The primary nonlin-

Parameter	Value	Conditions
I_{\max}	190 mA	$V_{ds} = 2$ V $V_{gs} = 1$ V
G_m	95 mS	$V_{ds} = 2$ V $V_{gs} = 0$ V
V_p	-0.8 V	$V_{ds} = 2$ V $I_{ds} = 2$ mA
BV_{gd}	-16 V	$I_{gd} = 2$ mA
Max P_{in}	80 mW	
Max T_{ch}	150° C	
P_{1dB}	23 dBm	$V_{ds} = 5$ $V_{I_{ds}} = 50\% I_{dss}$ $f = 15$ GHz
$P_{diss}(\max)$	800 mW	

▲ Table 1. Important parameters for the LP6836-P70 transistor.

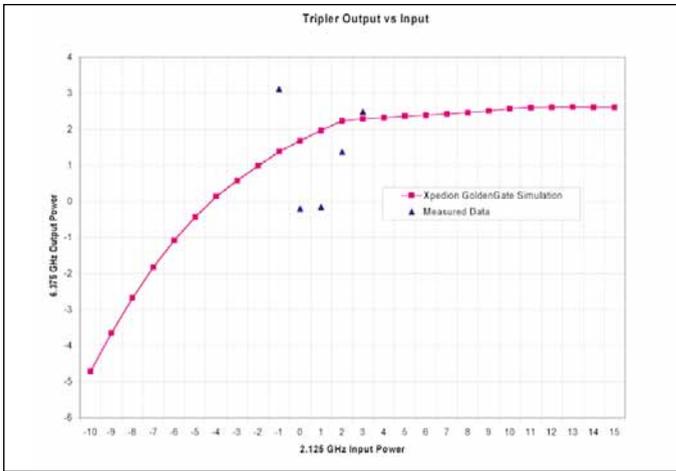
earities in this transistor are the drain current generator and the nonlinear gate capacitances, which are modeled by the Statz-Pucel model. The Curtice Cubic model was used for the design and is available on the Filtronic Solid State web site, <http://www.filtronicssolidstate.com>, nonlinear models. In addition to this model, the Angelov model will soon be implemented for this transistor. Some important parameters for this transistor are given in Table 1.

The design procedure proceeds as follows. The S_{11} at 2.125 GHz is matched to a 50 ohm generator. Also, the stability factor, k , must be greater than unity at all frequencies in all 3-terminal transistor circuits. Thus, a 20 ohm resistor has been added in the gate bias stub to achieve this stability.

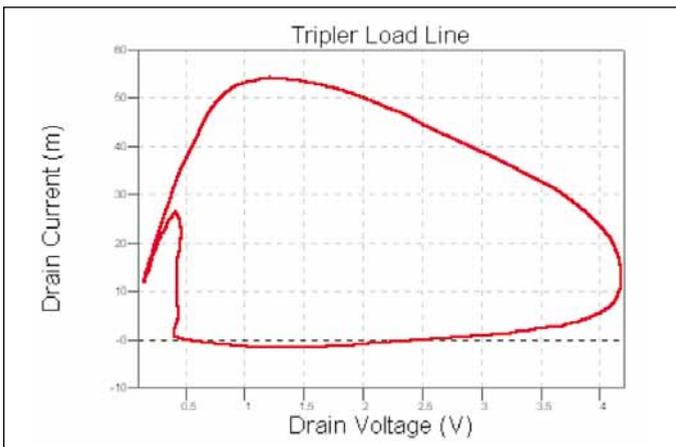
The load circuit is then designed and is the most crucial part of any generator design. All signal generators are one-ports, including this (and any other) frequency multiplier. The input port is irrelevant in the signal generator mode. Understanding the circuit performance and the role of the device is essential to improving the circuit performance. With the help of harmonic balance and envelope simulation techniques, the nonlinear device behavior may be deduced for various circuit conditions such as bias and input drive level.

Returning to the output design, the following steps are required:

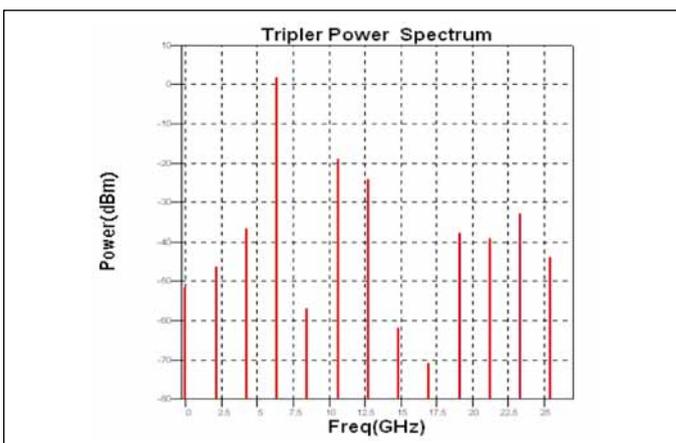
1. A low-loss bandpass filter is designed for the output frequency, 6.375 GHz.
2. A 50 ohm line of $\lambda/4$ is inserted between the filter and the transistor. Since the filter is approximately a short circuit at the fundamental, the drain of the transistor sees an open circuit and therefore a maximum fundamental voltage and a maximum 3rd (and other odd harmonics) at the drain.
3. An idler stub is inserted at a voltage minimum on the drain which is a $\lambda/4$ short circuited transmission-line stub at f_0 . It is therefore an open circuit at all odd frequencies and a short circuit at all even harmonics.



▲ **Figure 2. Simulated and measured 6 GHz levels for a swept range of 2 GHz drive levels.**



▲ **Figure 3. Tripler load line, rotating clockwise.**



▲ **Figure 4. Simulated tripler output spectrum.**

Next, the bias condition for optimum gain is found by tuning these variables for a given input power. Usually, the design is found for some optimum bias where the

measurements do not agree. Then the bias for best gain is found in the lab, which can then be verified on the computer. This was the design cycle for this tripler.

Frequency (GHz)	Power (dBm)
2.125	-30
4.250	-35
6.375	0
8.500	-30
10.625	-35

▲ **Table 2. Typical data for harmonic levels.**

Measurements

In Figure 2 the third harmonic output has been plotted versus the fundamental input power for both the measurements and the design calculations. The optimum measured gain occurred for an input power of -1 dBm and an output power of 3.1 dBm at a bias of $V_{ds} = 1.0$ V, $V_{gs} = -0.77$ V and $I_{ds} = 19.6$ mA. The output power saturates at about 9 dBm for a bias of $V_{ds} = 2.8$ V, $V_{gs} = -3.82$ V, $I_{ds} = 35.9$ mA and $P_{in} = 15$ dBm (see Figure 2). The gain is found to be ± 4 dB, or essentially 0 dB in the linear range. Several devices were tested with various values of I_{dss} , and the measurements plotted in Figure 2 include all of these transistors. We have seen CAD designs with as much as 12 dB gain, but the drain voltage is much too high for safe and reliable operation. This can only be discovered by using a nonlinear simulation and investigating the dynamic load-line.

The typical conversion gain is near 0 dB at an input power of 0 dBm. This has been verified with many devices. The most critical tuning is the idler circuit described above. The substrate material was 10 mils Rogers 6002, with $\epsilon_r = 2.94$, $h = 10$ mils and $\tan \delta = 0.003$. Other materials could give better performance (lower loss tangent). The metal is gold with $t = 5$ μm . The circuits are fabricated at Filtronic Solid State using their standard low-cost process for hybrid microwave integrated circuits.

The dynamic load is plotted in Figure 3 for a bias of $V_{ds} = 3.4$ V, $V_{gs} = -0.9$ V and $P_{in} = 15$ dBm. The approximate slope is 200 ohms. Typical data for harmonics are shown in Table 2 and Figure 4. Using the envelope-transient technique, the startup waveform is shown in Figure 5. The circuit diagram created for simulation is shown in Figure 6.

Using the Leeson noise theory for oscillators (Ref. 4), the phase noise of this tripler may be calculated, assuming $Q_L = 62$, $P_o = 0$ dBm, $F = 3$ dB and $f_c = 10$ MHz (flicker noise corner frequency). The calculation gives

$$\mathcal{L}(f_m) = \mathcal{L}(100 \text{ kHz}) = -100 \text{ dBc}$$

For an input frequency of 2.125 GHz, this is a phase noise of -112 dBc, since the phase noise is expected to increase by 12 dB for a tripler.

Conclusions

Using design procedures given in the literature and new PHEMTs with good microwave gain, a state-of-the-art tripler has been designed using a new nonlinear CAD package from Xpedion Design Systems, Inc., and tested for the 2-6 GHz range with 0 dB gain at an unusually low drain voltage bias point. Diode multipliers will always have loss, so this is an important bench-mark for future frequency multipliers. ■

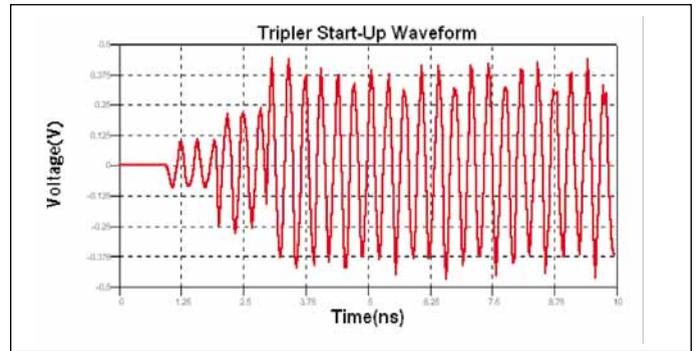
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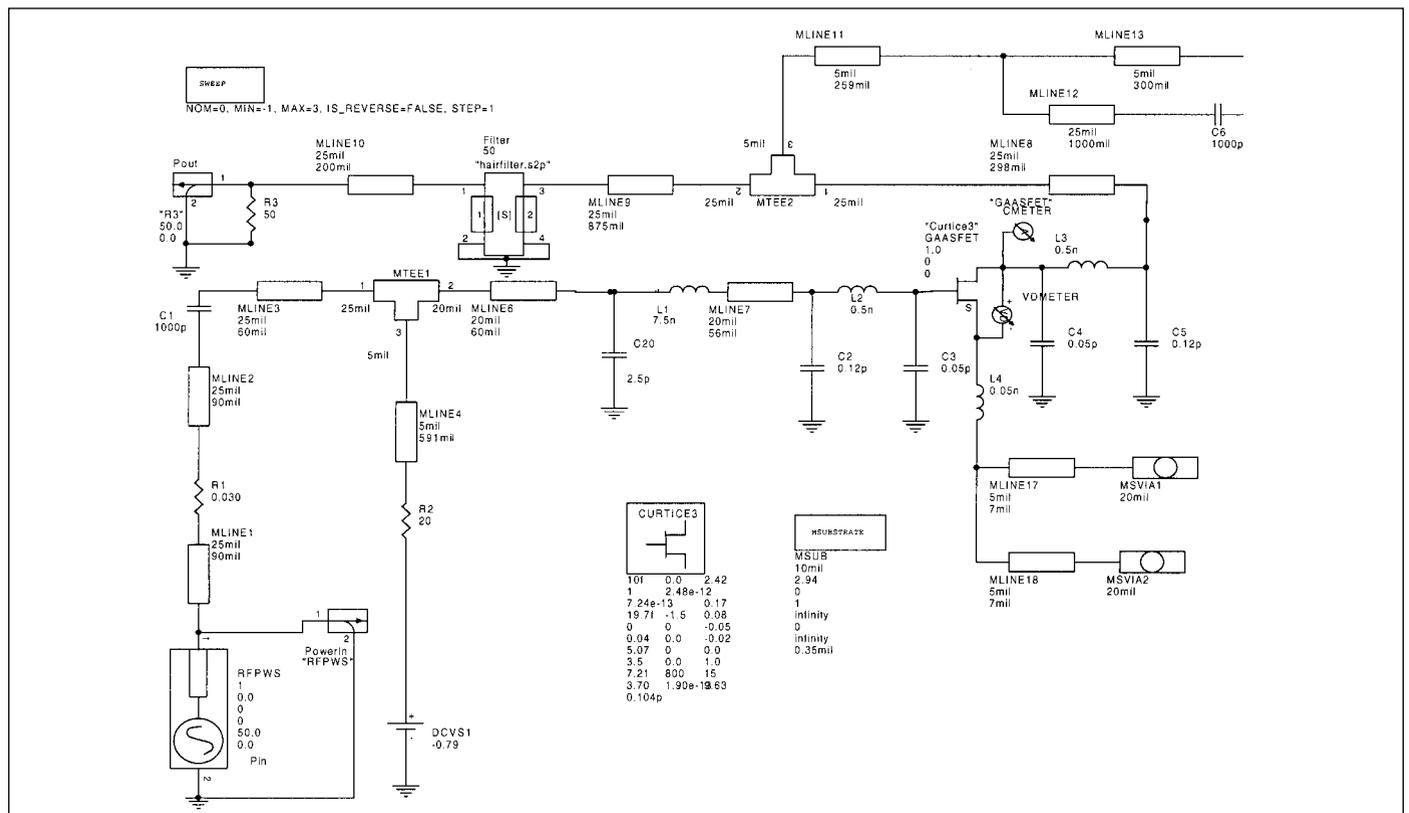
▲ Figure 5. Simulated tripler startup waveform.

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▲ Figure 6. Circuit diagram of the tripler, as defined for simulation in Expedion's GoldenGate.