All Digital Fractional-*N* Synthesizer for High Resolution Phase Locked Loops

Part 2: Performance results for a third order loop

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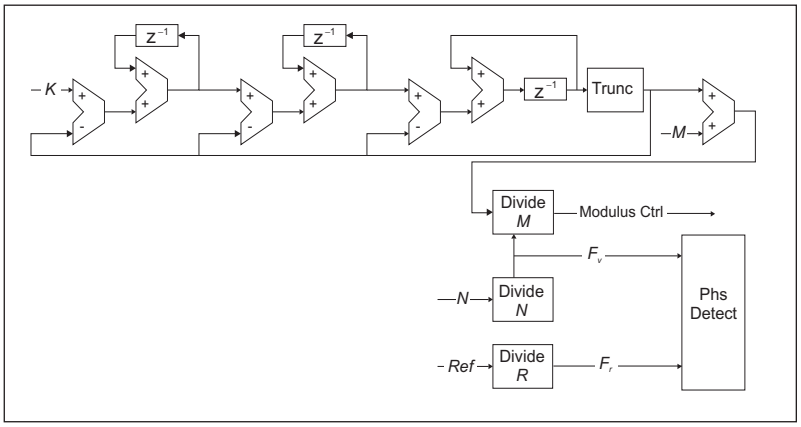
In the first part of this article, we surveyed principles of fractional-N PLL, including basic architeture, sigma delta modulation and output analysis. Here, we will show the results of third order PLL loops, a new technology using all digital DSP for oversampling, noise shaping and spurious rejections.



■ **Figure 1. Third order sigma delta all digital fractional.**

First order loop

To illustrate the first order loop, we will review a couple of examples using a first order sigma delta modulator. This is exactly what we earlier called fractional-*N* of the first order and is implemented simply with a single accumulator. The duty cycle of the accumulator carry out is always K/F; there is no waveshaping. For input K, we expect the accumulator to roll over (produce a carry out) K every time F cycles.

The first example is the output of the first order sigma delta modulator for input K=1, truncation = 4 bits, such that the fractionality $K/F = 1/2^4 = 0.0625$: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1. Spurious will show at $F_r/16$ and multiples.

The second example is the output of a first order sigma delta modulator for input K=13, truncation=4 bits such that the fractionality $K/F = 13/2^4 = 0.8125$: 0 1 1 1 1 0 1 1 1 1 0 1 1 1 1 1. Spurious will show again at $F_r/16$ and multiples, since the greatest common divisor of 13 and 16 is 1. However, for K=4, the waveform will be 0001000100010001, so spurious will show only at $F_r/4$ and multiples; for K=6, only at $F_r/2$ and multiples. Note that the greatest common denominator (16,6)=2.

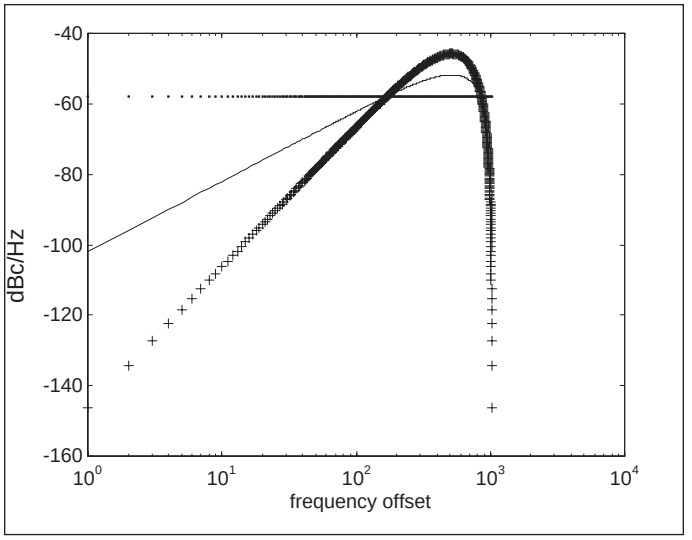
Third order loop

The implementation (fractional control section) shown in Figure 1 was used to simulate a third order sigma-delta modulator. Figure 2 plots the theoretical spectral shaping output for a first, second and third order sigma-delta system. Figure 3 plots the theoretical and simulated output for a third order sigma-delta system.

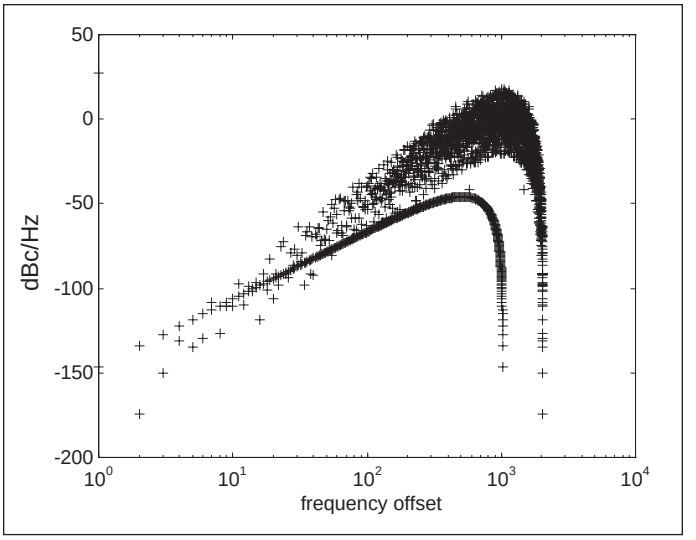
For input K=1, truncation = 4 bits such that the fractionality $K/F = 1/2^4 = 0.0625$. However, this is an average, because the sequence is now very long (pseudo random because it is deterministic but with a huge periodicity; the accumulators can be very large) with an average of 1/16.

Sample of the output sequence: 0 1 –1 0 1 –1 1 2 –2 1 –1 1 0 1 0 –1 2 –2 3 –2 2 1 –1 0 ...

This example assumes each accumulator starts in the all-zeros state. For the third order loop, other sequences are possible, depending on the state of each accumulator. We have noticed that this affects the output spurious for a given input value. Also, performance is affected



■ **Figure 2. Theoretical first, second, third order sigma-delta modulator.**



■ **Figure 3. Simulated third order sigma-delta modulator.**

depending on the lowest bit engaged in the input. For example, an input of 32 (10000 binary) would not benefit from the effect of having the frequencies spread over the least significant 4 bits as would an input of, say, 33 (10001 binary), since these inputs are accumulated (see example below). To ensure "longevity," the LSB bit is always activated. The effect will be the creation of a very long sequence, almost "random," eliminating initial condition effects with high pass characteristics and the average of K/F.

Hz offset from carrier	L(fm) in –dBc/Hz
10	70
100	70
1000	80
10k	110
100k	132
1M	147

■ **Table 1. Measured phase noise of the PLL from HP, at 500-1000 MHz. Reference frequency is 200 kHz; the 200 kHz spur is attenuated more than –90 dBc.**

This can create a frequency error of $F_r/2^L$, where L is the size of the accumulator. For L=32 bits, the frequency error for F_r=1 MHz is .023 MHz, which is also the resolution of the synthesizer. Note that most numbers, and especially 2 and 3, are followed by a negative value, intuitively showing "high pass" characteristics.

10000 + 10000 + 10000 + 10000 + ... —> 32, 64, 96, 128, 160, 192, 224, 0, 32, 64, 128, etc.

vs.

10001 + 10001 + 10001 + 10001 + ... —> 33, 66, 99, 132, 165, 198, 231, 8, 41, 74, 107, etc.

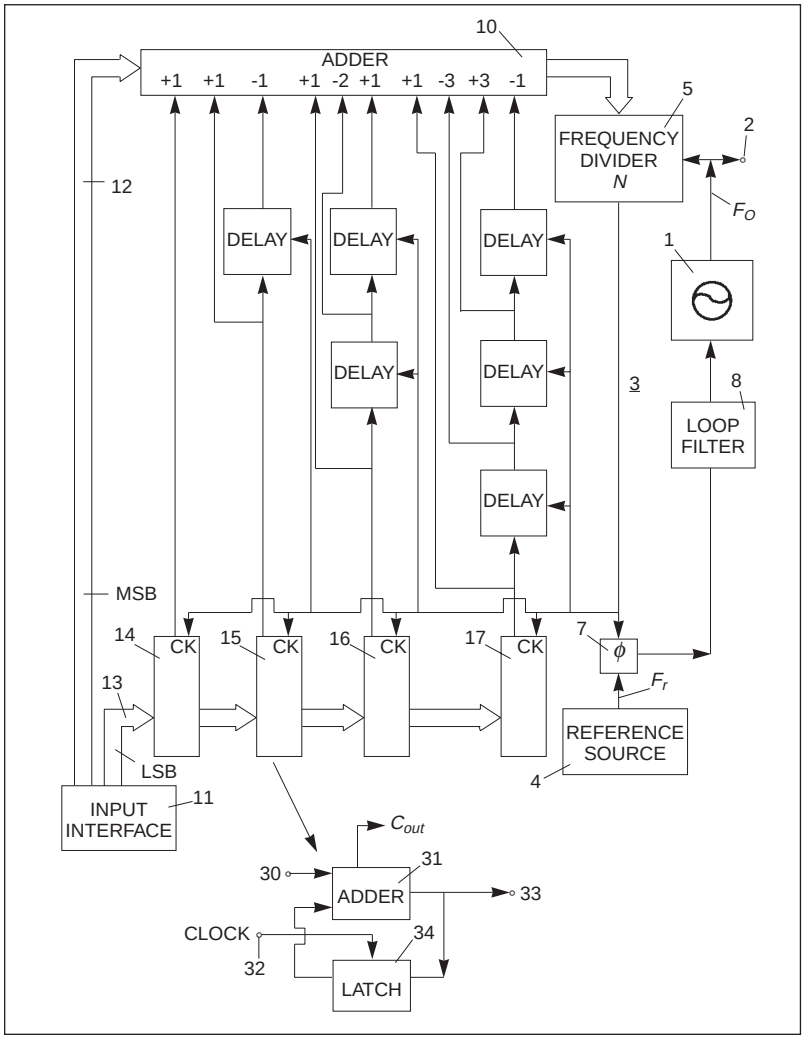
Performance

1) The Sciteq 1618 (first order) is implemented with an equivalent first order sigma delta modulator. General performance:

- Single chip fractional PLL, using CMOS technology.
- Input speed: F_r, F_v => 100 MHz, 3-5 VDC power supply.
- Reference divider: 5 bits.
- Fractional level: Programmable from 0 (no fractional) up to F=64.
- Phase detector noise floor for F_r=1 MHz, better than –155 dBC/Hz.
- Power: 5V @19 mA, 3V @ 12mA.
- Usual implementation uses external 16/17 or 32/33 dual modulus. Practical resolution is above 25 kHz.

2) The HP ADF has been described in detail in Reference 4. Phase noise performance close to carrier, in loop bandwidth of 2 kHz, is approximately –140 dBc/Hz. Resolution: <.012 Hz. Device uses external dual modulus 32/33. See Table 1 for performance.

3) Marconi of the UK, a pioneer of this technology (and a winner of the Queen's award for this invention), has developed a similar technique approximating the process as shown in Figure 4. The alternate ±1, ±2, ±3



■ **Figure 4. Diagram of the Marconi all-digital fractional chip from [8].**

approximates the "high pass" behavior. Details of ASIC performance are not known to us at this time. (Also see the comparison of 1, 2, 3 modulator waveforms in Figure 5.)

Conclusion

PLL technology is evolving in two directions. One is mainly in IC techology, allowing better integration, functionality, voltage and power. The other is the integration of PLL with DSP, resulting in advanced fractional-*N* solutions that allow better phase noise performance and improved switching speed. Fractional-*N* technology has very modest presence in the PLL universe, but this will probably change in the near future. F*N* requires only modest increase in complexity and therefore allows significant improvement at a very marginal increase in cost.

All-digital fractional-*N* requires theoretical work and ASIC development to achieve manufacturing level and maturity. We expect this to happen within the next 3-5 years. Additional focus will be on switching speed as fast hopping becomes a networking and diversity technology, and of course the continuous lowering of operating voltage and current. RF engineering now requires good basic knowledge of DSP. These are exciting and interesting challenges for design engineers and another level of evolution in wireless communications. ■

References

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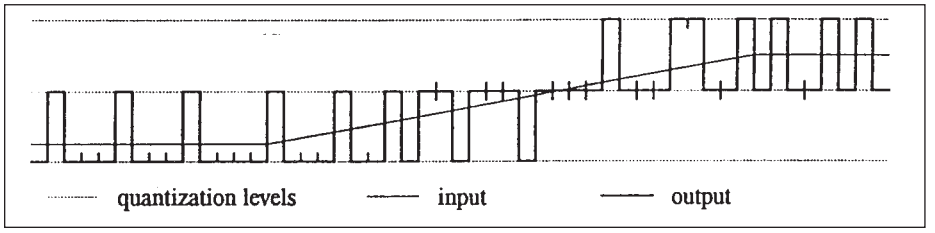

■ **Figure 5. Generating "smooth" analog signals by high speed digital approximation.**

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