

# Fast, Flexible DSP Raises Wireless Base Station Performance

**TMS320C6x series devices offer 1600 MIPS power for optimized performance in wireless applications**

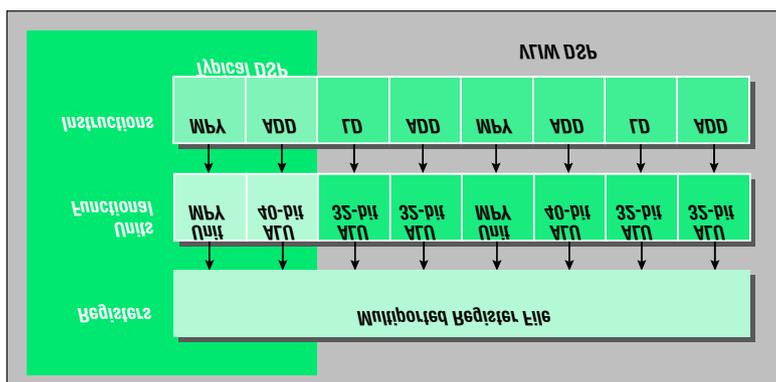
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The success of the wireless telephone industry depends as much on effective base station design as it does on design of the telephone handsets themselves. Many requirements that affect handsets also affect base stations: standards, algorithms, power consumption, even size. Just as handsets continually pack more performance into smaller spaces, so do base stations.

Traditional wireless cells measure several kilometers in diameter, so that base station transmitters must be large and powerful, with systems in sheds or even larger buildings. The increased use of digital cellular and Personal Communications Systems (PCS) standards will encourage the innovation of much smaller future cells, perhaps covering no more than a factory floor or a shopping mall. For these digital "picostations" of the not-too-distant future, transmission power requirements will not be as great as for the larger analog macro-cellular systems, but data processing requirements will be much higher. (See sidebar "How DSPs optimize base station solutions" on the next page.) Moreover, these smaller wireless cells will bring many new applications, such as their use as access mechanisms for wireless PBXs, so that base station IC solutions will have to offer design flexibility along with high performance.

## A DSP for base stations

TI's new TMS320C6201 Digital Signal Processor (DSP) offers the combined flexibility and performance required to meet the design



■ Figure 1. VelociTI Advanced VLIW architecture.

requirements of multichannel next-generation wireless base stations, including the compact picostations envisioned for future small-area applications. The 'C6201 is the first member of a new family of high-performance fixed-point DSPs, the TMS320C6x series. The new device offers the highest performance of any general-purpose programmable DSP available today, processing up to 1600 MIPS — ten times the performance of previous DSPs. Along with its speed, the 'C6201 provides an efficient C compiler that minimizes the need to hand-code in assembly, saving development time and providing programming flexibility.

The 200-MHz fixed-point 'C6201 is the first processor based on the VelociTI(tm) Advanced Very Long Instruction Word (VLIW) architecture, illustrated in Figure 1. With two multipliers and six arithmetic units, the architecture provides a cost-effective means of dealing with the parallelism inherent in many DSP communications algorithms. By packing up to eight 32-bit instructions into parallel execution units in each 5-ns cycle, the architecture reduces code

size, program fetches and power consumption. All instructions are conditional, minimizing branching for higher sustained performance.

The efficiency of the VelociTI architecture is illustrated by its speed of execution on algorithms frequently used in communications. Multiply-accumulate operations (MACs) can be accomplished 400 million times per second, and a 1024-point Fast Fourier Transform (FFT) requires only 70 ns. Such high performance lets designers pack more channels into existing base stations, or shrink base stations to fit into much smaller equipment. Design studies indicate that a 'C6201 can implement 30 GSM voice channels at \$3 per channel in a wireless base station, *vs* five voice channels at \$7 per channel with previous DSPs.

The streamlined architecture allows the 'C6201 to be implemented in only 550,000 logic transistors, providing a tremendous processing throughput for a relatively small die size. The device is designed using a 0.25-micron CMOS process technology, which is very thrifty in power consumption for cool operation.

### A programming shift from assembly to C

The 'C6x C compiler generates code that executes on the highly independent functional units, with three times the efficiency of existing fixed-point DSP compilers. A code optimizer pinpoints the code that will yield the greatest gain in efficiency through rewriting, helping developers conserve resources and reduce time to market. The architecture provides saturation and normalization; scalable 8-, 16- and 32-bit data support; bit field manipulation and instructions for extracting, setting, clearing and counting bits; and support for 40-bit arithmetic options for extra precision in vocoders and other computationally intensive applications.

In the past, DSP developers have had to maximize software performance by hand-crafting assembly code. The efficiency of the 'C6x software tools allows software engineers to code in high-level C code, without worrying about the mechanics of the underlying processor. The shift in programming from assembly to C can cut development time drastically, opening up product development to a wide pool of experienced C programmers who

### How DSPs optimize base station solutions

Wireless base stations consist of two major systems, as shown in the accompanying functional block diagram. The transceiver, located at the antenna, provides the send and receive functions. The transcoder provides speech processing and typically serves several transceivers (though this physical separation may not apply in future small-area applications served by picostations).

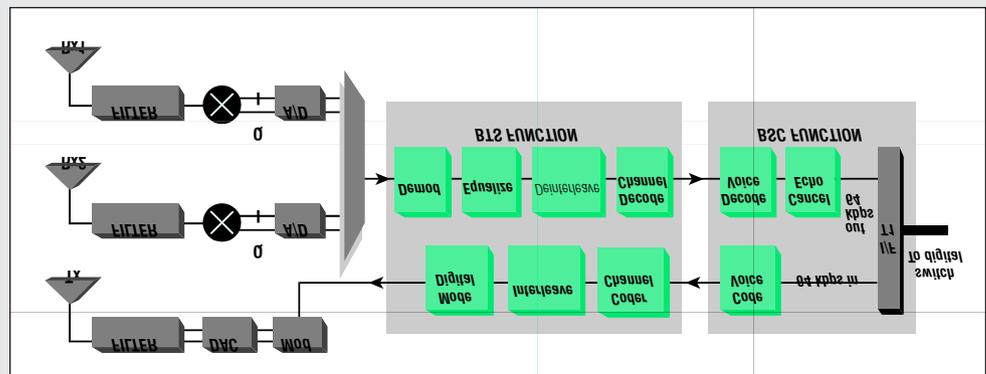
In the transcoder, where analog speech input is converted to digital data, the voice encoder compresses speech from a 64-kbps sample rate for transmission at 30 kbps or less, including as much as 50 percent overhead. On the return path, the voice decoder decompresses speech, while echo cancellation removes reflected sound from the source (acoustic echoes) and reflected line signals (line echoes).

In a TDMA transceiver, the channel encoder multiplexes encoded speech into time slots and adds forward error correction (FEC) to the data stream. The interleaver shuffles the bits within the slot so that transmission burst errors cannot destroy all the data in a brief time period. Digital modulation codes the bit streams as symbols. In reception, the transceiver reverses these processes and also compares the signal against an included known bit stream pattern to equalize the length of bits and interbit spreads, minimizing the effects of multipath transmission interference.

As these functions clearly show, both the transceiver

and transcoder handle large volumes of digital data in real time. The real-time processing that is required for multiple channels is beyond the capacity of general-purpose CPUs at reasonable costs. Custom hardware can be designed to perform the individual functions, but this approach is redundant, since many of the same hardware structures must be built over and over again for each function.

A DSP eliminates this redundancy and at the same time provides programming flexibility, allowing designers to change the operation of the system as standards evolve and algorithms improve. A DSP also simplifies modification of a system to support other standards, since many of the changes are in software. With its 1600 MIPS of performance, the TMS320C6201 provides the processing power needed by multichannel wireless base stations. At the same time, the 'C6201's highly efficient C compiler allows designers to take advantage of this performance with the full flexibility and rapid development of high-level programming.



■ Figure 3. Block diagram of wireless base station, showing where DSP-implemented functions are located in the signal path.

