Hybrid Frequency Synthesizer Combines Octave Tuning Range and Millihertz Steps

DDS and PLL techniques are combined in this high-resolution synthesizer

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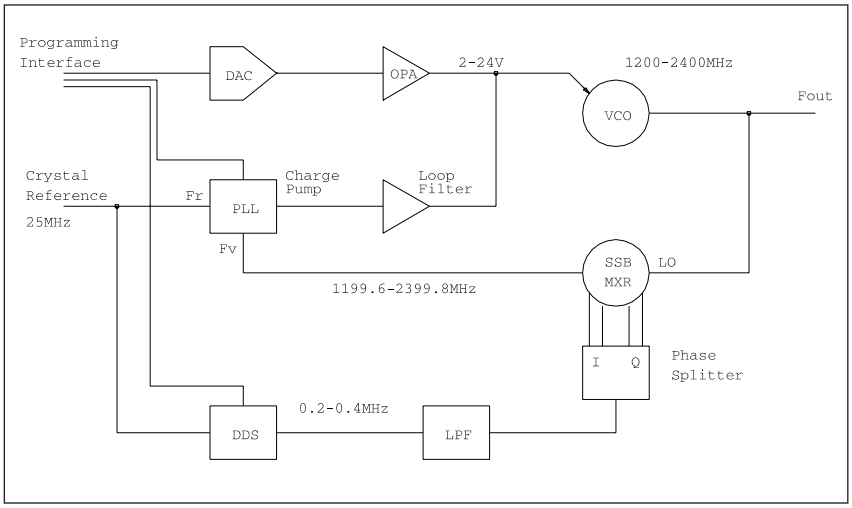
Microwave synthesizers with wide tuning ranges and fine tuning steps are found in applications including RF signal generators, spectrum analyzers, communication transceivers, surveillance receivers and TV/CATV monitoring and test equipment. The advance of semiconductor technology has simplified the design of these microwave frequency synthesizers while reducing the cost, size and complexity. This article describes a simple implementation of such a synthesizer which delivers good phase noise and spurious performance along with an octave tuning range and fine tuning steps.



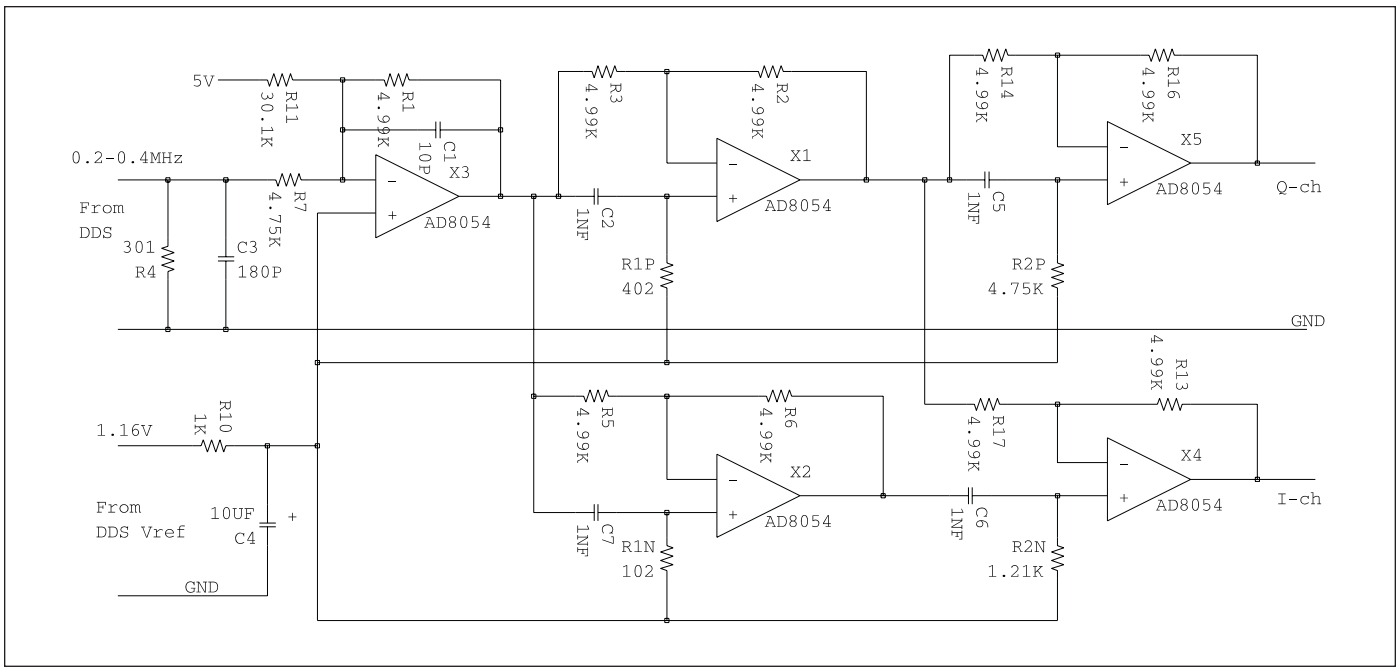
▲ **Figure 1. Frequency synthesizer block diagram.**

Hybrid phase-locked loop overview

Figure 1 shows the block diagram of a microwave synthesizer consisting of a phase-locked loop with an octave-tuning voltage-controlled oscillator (VCO), a single-sideband (SSB) mixer and a direct-digital synthesizer (DDS). Support circuitries include a coarse-tuning digital-to-analog converter (DAC), a loop filter and a quadrature phase-splitter. Using the SSB mixer, the VCO output frequency is offset by that of the DDS before it is fed to the frequency divider of the PLL. By comparing the phase of the frequency-divided mixer output with that of a crystal-based reference and feeding back the error to correct the VCO frequency, the PLL sets the coarse frequency steps via its divider value. The DDS controls the fine tuning of the VCO. An external crystal oscillator provides the reference frequency used by both the PLL and the DDS. Detailed operation of the PLL can be found in several texts [1-4].

Frequency planning

The synthesizer presented here is intended to be used in both a 2.4 GHz RF signal generator and a 1 GHz spectrum analyzer. The VCO, and hence the synthesizer, will be tuned over the range of 1.2 - 2.4 GHz. The DDS generates a signal from 0.2 - 0.4 MHz, which is lowpass filtered to produce the offset frequency in millihertz steps. This offset frequency then goes through a quadrature phase-splitter to modulate a sample of the VCO output using the quadrature modulator. The resultant signal is then fed to the PLL



▲ **Figure 2. DDS lowpass filter and phase splitter schematic.**

chip, where the former gets divided by the fractional ratio of 1199.6 to 2399.8 before phase-comparison with the frequency-divided crystal reference. The phase-comparison frequency of 1 MHz is the highest usable by the commercially available single-chip PLL synthesizer device, due to its use of a divide-by 32/33 dual modulus prescaler.

Building blocks

VCO — The VCO selected for this project is model V6009001 from Z-Communications [5], since it is the only commercially available 1.2 - 2.4 GHz VCO that was found. It requires 55 mA at a supply voltage of 15 V and a tuning voltage range of 2 - 24 V to cover the whole frequency range. The phase noise is rated at a very respectable –100 dBc/Hz at 10 kHz offset, which is very good for a VCO given the tuning ratio and operating frequency. A note of caution: This VCO is sensitive to output loading and it can stop oscillating when the tuning voltage runs below 1.8 V. The measured tuning sensitivity (K_V) varies between 80 to 40 MHz/V over its frequency range, and the phase noise measured on the bench using the HP8562E is –96 dBc/Hz at 10 kHz offset. The VCO provides plenty of signal power (+15 to +19 dBm), hence the output is resistively tapped to provide a signal for the phase-locked loop.

Direct-digital synthesizer (DDS) — The DDS chip used in this project is the AD9832 from Analog Devices [6], running at a clock frequency of 25 MHz with 32-bit frequency resolution. The output frequency is given by the following equation:

$$F_{DDS} = F_{CLK} \times N_{FRQ} / 2^{32}$$

where F_{DDS} is the DDS output frequency, F_{CLK} is the DDS clock frequency and N_{FRQ} is the value programmed into the DDS chip's Frequency Register.

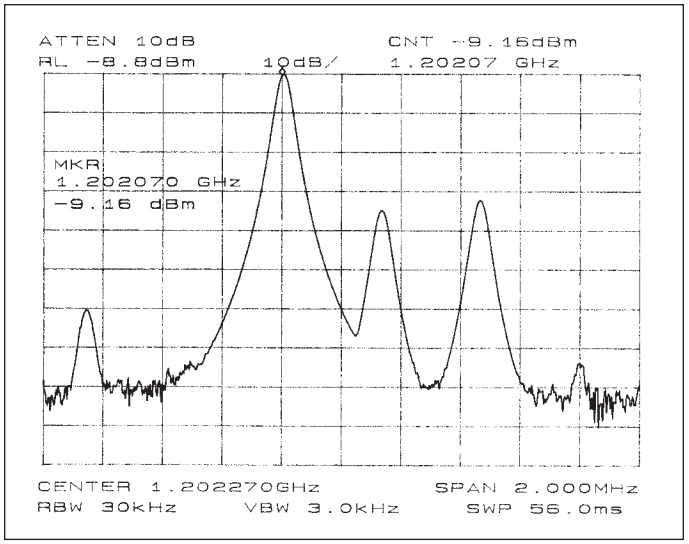
The resultant frequency increment is given by

$$F_{CLK} / 2^{32} = 25 \text{ MHz} / 2^{32}$$
$$= 5.821 \text{ millihertz}$$

For the output frequency range of 0.2 - 0.4 MHz, the highest sidebands observed were less than –75 dBc. The output of the DDS is lowpass filtered to remove the alias components due to sampling by the reference clock, and DC offset is set to 1.2 V as required later by the quadrature modulator.

Phase-splitter and single-sideband (SSB) mixer — The SSB mixer is formed with a phase splitter along with a quadrature modulator. The phase splitter contains two branches of all-pass networks that create a phase difference of 90 degrees over the DDS frequency range (Figure 2). The design of such phase splitters is described by Willams and Teylor [7]. Following the procedures from this reference, a 4-section network is selected to provide a quadrature error of 1.31 degree peak over the upper to lower frequency ratio of 11.47. The Frequency Scaling Factor (FSF) is given by

$$\text{FSF} = 2\pi \times (F_{lower} \times F_{upper})^{1/2}$$
$$= 2\pi \times [(0.2 \times 0.4) \times 10^6]^{1/2}$$
$$= 7.10 \times 10^6 \text{ rad/s}$$



▲ **Figure 3. SSB mixer output spectrum.**

The resistor values are computed by picking C = 1000 pF and substituting in the formula

$$R_{xx} = 1 / (\alpha_{xx} \times \text{FSF} \times \text{C})$$

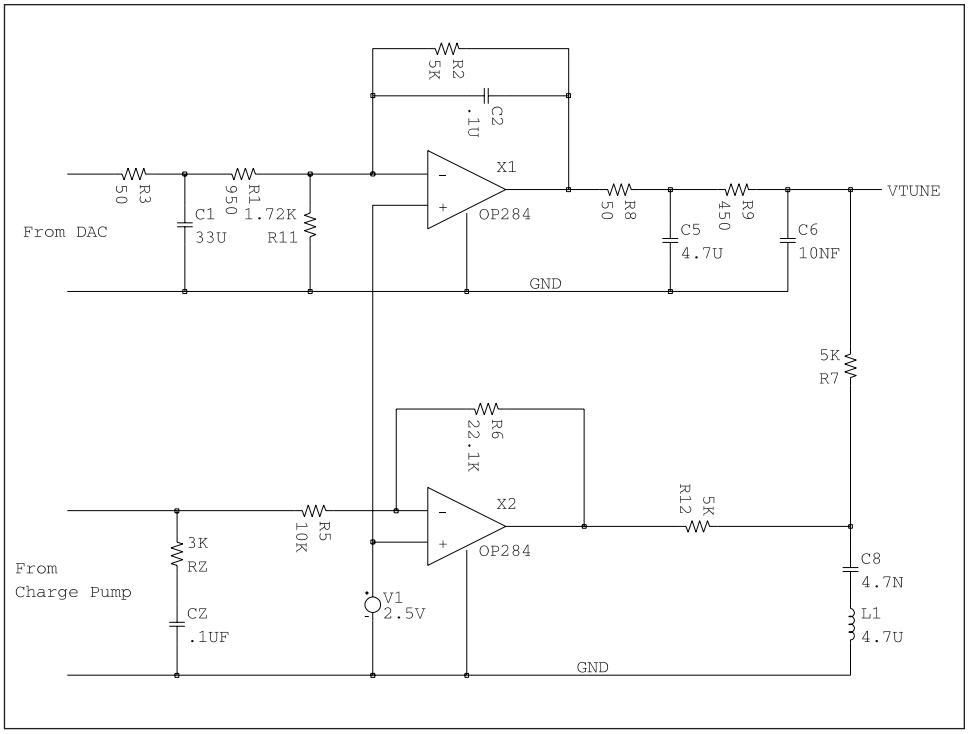
where R_{xx} are the resistor values for the appropriate sections and α_{xx} are the normalized pole values.

Section	α_N	α_P	R_N	R_P
1	5.9939	1.5027	102	402
2	0.5055	0.1280	1.21k	4.75k

The DC reference level of the phase splitter is set to 1.16 V using the DDS's on-chip reference to match that of the filtered DDS output. An additional inverting amplifier provides the required complimentary base-

band signals for the quadrature modulator that follows. The phase noise of the DDS signal at the phase splitter outputs is measured to be –116 dBc/Hz at 10 kHz offset.

The quadrature modulator used is the AD8346 from Analog Devices [8], which can operate through the frequency range of 0.8 - 2.5 GHz. The baseband signals from the phase splitter are modulated onto the LO signal coming from the VCO. The desired lower sideband (LSB) output at the difference frequency is sent to the fractional-N PLL synthesizer chip. Also present in this output are the LO leakage at the VCO frequency and the unwanted sideband (USB) at the sum of the VCO and DDS frequencies, along with other intermodulation products. Figure 3 is the modulator's output spectrum, showing the LO leakage and USB at around 35 dB below the desired LSB signal. These unwanted signals will ultimately show up as additional tones modulating the VCO, and must be rejected by the loop filter.



▲ **Figure 4. Loop filter and coarse tuning circuit schematic.**

Fractional-N PLL — The National Semiconductor LMX2350 2.5 GHz single-chip fractional-N PLL synthesizer has been selected for its flexibilibity and availability [9]. There are two synthesizer on the same chip, though the 550 MHz IF synthesizer section is not be used in this project. The LMX2350 contains registers to store values for the various reference and variable frequency dividers.

Coarse tuning — A digital-to-analog converter (DAC), Analog Devices' DAC8512 [10], is used to set the coarse tuning voltage for the VCO. The 0 - 4 V output

from the DAC is low-pass filtered, offset, amplified and heavily filtered again to cover the 2 - 22 V tuning voltage range as shown in Figure 4. The PLL will only need to correct for a small frequency error of the order of ±5 MHz, thus the required tuning sensitivity is lowered along with its noise implications for the PLL. However, it still takes some very careful design and layout to minimize the amount of hum and unwanted signals presented to the VCO's tuning input.

Loop filter design — The loop bandwidth (LBW) of the PLL is chosen to optimize the phase noise performance of the loop. The multiplied reference noise is computed from

$$\boldsymbol{L}(f) = 20 \times \log(N_{div}) + N_D$$

where N_{div} is the divide ratio in the PLL, and N_D is the noise floor of the PLL chip, assumed to be –160 dBc/Hz (unconfirmed).

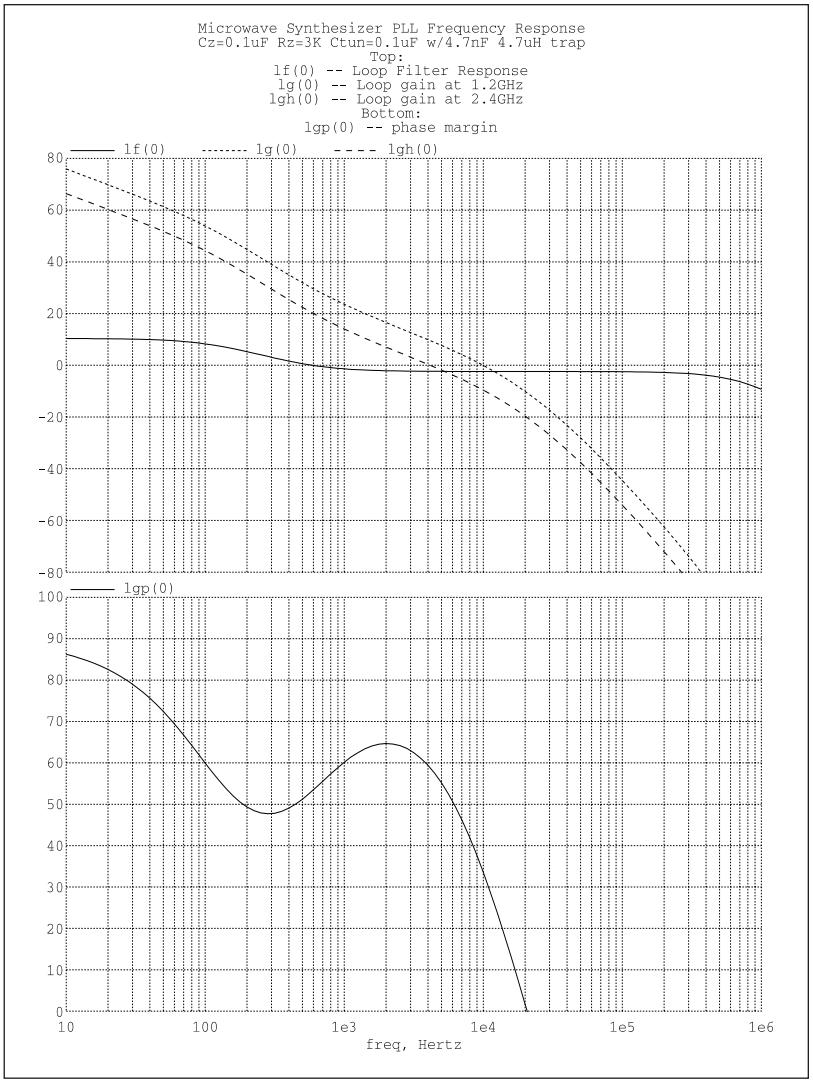
The contribution by the crystal reference is assumed to be negligible after being divided by the Reference Divider. With N_{div} varying from 1200 to 2400, $\boldsymbol{L}(f)$ lies between –98 to –92 dBc/Hz accordingly. With N_{div} = 1200, the VCO's phase noise will be equal to that of the multiplied reference at an offset frequency of 8 kHz. If the loop bandwidth is set also to the same frequency, then the resultant phase noise of the PLL will track that of the reference for offset frequencies below 8 kHz and that of the VCO above 8 kHz, getting the best of both worlds.

The VCO The procedure for designing the loop filter for a phase-locked loop can be found in many texts, such as Gardner [1]. The loop gain is given by

$$LG(s) = K_P \times K_V \times H(s) / (s \times N_{div})$$

where K_P is the phase detection constant, K_V the VCO tuning sensitivity, and $H(s)$ is the transfer function of the loop filter.

In this case the pole of the loop filter (formed by R_5 and C_z) and the zero of the loop filter (formed by R_z and C_z), are selected to obtain a frequency response where the loop gain crosses the unity line at 8 kHz and at a slope of –20 dB/decade to ensure stability.



▲ **Figure 5. Loop gain and loop filter response.**

The loop filter output is then resistively summed with the coarse tuning voltage. The overall response of the loop gain and that of the loop filter (from the charge pump output to the VCO's tuning input) is shown in Figure 5.

Programming interface — Programming of the PLL's frequency is through a PC parallel port into the serial interfaces of the different sections. Since each of the three devices, DDS, DAC and PLL, uses a three wire serial interface, the Clock and Data lines are shared, and each Latch Enable input is driven by a separate bit from the PC's parallel port.

Source	Frequency Offset	Level	Comment
DDS	anywhere	~ -72 dBc	Unfilterable
Phase Detector Reference	1 MHz	~ -70 dBc	Isolation limited
SSB Mixer (LO & USB)	0.2-0.8 MHz	~ -50 dBc	Isolation + Filter
Crystal Oscillator	25 MHz	~ -50 dBc	Isolation limited

▲ **Table 1. A list of the sources that contribute to spurious sidebands.**

Performance analysis

Phase noise — At offsets less than the PLL's loop bandwidth, phase

noise is dominated by the reference divider noise floor (~–160 dBc) + 20 log(N_{div}), where N_{div} is the divide ratio (1199.6 - 2399.8), which gives –98 to –92 dBc/Hz. Phase noise outside the loop bandwidth is set by the VCO and its tuning circuitry.

The phase noise of a breadboard prototype version of the frequency synthesizer is shown in Figure 6. With –76 dBc/Hz at 10 kHz offset, the synthesizer is far from obtaining its potential of –92 to –98 dBc/Hz level. Most of this excess noise can be attributed to inadequate power supply and voltage reference conditioning, so that broadband noise is coupled into the VCO. (Frequency synthesizer designers are known to use the largest quantity of tantalum capacitors per unit area on the printed circuit, in addition to the heavy metal armor around the circuitry). At an offset of 100 kHz, the phase noise finally comes back down to –116 dBc/Hz, which is close to the performance of the VCO alone.

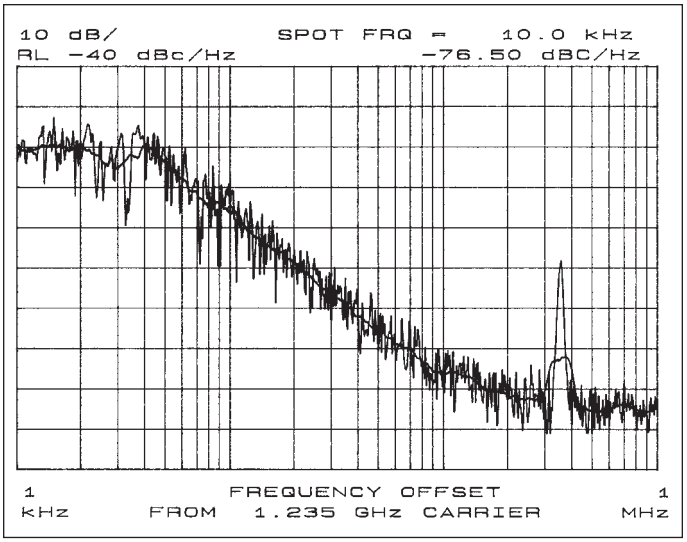
Spurious sideband levels — There are several contributors to spurious sidebands. The sources and the results measured on the prototype breadboard circuit are listed in Table 1.

The DDS generates low level spurious sidebands all over its spectrum. Those that fall inside or close to the loop bandwidth cannot be filtered off. Fortunately, by running the DDS output at a small fraction of its clock frequency, these spurious signals are kept to a low level. The Phase Detector Reference sideband is trapped in the loop filter, and only shows up due to the limited isolation on the breadboard. The SSB Mixer spurs require a more careful design of the loop filter as they fall closer to the loop bandwidth and they suffer from the lack of isolation due to the construction of the breadboard. The 25 MHz crystal reference is present all over the breadboard and, like the two previous sources, it needs a better layout to provide the necessary isolation.

Frequency settling time — Frequency settling time is mostly limited by the requirement to adequately filter the SSB mixer spurs and fractional-N jitter with offsets from 0.2 to 0.8 MHz, and also by the fact that the coarse tuning output needs to be heavily filtered. The performance on the breadboard was severely hampered as the coarse tuning path does not have any means to reduce the filtering during a frequency change.

Conclusion

The microwave synthesizer presented above demonstrates the simplicity of the design. The whole synthesizer can be built from readily available components, and the resultant printed circuit board can fit in the palm of a hand. In order to reach



▲ **Figure 6. Synthesizer phase noise plot.**

the full potential in phase noise, spurious level and switching performance, greater attention must be given to the details of a careful layout and power supply conditioning. ■

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