A Suppressed Harmonic Power Detector for Dual Band Phones

A novel design allows a single detector to be used at different frequencies

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This article discusses a novel detector for power control loops. Its design combines circuitry to suppress the second harmonics generated at the input with provisions for temperature compensation.

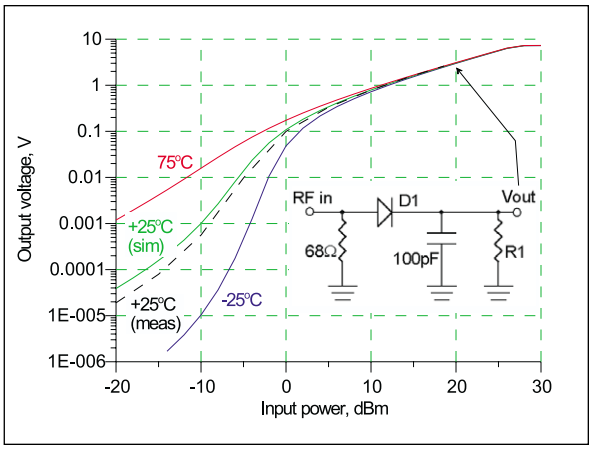
The problem

The increase in demand for dual band mobile phones for use on GSM900 and GSM1800 or GSM1900 systems has given designers a considerable challenge — how to fit the additional circuitry required into the same or smaller space as the existing single band phones. The RF output power monitoring part of the power control loop is one area where designers would like to save space. In a single band phone, this is often designed with a directional coupler, either a printed or a surface mount component, and the detector normally based around a temperature compensated Schottky circuit [1].

For a dual band phone, the coupler ideally would be placed in the path to the antenna. However, this would not increase the component count needed. Unfortunately, a conventional detector circuit generates harmonics of the fundamental frequency. This is normally not a problem in a single band phone, as there is sufficient low pass filtering between the coupler and the antenna.

In a dual band phone, however, the same antenna is used for both bands, and therefore no low pass filtering is possible. This means that the second harmonic generated by the detector when the phone is operating in the GSM900 band does not get attenuated and the phone design fails the spurious emission regulations.

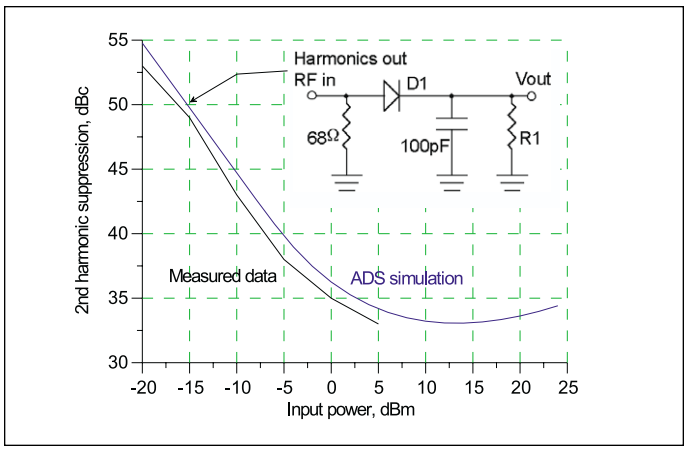
One way to combat this problem is to provide a separate coupler after each PA and use two independent detectors. This can be done with the HSMS-282L, which has the advantage of having three Schottky diodes in one SOT363 package, two for the detectors and one common reference diode for temperature compensation. The penalty for this solution is the space required by and the cost of the additional coupler. A better method would be to have a detector design that does not produce high levels of harmonics or that suppresses them.



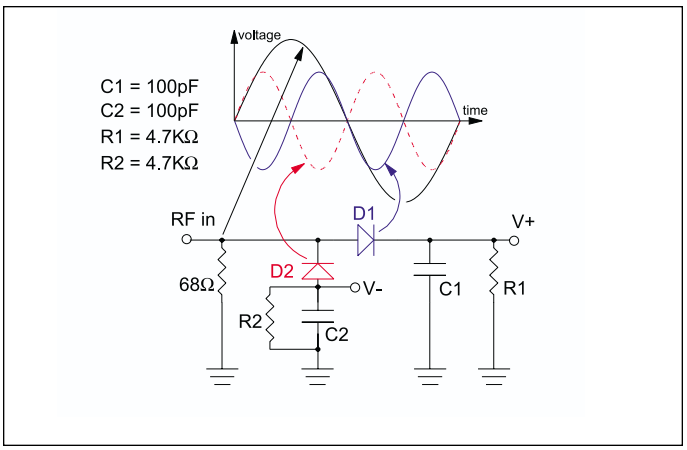
▲ **Figure 1. The temperature dependent transfer curve exhibited by the conventional single-diode detector.**

The solution

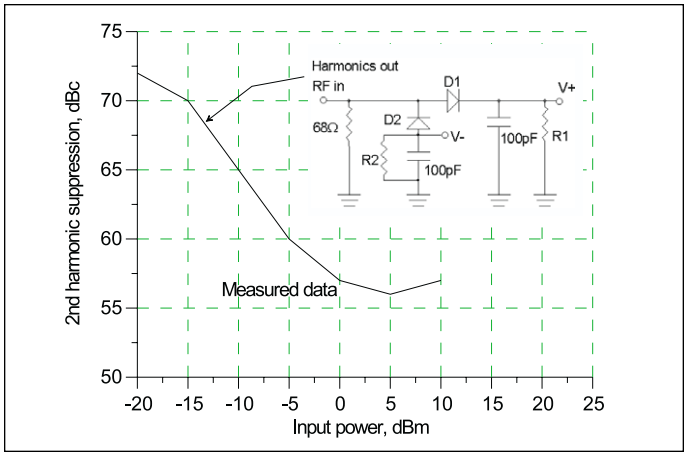
The conventional single-diode detector [2] exhibits the temperature-dependent transfer curve shown in Figure 1. At the input of the circuit, harmonics are generated by the Schottky diode (such devices are used in frequency multipliers). The level of the second harmonic is given in Figure 2, where a harmonic balance



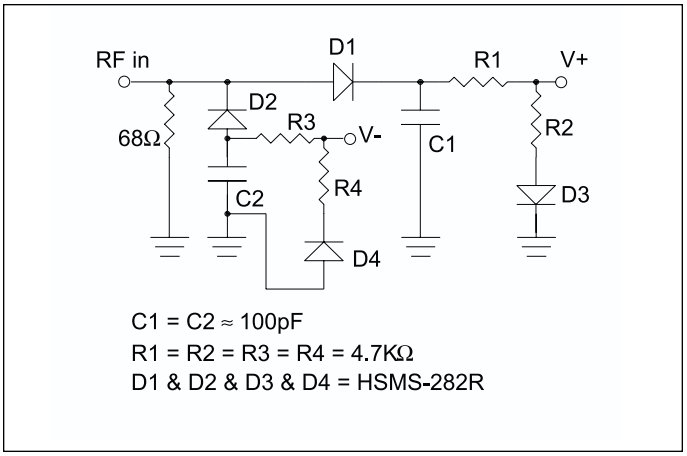
▲ **Figure 2. The level of the second harmonic where the harmonic balance simulation is compared to measured data.**



▲ **Figure 3. The addition of a second diode with an associated bypass capacitor and load resistor.**



▲ **Figure 4. The measured harmonic suppression obtained from the experimental circuit.**



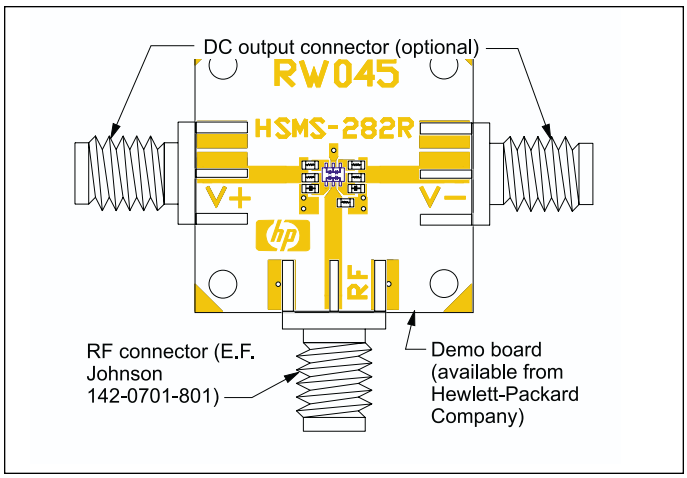
▲ **Figure 5. A temperature-compensated version of the detector.**

simulation (using ADS [3]) is compared to measured data. Second harmonic levels are given in dBc, relative to the 900 MHz input signal. R1, the load resistance, was 4.7 kohms in both cases. Note the good agreement, despite the fact that the test equipment used in our lab limited the available input power to +5 dBm. Worse case harmonic levels are 32 dBc at an input power level of +10 dBm (measured at the input to the detector). This level is sufficiently high, causing the phone to fail spurious emissions tests.

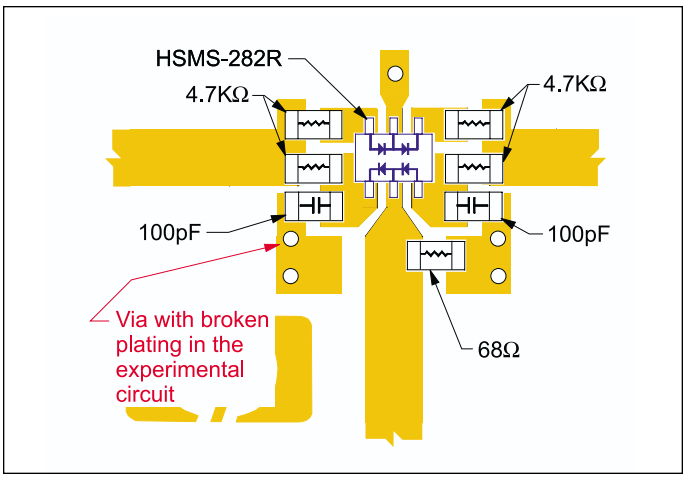
One can suppress the second (and all other even-order) harmonics through the addition of a second diode with an associated bypass capacitor and load resistor, as shown in Figure 3. The second diode (D2) is connected in anti-parallel to the detector diode in the RF circuit, creating a second harmonic out of phase with that created by D1. In theory, this cancellation is ideal (zero second harmonic voltage) if D1 and D2 are perfectly matched to each other (along with R1 and R2), and if the circuit parasitics (ground via inductances, etc.) are equal in both sides of the RF circuit. If an unbalanced output (V+) is used, the transfer curve of this detector will be identical to that shown in Figure 1 for the single diode detector. If a balanced output is used (V+ compared to V-), the output voltages will be twice that shown in Figure 1.

Measurements were made on such a circuit, built around the HSMS-282C matched pair of Schottky diodes and chosen for best matching of diode characteristics [4]. The measured second harmonic suppression obtained from the experimental circuit is shown in Figure 4. The suppression is not as ideal as predicted, because of small differences in the two diodes as well as approximately 0.3 nH of extra via hole inductance in the D1 side of the circuit. Better attention to detail in the layout of the detector board will result in some improvement over the data given in Figure 4.

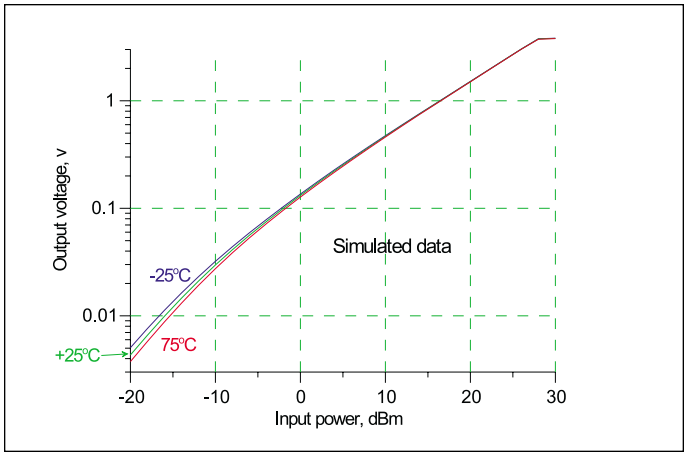
While not infinite, the 55 dBc second harmonic suppression of this circuit, along with the additional coupling loss of the directional coupler, is sufficient to



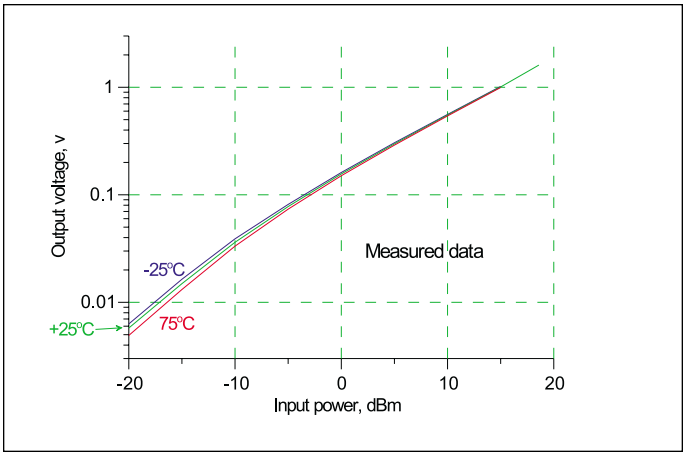
▲ **Figure 6. Assembly drawing of the experimental circuit.**



▲ **Figure 7. Assembly drawing of the experimental circuit.**



▲ **Figure 8. Simulated output voltage over temperature.**



▲ **Figure 9. Measured data for the experimental circuit.**

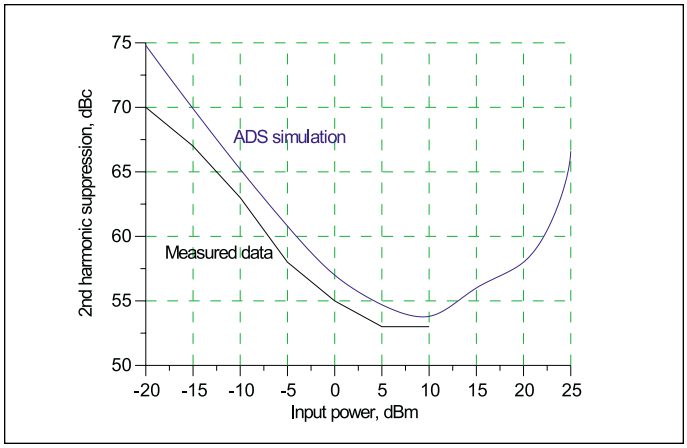
enable a phone that is using it to meet spurious emission regulations. However, the variation of output voltage over temperature is unacceptable.

Temperature compensation of this suppressed harmonic detector can be achieved by applying the techniques described in [1]. This circuit is shown in Figure 5. Reference [1] provides details on how R1, R2 and D3 act as a temperature-sensitive variable voltage divider to compensate for the temperature variation of D1's output. D4 and its associated resistors provide a similar function for the harmonic suppression diode (D2). As was the case with the earlier circuit, an unbalanced output can be taken from port V+ (compared to ground), or a balanced output can be taken from V+ compared to V–. Because the series resistance of R2 + D3 can be very high at cold temperatures, V+ and V– must be fed into an amplifier with an input impedance in excess of 10^9 ohms.

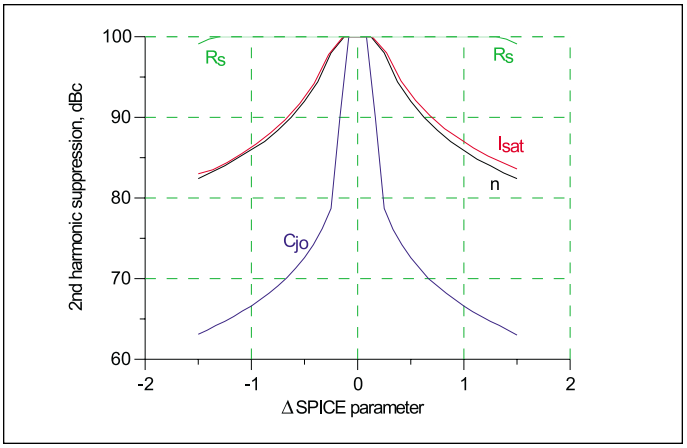
Such a circuit requires that D1 and D2 be as perfectly matched as possible, along with D3 and D4. This can be accomplished with two HSMS-282C pairs, but a single HSMS-282R quad uses less board space. This can be seen in the assembly drawing of the experimental circuit, shown in Figures 6 and 7.

This circuit was simulated and the experimental circuit was tested. Simulated output voltage over temperature is given in Figure 8 and measured data is provided in Figure 9. Note that limitations in our test equipment did not permit us to test the circuit at power levels over +18 dBm. It should also be noted that input power levels in excess of +25 dBm may drive the detector diode into reverse break-down, severely reducing its reliability. Test data very closely tracks the harmonic balance simulation, and stability over temperature is excellent.

Simulated and measured harmonic performance of the combined circuit is given in Figure 10. In setting up the simulation, the values of four key SPICE parameters (n, I_{sat}, R_{series} and C_{jo}) for D2 were offset from those of D1 by 1σ (see reference [4]). In addition, 0.3 nH of via hole inductance was added to the RF circuit between C2 and ground to represent the circuit imbalance created by broken plating in a via hole. Agreement with measured data was fairly good.



▲ **Figure 10. Simulated and measured harmonic performance of the combined circuit.**



▲ **Figure 11. Results of simulations performed to determine which of the four SPICE paramters had the largest effect upon second harmonic suppression.**

Effect of varying SPICE parameters

Additional simulations were performed to determine which of the four SPICE parameters had the largest effect upon second harmonic suppression. The four parameters evaluated are n (ideality factor), I_{sat} (saturation current), R_{series} (parasitic series resistance) and C_{jo} (junction capacitance). The circuit was set to be perfectly balanced, and at one time, the SPICE parameter in D2 was varied, with the other three identical between the two diodes. Each parameter in D2 was varied $\pm 1.5\sigma$, where s (standard deviation) is obtained from the statistical data in reference [4]. The results are given in Figure 11. The variation in junction capacitance has the largest effect upon second harmonic levels, while series resistance can vary between $\pm 1.5\sigma$ with almost no effect upon harmonic performance. This illustrates the importance of using diodes, which are optimized for consistency and matched characteristics, and for which statistical data is available.

Conclusion

A circuit has been described which provides both suppression of second harmonics and temperature compensation of output voltage, using readily available surface mount components. Both harmonic balance simulation and measured data have been provided. ■

References

1. H. Eriksson and R. Waugh, "A Temperature Compensated Linear Diode Detector," to be published.

2. R. Waugh, "Designing Large-Signal Detectors for Handsets and Base Stations," *Wireless Systems Design,* Vol. 2, July 1997.

3. Hewlett-Packard, Advanced Design System.

4. R. Waugh, "A Schottky Diode Optimized for Consistency," Hewlett-Packard Design Tip D002.

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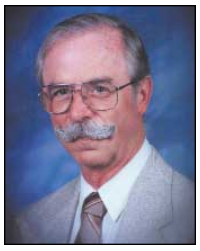

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