Frequency Properties of a Reverse Biased Thick Switching PIN Diode

A review of PIN diode behavior in a large-signal environment

By Lioudmila Drozdovskaia
Villanova University

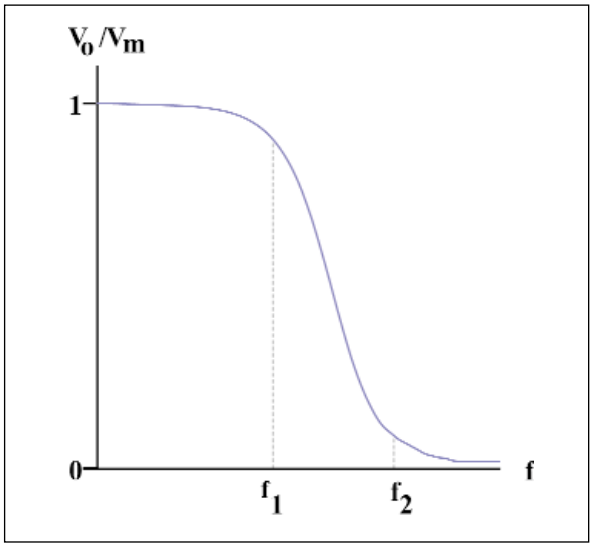
In modern wireless RF and microwave communications systems, PIN diodes and several types of transistors are used as controlled components for different control devices such as switches, attenuators, and phase-shifters [1]. In many cases, Si or GaAs PIN diodes are the devices of choice because of their good power-handling capability. Forward-biased PIN diodes exhibit low impedance; reverse biased ones exhibit high impedance and provide good bandwidth performance.

Although PIN diodes have been used widely in different applications for the last 40 years [2, 3], many of their properties are not well understood. One of these less understood properties is the reverse-biased state in a large-signal environment. The reverse-bias voltage is used to keep a high-impedance PIN diode in a low-distortion state. In this case, the PIN diode has a large RF or microwave voltage and a DC reverse-bias voltage applied to it. This DC voltage prevents any detection effects and, therefore, reduces the harmonic distortions produced by the PIN diode, especially in an RF or microwave high-power regime [2–7]. It is very important to determine correctly the required reverse DC bias voltage.

This article discusses experimental data and theoretical results of the required DC bias voltage estimated by different mathematical and physical models.

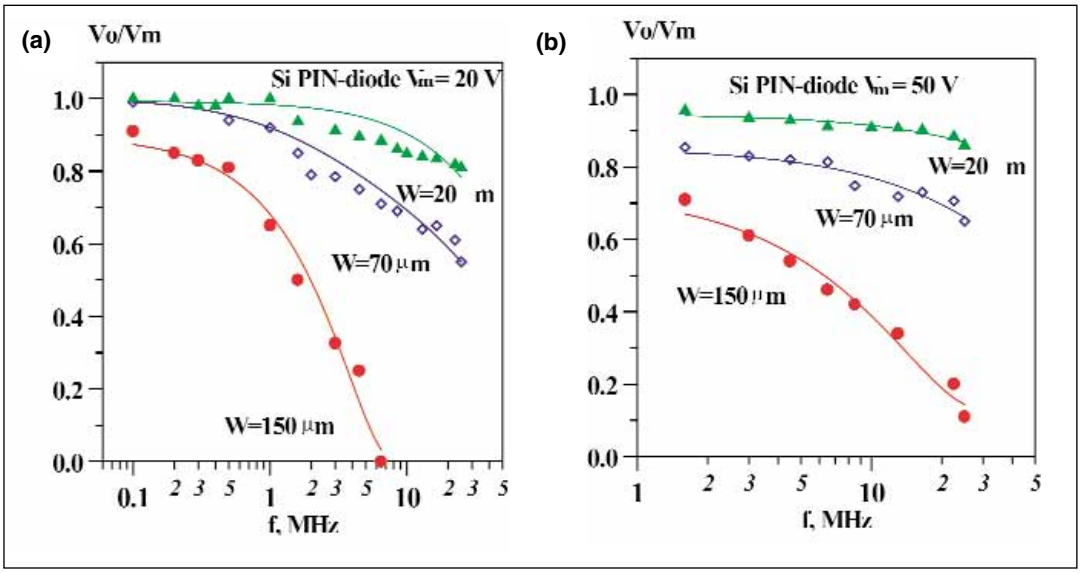
PIN diode under DC reverse-bias voltage

Experimental data [2, 3, 5, 8] has shown that the applied DC reverse-bias voltage depends on the frequency of the input RF or microwave power, as shown in Figure 1. The first area ($f < f_1$) is where the minimum required DC reverse bias voltage V_0 is the peak RF voltage across the diode V_m: $V_0 \approx V_m$. In the second area ($f > f_2$), the minimum required DC reverse bias voltage V_0 may be much smaller compared with the RF or microwave peak across the diode: $V_0 << V_m$.



▲ **Figure 1. Minimum Pin diode DC bias voltage versus frequency.**

The low-frequency area ($f < f_1$) is based on the properties of the classical detector [2, 3, 6], because the switching PIN diode behavior is similar to it. However, there are different suggestions regarding the second area ($f > f_2$). The first and simplest explanation is based on an i-region transit time of electrons and holes [2, 3, 6]. This approach may explain the reduction of the reverse DC bias voltage with the frequency increase for the short PIN diodes when the i-layer is less than the depleted region in the non-biased state (above the punch-through).



▲ **Figure 2. Required DC reverse bias voltage versus frequency for PIN diodes with different i-layer thickness. (a) V_m = 20 V; (b) V_m = 50 V.**

However, for the thick PIN diodes, where the i-layer is longer than the depleted region, this explanation is not sufficient [7, 9].

Another explanation [7, 9] is based on the multilayer impedance model [10, 11]. This model takes into account the fact that the i-region of the PIN diode below the punch-through consists of undepleted and depleted regions (for details of this model, see the Appendix). Each region can be represented [10, 11] as the shunt configuration of resistance and capacitance. The properties of the frequency-dependent impedance divider formed by these regions should be taken into account to explain the characteristic shown in Figure 1.

The depleted region resistance of the unbiased thick PIN diode is much greater than the resistance of the undepleted region. When the reverse DC voltage is applied to the PIN diode, most of it drops across the depleted region. At the same time, applied AC voltage is divided between two regions according to the properties of the frequency-dependent impedance divider [10]. At low frequencies ($f < f_1$), divider behavior is defined mainly by the depleted region resistance and the AC voltage is across the depleted region. At the high frequencies ($f > f_2$), its behavior is determined by the capacitances of both regions.

In the case of the thick PIN diode, the depleted region capacitance is greater than the undepleted one and the AC voltage is across the undepleted region at high frequencies. AC voltage applied to the depleted region causes detection effects. To prevent it, the DC reverse bias voltage is necessary. The required DC voltage value should be at least equal to the amplitude of the AC voltage applied to the depleted region. But the AC voltage across the depleted region decreases with frequency, so the required DC reverse bias voltage also drops with frequency (Figure 1). The transit time effect provides the full absence of any detection effects in PIN diode with the further frequency increase.

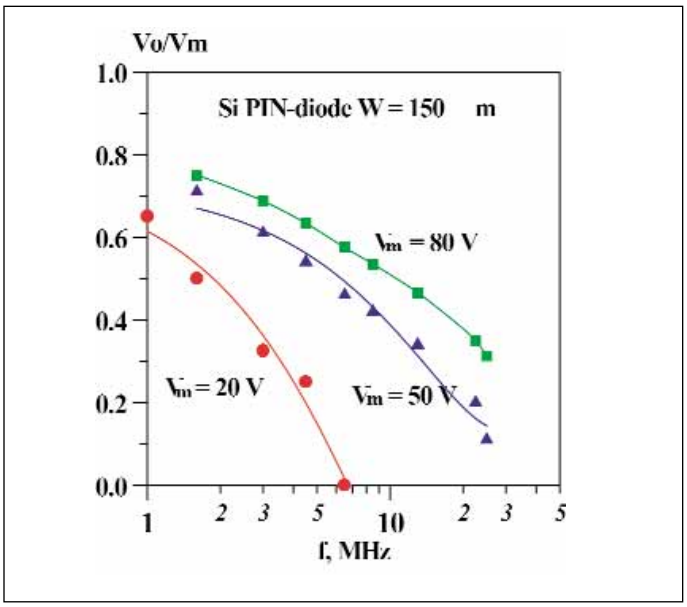
A program based on the isothermal drift-diffusion model of a semiconductor structure was also implemented for simulation and determination of the required DC reverse bias voltage [12]. This program numerically solves one-dimensional continuity equations for electrons and holes, the Poisson equation and the total current equation.

Experimental measurements

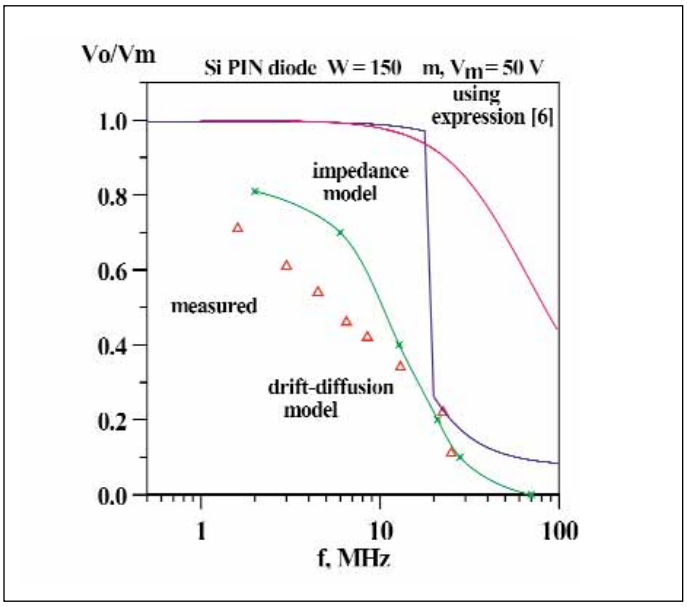
The measured required DC reverse bias voltage data were taken using the experimental setup described in [8]. The input RF signal was generated with a power CW transponder that was allowed to reach the amplitude of several tens of volts in the waveband of several megahertz. As a device under tests, the shunting different PIN diodes with the return path were used. The DC current rectified by the diode was monitored as a measure of merit of the diode nonlinearity. The current value of 10 mA was chosen as the sufficient experimental parameter of the low nonlinearity and low harmonic distortion when a reverse bias voltage was applied to the PIN diode.

The silicon PIN diodes used in the experimental measurements had different i-layer thicknesses: W = 20 mm, 70 mm and 150 mm. Figure 2 illustrates the measured minimum necessary DC reverse-biased voltage (V_o), keeping PIN diodes in the low nonlinearity and low harmonic distortion state against frequency. The measurements were performed for all types of diodes, with the RF amplitude across the diode (V_m) of 20 V [Figure 2(a)] and 50 V [Figure 2(b)]. The shapes of the curves are in accordance with the experimental curve shown in [5] for the thick PIN diode and theoretical discussions in [6–9]. Figure 2 shows that when the i-layer thickness increases, the area with the diminished required DC reverse bias voltage shifts to the lower frequencies.

Figure 3 shows the required DC reverse-bias voltage against frequency with a different input RF voltage amplitude. The silicon PIN diode with the i-layer thick-



▲ **Figure 3. Required DC reverse-bias voltage versus frequency of a 150 μm PIN diode with a different input RF voltage amplitude.**



▲ **Figure 4. Computed and experimental results [9].**

ness of 150 mm was under test. Figure 3 clearly shows that the area with the diminished voltage shifts to the higher frequencies while the applied RF voltage amplitude increases.

Computer simulation results and discussion

Three different mathematical and physical models were used to estimate the necessary DC reverse bias voltage to keep the PIN diode in a low-distortion state. Computed results based on these models are verified with experimental RF performance data.

The silicon PIN diode with p^+–n–n^+ structure and the i-layer width of 150 μm was used in simulation. The other parameters of the diode were: cross-section of 3.14×10^{-2} cm^2; i-layer doping level of 5×10^{12} cm^{-3}; and electron and hole lifetimes of 10^{-5} s. The diode doping profile was assumed to be abrupt, with acceptor p^+ and donor n^+ concentrations of 5×10^{19} cm^{-3} and 1×10^{20} cm^{-3}, respectively.

The distortion factor was used as a nonlinearity and a distortion figure of merit in calculations with a drift-diffusion model [7]. The distortion factor value of 10^{-4} was chosen as the permissible low level of harmonic distortions. The effective threshold voltage $V_{t\,eff}$ of 0.1...0.2 V plays the same role in the multilayer impedance PIN diode model (see the appendix). In both models, it provides a DC current generated by the PIN diode of several microamperes. This is in agreement with the experimental parameter of the low nonlinearity and low harmonic distortion that have been used in the measurements.

Figure 4 compares the measured and computed required reverse bias DC voltage V_o [9]. The computed results based on the isothermal drift-diffusion model of a semiconductor structure (green line) provide the better agreement with the experimental data, but the use of this model requires a lot of time. Computed data based on the analytical expressions (red line) [6], taking into account only the i-region transit time, shows qualitative agreement but overestimates the required DC reverse bias voltage in a wide frequency range. The accuracy of this expression is decreased for the PIN diodes with the i-layer thickness exceeding the depleted region width.

The multilayer impedance model, considering transit time and effects of the field distribution inside the i-layer, produces a compromise between the computational time and accuracy. It provides more precision estimation (blue line) than the model [6] and it does not require significant computation time like the drift-diffusion model [12]. The expressions for the minimum required reverse DC bias voltage estimations, using this model, are shown in the Appendix.

Conclusion

A reverse-bias state of the PIN diodes with different i-layer thicknesses were under experimental consideration in this article. Several mathematical and physical models were used to estimate the necessary DC reverse-bias voltage to keep PIN diodes in a low-distortion state. The multilayer impedance model, considering the electric field distribution inside the i-layer, provides the trade-off between the computational time and accuracy. It allows engineers and designers of microwave control devices to obtain more precise estimations of the required reverse DC bias voltage. ■

Acknowledgements

The author wishes to thank Prof. I.V. Lebedev as a scientific adviser, Prof. A.S. Shnitnikov for helpful discussions and Dr. N.I. Filatov for the permission to use the computer software ISTOC.

References

1. C.J. Weisman, *Essential Guide to RF and Wireless,* Upper Saddle River, NJ: Prentice Hall, 1999.

2. R.V. Garver, *Microwave Diode Control Devices*, Norwood, MA: Artech House, 1976.

3. J.F. White, *Microwave Semiconductor Engineering*, New York: Van Nostrand Reinhold, 1982.

4. H.M. Olson, "Design Calculations of Reverse Bias Characteristics for Microwave PIN Diodes," *IEEE Trans.*, 1967, Vol. ED-14, No. 8: 418–428.

5. M. Caulton, et.al., "PIN Diodes for Low Frequency High Power Switching Application," *IEEE Trans.*, 1982, MTT-30, No. 6: 875–886.

6. R.H. Caverly and G. Hiller, "Establishing the Minimum Reverse Bias for a PIN diode in a High-power Switch," *IEEE Trans.*, 1990, MTT-38, No. 12, 1938–1943.

7. I.V. Lebedev, et.al., "Minimal Reverse Bias Voltage of the High-power PIN diode Switch," *Radioelectronics and Communications Systems*, V ol. 38, No. 10, 1995: 21.

8. L.M. Drozdovskaia and N.V. Drozdovski, "Experimental Exploration of a Reverse Biased Thick Silicon PIN diodes," *Proceedings of the Power Conversion, Intelligent Motion & HFPC Conference,* Tokyo, Japan, April 15–17, 1998: 83–86.

9. L.M. Drozdovskaia, "RF Frequency Properties of a Reverse-biased Thick Switching PIN diode," *Proceedings of the 2000 IEEE Radio and Wireless Conference*, September 10–13, 2000, Denver, CO: 147–150.

10. I.V. Lebedev, "Nonlinear Properties and Characteristics of Microwave PIN diodes," *Radioelektronika* (Izv. VUZ), 1992, Vol. 30, No. 11: 1944–1947.

11. P.R. Hercfeld, et al, "Optically Controlled Microwave Devices and Circuits," *RCA Review*, Vol. 46, 1985: 528–551.

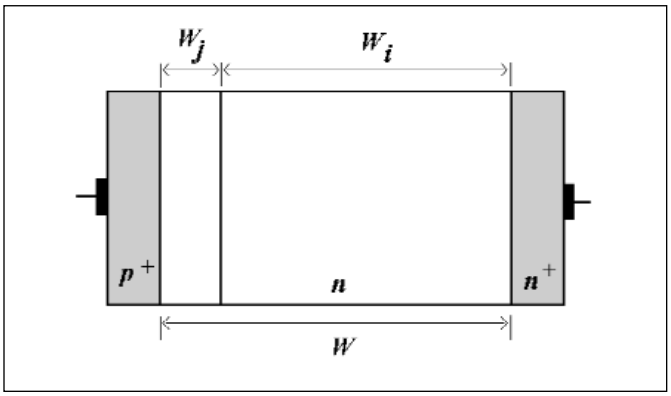
12. A.S. Shnitnikov and N.I. Filatov, "Microwave Limiter Diode Performance Analyzed by Mathematical Modeling," *Solid-State Electronics*, 1991, Vol. 34, No. 1: 91–97.

Author information

Lioudmila Drozdovskaia received a Diploma in Electrical Engineering in 1984 and the Candidate of Technical Science Degree in Microelectronics in 1997, both from the Moscow Power Engineering Institute (Technical University), Moscow, Russia. She has authored and co-authored 10 journal papers, about 20 conference presentations and holds 6 patents. Her main research interests are RF and microwave control devices and semiconductor components, especially Si and GaAs PIN diodes. She can be contacted at ECE Department, Villanova University, 800 Lancaster Ave., Villanova, PA 19085; Tel: 619-519-4973; E-mail: ldrozd@ece.vill.edu.

Appendix

The impedance multilayer model of a PIN diode [7, 10] is based on the notion that the i-region of the diode below punch-through consists of undepleted and depleted regions (Figure A1). The depleted region width W_j and capacitance C_j of a reverse-biased PIN diode are defined using the expressions:



▲ **Figure A1. Multilayer model of the PIN diode.**

$$W_j = W_{j0} \times \sqrt{1 + \frac{V_0}{V_k}} \quad (1)$$

$$C_j = C_{j0} \times \sqrt{1 + \frac{V_0}{V_k}} \quad (2)$$

where

$$W_{j0} = \sqrt{\frac{2\varepsilon_i V_k}{eN}} \quad (3)$$

$$C_{j0} = \sqrt{\frac{\varepsilon_i S}{W_{j0}}} \quad (4)$$

continued on following page

W_{j0} = depleted region width of non-biased diode, V_k = built-in potential, V_0 = DC reverse bias voltage, e = single charge, N = i-layer doping level, ε_i = silicon dielectric permittivity, S = diode cross-section area. The value of depleted region resistance R_j was assumed to be about 1 to 2 Mohms.

The undepleted region capacitance C_i and resistance R_i are

$$C_i = \frac{\varepsilon_i S}{W - W_j} \tag{5}$$

$$R_i = \frac{\rho\left(W - W_j\right)}{S} \tag{6}$$

where

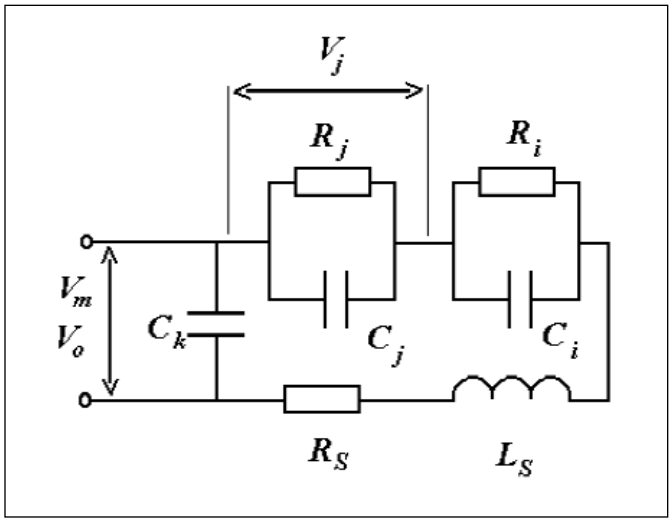
$$\rho = \frac{1}{(e\mu N)} \tag{7}$$

ρ = i-layer bulk resistance, W = i-layer width, μ = the majority carrier mobility.

The equivalent circuit of the diode according to this model is shown in Figure A2. There are also parasitic elements such as inductance L_s, contact or passive regions resistance R_s and package capacitance C_k (in the case of packaged PIN diode).

This model also takes into account the transit time effect. It leads to the reduction of the voltage across the depleted region V_j in $1/F(\theta_j)$ times. Here, $F(\theta_j)$ is the empirical function of the non-zero carrier transit time threw depleted region. This depends on diode geometry, semiconductor material properties, RF or microwave input power and applied DC reverse bias voltage [10].

When the diode is under DC zero or reverse bias voltage, $R_j >> R_i$. Therefore, DC voltage across the PIN diode is applied directly to the depleted region (to p^+–n junction). Applied AC voltage is divided between two regions in an i-layer according to the properties of



▲ **Figure A2. Equivalent circuit of a PIN diode.**

the frequency-dependent impedance divider formed by depleted and undepleted regions. It was assumed that p^+–n junction does not produce harmonic distortions when the total voltage across the depleted region is less than the effective threshold voltage $V_{t\,eff}$. This value was assumed to be about 0.1…0.2 V. This condition is written as [7]:

$$V_j - V_0 \le V_{t\,eff} \tag{8}$$

Finally, we can estimate required reverse bias DC voltage V_0 (for $L_s \approx 0$, and $R_s \approx 0$) as:

$$V_0 = V_m \times F\left(\Theta_j\right) \times \left| 1 + \frac{R_i}{R_j} \times \frac{1 + j2\pi f C_j R_j}{1 + j2\pi f C_i R_i} \right|^{-1} - V_{t\,eff} \tag{9}$$

where f is the operating frequency, V_m is the RF or microwave amplitude across the diode. Taking into account Equations (1) and (2), we can see that Equation (9) is the nonlinear equation, with V_0 : $V_0 = F(V_0)$, and should be solved iteratively.