Gallium-Arsenide Chip Costs

Today gallium-arsenide chips, especially integrated circuits, are sufficiently expensive to qualify GaAs as a technology of the future, something it has been called for the last 20 years. The author examines how defect densities, overall process yields and raw material costs contribute to finished chip costs.

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Numerous high volume applications for gallium-arsenide chips are unexplored because the user community identifies GaAs with, not only high prototype costs, but high production costs. Despite the fact that GaAs circuit applications have increased, this perception, supported by the notions of $10,000 wafer costs, has precluded GaAs even from being considered for use in many systems of the future.

Our firm has analyzed the manufacturing costs of GaAs products, paying particular attention to the construction of a GaAs wafer fabrication cost model. The fabrication cost for a 14-mask, three-layer metal, GaAs process was calculated and, for reference, compared to the cost of an 18-mask, two-layer metal, BiCMOS process. The analyses begin with fixed asset costs and add direct and indirect manufacturing costs. Assuming reasonable facility utilization (wafer volume), the input wafer fabrication costs for the two processes are reasonably comparable.

Using a silicon defect-density model (Murphy), die costs for four GaAs dice and one silicon die were obtained. Calculations of assembly and final test costs and final test yields resulted in product costs. At a $188.00 price, an 80,000 square mil digital ASIC GaAs device would currently contribute a gross margin of 50 percent. If silicon-type yields can be achieved, the same gross margin would be realized at a selling price of $96.00.

Gallium-arsenide has been called the integrated circuit technology of the future for the past twenty

years, and likely will retain this image until it is manufactured with efficiencies and yields that approach those of silicon manufacturers.

Unless those gallium-arsenide manufacturers who are presently sales leaders dramatically improve their manufacturing operations, they will be overtaken by the large silicon houses that are investing heavily in gallium-arsenide. Figure 1 lists some of the recent gallium-arsenide announcements. Companies such as Motorola and Fujitsu, which have large 200mm diameter silicon wafer fabrication operations, will apply their silicon-based experience to gallium-arsenide manufacturing. It is highly unlikely that these companies, which achieve 98-100 percent wafer throughput yields when running 200mm silicon wafers, will accept 50-65 percent yields when running 100mm gallium-arsenide wafers.

Although integrated circuit cost analyses seem to be fraught with complex variables and assumptions, there are a relatively few issues that always seem to apply. At the forefront of these are facility utilization and yields.

Facility Utilization

The high cost of facilities and equipment have made facility utilization a more significant factor in cost of manufacturing integrated circuits. Figure 2 shows the impact of facility utilization on the cost of processing an integrated circuit wafer. If the facility described in this figure were being operated at 100 percent of capacity, the direct labor would be six percent of the total wafer cost, the price of the raw wafer would be 8.5 percent, direct and indirect factory overheads would be 31 percent, and depreciation would be 54 percent.

If the facility were only operating at 50 percent of capacity, depreciation would increase to 64.5 percent of the total wafer cost. This example clearly depicts one of the major problems facing gallium-arsenide manufacturers. The volume-sensitive nature of integrated circuit manufacturing weighs heavily on small manufacturers that are unable to establish and maintain run-rates that represent a high percent of their total capacity.

- Vitesse and Martin Marietta jointly form a military GaAs ASIC design center at a Martin Marietta facility in Littleton, CO.
- Seven European companies plan to form a joint GaAs research program under the guidance of the Eureka project.
- Thomson Microwave Components began ramping up its 100mm GaAs fab in Saint-Egreve, France in June of 1992. The fab will produce 0.8µ digital ICs (mostly ASICs).
- Fujitsu plans to have GaAs IC sales of $90M and GaAs discrete sales of $135M in FY92 (ending March '93).
- In February of 1992, Vitesse announced it had begun shipping samples of its 0.6µ 350K-gate GaAs array. The device has 1.2M transistors and offers 130ps loaded gate delays.
- In the largest financial commitment to GaAs technology to date by a major U.S. chip maker, Motorola is investing $100 million in a Tempe, Arizona, plant.

Figure 1. Sampling of 1992 GaAs announcements.

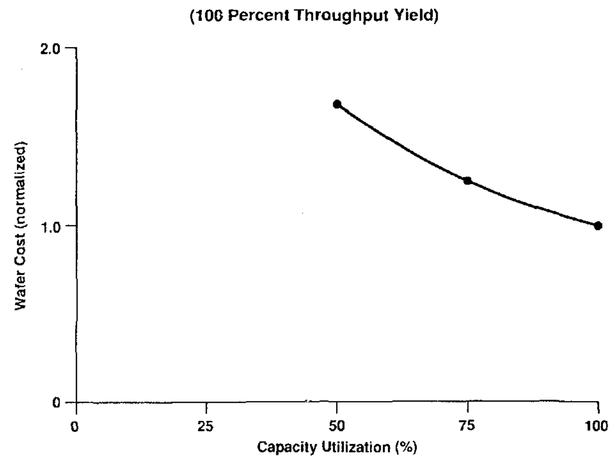

Figure 2. Wafer cost versus capacity utilization.

Since many of the gallium-arsenide manufacturers and many of the silicon ASIC manufacturers fit this description far too well, facility loading is not used as a factor in the models in this paper, however the influence of facility loading should not be ignored.

GaAs Models

The gallium-arsenide process analyzed in this paper is shown in Figure 3. It is a 14-mask, three-layer metal process using steppers on all mask layers and 100mm wafers. The labor costs presume a facility located in the northwest part of the U.S.

The wafer throughput yield shown in Figure 3 is 67.4 percent. This is a fairly optimistic number for gallium-arsenide manufacturers today.

The cost calculations are based on 100 percent capacity utilization. This is very optimistic. Since the costs for the BiCMOS process described below are also based on 100 percent utilization, directly comparing the costs of the two processes is valid. For utilization rates of less than 100 percent, the derating curve shown in Figure 2 can be used with acceptable accuracy.

BiCMOS (Silicon)

The silicon BiCMOS process analyzed in this paper is shown in Figure 4. It is an 18-mask, two-layer

GaAs COST MODEL

(D.L. + MNFG OH = $37.50/HR)

PROCESS STEP	DIRECT MATERIAL COST ($)	EQUIPMENT COST ($)	HOURLY DEPRECIATION ($)	UNITS/HOUR	UNYIELDED COST ($)	YIELD (%)	YIELDED COST ($)	CUMULATIVE YIELD (%)
WAFER 4" TO SPEC	260				0.00	100.0	260.00	100.0
WAFER PREP		100,000	4.81	15	2.82	99.0	265.48	96.0
IMPLANT OXIDE DEP		100,000	4.81	30	1.41	100.0	266.89	96.0
WAFER ID MARK		50,000	2.40	15	2.66	100.0	269.55	96.0
ALIGN MK 1.0		1,800,000	86.54	30	4.13	100.0	273.68	96.0
OXIDE ETCH		30,000	1.44	50	0.78	100.0	274.46	96.0
ENHANCE MK 2.0		1,800,000	86.54	30	4.13	99.0	281.41	95.0
ENHANCE IMPL		500,000	24.04	15	4.10	100.0	285.51	95.0
DEPL MK 3.0		1,800,000	86.54	30	4.13	99.0	292.57	94.1
DEPL IMPL		500,000	24.04	15	4.10	100.0	296.67	94.1
N+ CONT MK 4.0		1,800,000	86.54	30	4.13	99.0	303.85	93.1
N+ CONT IMPL		500,000	24.04	15	4.10	100.0	307.95	93.1
OXIDE ETCH		100,000	4.81	50	0.85	100.0	308.80	93.1
OXIDE REDEP		100,000	4.81	30	1.41	100.0	310.21	93.1
ANNEAL		100,000	4.81	20	2.12	100.0	312.32	93.1
OXIDE STRIP		100,000	4.81	50	0.85	100.0	313.17	93.1
FLD NIT DEP		300,000	14.42	15	3.46	100.0	316.63	93.1
TFR MK 5.0		1,800,000	86.54	30	4.13	99.0	324.00	92.2
TFR DEP		300,000	14.42	15	3.46	100.0	327.46	92.2
TFR LIFTOFF		200,000	9.62	30	1.57	100.0	329.04	92.2
TFR CONT MET MK 6.0		1,800,000	86.54	30	4.13	99.0	336.54	91.3
TiPdAu DEP	10	300,000	14.42	10	15.19	100.0	351.73	91.3
TiPdAu LIFT OFF		200,000	9.62	30	1.57	100.0	353.30	91.3
TFR SINTER		100,000	4.81	20	2.12	100.0	355.41	91.3
OHMIC MET MK 7.0		1,800,000	86.54	30	4.13	99.0	363.18	90.4
NIT ETCH		300,000	14.42	20	2.60	100.0	365.78	90.4
AuGeNiAu DEP		300,000	14.42	10	5.19	100.0	370.97	90.4
LIFTOFF		200,000	9.62	30	1.57	99.0	376.30	89.5
ALLOY		50,000	2.40	50	0.80	100.0	377.10	89.5
PRE-ISO PROBE		100,000	4.81	12	3.53	97.0	392.40	86.8
ISO MK 8.0		1,800,000	86.54	30	4.13	100.0	396.53	86.8
ISO IMPL		500,000	24.04	30	2.05	100.0	398.58	86.8
GATE MET MK 9.0	10	1,800,000	86.54	15	18.27	98.0	425.36	85.1
NIT ETCH		300,000	14.42	20	2.60	100.0	427.96	85.1
Vt ADJUST ETCH (RECESS)		300,000	14.42	10	5.19	96.0	451.20	81.7
TiPdAu DEP	15	300,000	14.42	10	20.19	100.0	471.39	81.7
LIFTOFF		200,000	9.62	30	1.57	98.0	482.61	80.0
NIT DEP		300,000	14.42	20	2.60	100.0	485.21	80.0
MET 1 MK 10.0		1,800,000	86.54	30	4.13	99.0	494.28	79.2
NIT ETCH		300,000	14.42	20	2.60	100.0	496.88	79.2
TiPdAu MET 1 DEP		300,000	14.42	10	5.19	100.0	502.07	79.2
LIFT OFF		200,000	9.62	30	1.57	98.0	513.92	77.6
1ME PROBE		100,000	4.81	10	4.23	95.0	545.42	73.8
NIT DEP		300,000	14.42	20	2.60	100.0	548.02	73.8
VIA MK 11.0		1,800,000	86.54	30	4.13	100.0	552.15	73.8
NIT ETCH		300,000	14.42	20	2.60	100.0	554.75	73.8
A/B MET POST MK 12.0		1,800,000	86.54	30	4.13	99.0	564.53	73.0
TiPdAu DEP		300,000	14.42	10	5.19	100.0	569.72	73.0
A/B MET MK 13.0		1,800,000	86.54	30	4.13	99.0	579.65	72.3
ELECTROPLT AU	15	100,000	4.81	8	20.29	98.0	612.19	70.8
FLD MET ETCHBACK		500,000	24.04	15	4.10	100.0	616.29	70.8
NIT DEP		300,000	14.42	20	2.60	100.0	618.89	70.8
PAD MK 14.0		1,800,000	86.54	30	4.13	99.0	629.31	70.1
NIT ETCH-PLAS		300,000	14.42	20	2.60	100.0	631.91	70.1
PARAMETRIC PROBE		100,000	4.81	8	5.29	98.0	650.20	68.7
QA FINAL INSPECTION		30,000	1.44	12	3.25	98.0	666.78	67.4
UNYIELDED COST ADDED					234.56			

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Figure 3. GaAs cost model.

BiCMOS COST MODEL

(D.L. + MNFG OH = $25.00/HR)

PROCESS STEP	DIRECT MATERIAL COST ($)	EQUIPMENT COST ($)	HOURLY DEPRECIATION ($)	UNITS/HOUR	UNYIELDED COST ($)	YIELD (%)	YIELDED COST ($)	CUMULATIVE YIELD (%)
WAFER:P(100)	20				20.00	100.0	20.00	100.0
INIT OXID		100,000	4.81	100	0.30	100.0	20.30	100.0
N+ B.L. MK 1.0		1,800,000	86.54	30	3.72	100.0	24.02	100.0
OXID ETCH,WET		20,000	0.96	250	0.10	100.0	24.12	100.0
SCREEN OXID		100,000	4.81	100	0.30	100.0	24.42	100.0
N+BL IMPL		500,000	24.04	50	0.98	100.0	25.40	100.0
IMPL DRV IN		100,000	4.81	50	0.60	100.0	25.99	100.0
OXID STRIP		20,000	0.96	250	0.10	100.0	26.10	100.0
P B.L. IMPL		500,000	24.04	50	0.98	100.0	27.08	100.0
INTRIN EPI-RPCVD		800,000	38.46	10	6.35	99.0	33.76	99.0
PAD OXID		100,000	4.81	100	0.30	100.0	34.06	99.0
N-WELL MK 2.0		1,800,000	86.54	30	3.72	100.0	37.78	99.0
N-WELL IMPL		500,000	24.04	50	0.98	100.0	38.76	99.0
P-WELL MK 3.0		1,800,000	86.54	30	3.72	100.0	42.48	99.0
P-WELL IMPL		50,000	2.40	50	0.55	100.0	43.03	99.0
NIT DEP-LPCVD		100,000	4.81	50	0.60	100.0	43.62	99.0
OXID DEF MK 4.0		1,800,000	86.54	30	3.72	100.0	47.34	99.0
NIT PLAS ETCH		300,000	14.42	20	1.97	100.0	49.31	99.0
FLD IMPL		500,000	24.04	50	0.98	100.0	50.29	99.0
FLD OXID		300,000	14.42	50	0.79	100.0	51.08	99.0
NIT STRIP/OX DIP-2		20,000	0.96	250	0.10	100.0	51.18	99.0
SACRIF OXID		100,000	4.81	100	0.30	100.0	51.48	99.0
Vt IMPL		500,000	24.04	50	0.98	100.0	52.46	99.0
P Vt MK 5.0		1,800,000	86.54	30	3.72	100.0	56.18	99.0
P Vt IMPL		500,000	24.04	50	0.98	100.0	57.16	99.0
SACRIF OXID STRIP		100,000	4.81	100	0.30	100.0	57.46	99.0
GATE OXID		100,000	4.81	100	0.30	99.0	58.34	98.0
POLY I DEP-LPCVD		100,000	4.81	50	0.60	100.0	58.94	98.0
POCl3 PREDEP		100,000	4.81	50	0.60	100.0	59.53	98.0
GATE MK 6.0		1,800,000	86.54	30	3.72	100.0	63.25	98.0
POLY PLAS ETCH		300,000	14.42	20	1.97	100.0	65.22	98.0
COLLECT MK 7.0		1,800,000	86.54	30	3.72	100.0	68.94	98.0
COLLECT IMPL		500,000	24.04	50	0.98	100.0	69.92	98.0
COLLECT DRV IN		100,000	4.81	50	0.60	100.0	70.52	98.0
BASE MK 8.0		1,800,000	86.54	30	3.72	100.0	74.24	98.0
BASE IMPL		500,000	24.04	50	0.98	100.0	75.22	98.0
N+ S/D MK 9.0		1,800,000	86.54	30	3.72	100.0	78.93	98.0
LDD IMPL		500,000	24.04	50	0.98	100.0	79.92	98.0
LTO SPCR DEP-LPCVD		100,000	4.81	50	0.60	100.0	80.51	98.0
LTO ETCH BK-PLAS		400,000	19.23	50	0.88	100.0	81.40	98.0
N+ S/D MK 9.0		1,800,000	86.54	30	3.72	100.0	85.11	98.0
N+ S/D IMPL		500,000	24.04	50	0.98	100.0	86.09	98.0
P+ S/D MK 10.0		1,800,000	86.54	30	3.72	100.0	89.81	98.0
P+ S/D IMPL		500,000	24.04	50	0.98	100.0	90.79	98.0
INTR-PLY LTO DEP-LPCVD		100,000	4.81	50	0.60	100.0	91.39	98.0
SHRD CONT MK 11.0		1,800,000	86.54	30	3.72	99.0	96.07	97.0
LTO PLAS ETCH		300,000	14.42	20	1.97	100.0	98.04	97.0
POLY 2 DEP-LPCVD		100,000	4.81	50	0.60	100.0	98.64	97.0
POLY 2 MASK 12.0		1,800,000	86.54	30	3.72	100.0	102.35	97.0
POLY 2 PLAS ETCH		300,000	14.42	20	1.97	99.5	104.85	96.5
HI VAL RESIS IMPL		500,000	24.04	50	0.98	100.0	105.83	96.5
N+ EMIT/Vcc MK 13.0		1,800,000	86.54	30	3.72	100.0	109.55	96.5
N+ EMIT IMPL		500,000	24.04	50	0.98	100.0	110.53	96.5
EMIT DRV IN		100,000	4.81	100	0.30	100.0	110.83	96.5
BPSG DEP-LPCVD		300,000	14.42	50	0.79	100.0	111.61	96.5
BPSG STABIL		100,000	4.81	100	0.30	100.0	111.91	96.5
CONT MK 14.0		1,800,000	86.54	30	3.72	100.0	115.63	96.5
BPSG PLAS ETCH		400,000	19.23	50	0.88	99.0	117.69	95.6
REFLO		100,000	4.81	100	0.30	100.0	117.99	95.6
MET 1 DEP		400,000	19.23	20	2.21	100.0	120.20	95.6
MET 1 MK 15.0		1,800,000	86.54	30	3.72	100.0	123.92	95.6
MET 1 PLAS ETCH		400,000	19.23	20	2.21	99.0	127.41	94.6
INTRMTL DIEL DEP		100,000	4.81	50	0.60	100.0	128.00	94.6
VIA MK 16.0		1,800,000	86.54	30	3.72	100.0	131.72	94.6
DIEL PLAS ETCH		300,000	14.42	20	1.97	99.5	134.36	94.2
MET 2 DEP		400,000	19.23	20	2.21	100.0	136.57	94.2
MET 2 MK 17.0		1,800,000	86.54	30	3.72	100.0	140.29	94.2
MET 2 PLAS ETCH		400,000	19.23	20	2.21	99.0	143.94	93.2
PAD DEP-PECVD		100,000	4.81	50	0.60	100.0	144.54	93.2
PAD MASK 18.0		1,800,000	86.54	30	3.72	100.0	148.26	93.2
PAD ETCH		400,000	19.23	20	2.21	100.0	150.47	93.2

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Figure 4. BiCMOS cost model.

metal process using steppers on all mask layers and 100mm wafers. Although 125mm and 150mm wafers represent a very high percent of silicon production today, many ASIC lines are still using 100mm wafers.

The wafer throughput yield shown in Figure 4 is 93.2 percent. This is relatively conservative for a well-run 100mm facility. As mentioned above, the cost calculations shown in Figure 4 are based on 100 percent utilization.

Throughput Yield

A major difference between the efficiencies of gallium-arsenide manufacturers and silicon manufacturers is throughput yield. The throughput yields of gallium- arsenide manufacturers have improved in the last five years increasing from 50 percent yields on three-inch wafers to over 60 percent yields on 100mm wafersbut these figures do not approach the greater than 90 percent yields that silicon producers routinely achieve on 100mm, 125mm, 150mm, and even 200mm wafers.

The impact of the lower gallium-arsenide throughput yield is magnified by the higher cost of gallium-arsenide wafers. As shown in Figure 5, gallium-arsenide wafers cost more than 20 times silicon wafers on a square inch basis. Accordingly, yielded wafer area that does not produce useful product is correspondingly more expensive.

Figure 6 shows how the cost of a gallium-arsenide wafer, produced on the process shown in Figure 3, varies with throughput yield. At the 67.4 percent yield shown in Figure 3, the cost would be $667.00. Fifty percent yields, however, are not uncommon in gallium-arsenide operations, so a $900.00 finished wafer cost would not be extraordinary.

In order to be competitive with silicon, gallium-arsenide producers must dramatically improve their throughput yields. Since silicon producers can achieve over 95 percent yields on 200mm wafers, gallium-arsenide should be able to achieve 95 percent yields on 100mm wafers, having only one fourth the area. For the process shown in Figure 3,

Wafer Size	Material	Price ($)	Cost/sq. in. ($)
3 inch	GaAs	185.00	26.20
100mm	GaAs	260.00	20.70
100mm	Silicon	10.00	0.80

Figure 5. Raw wafer costs.

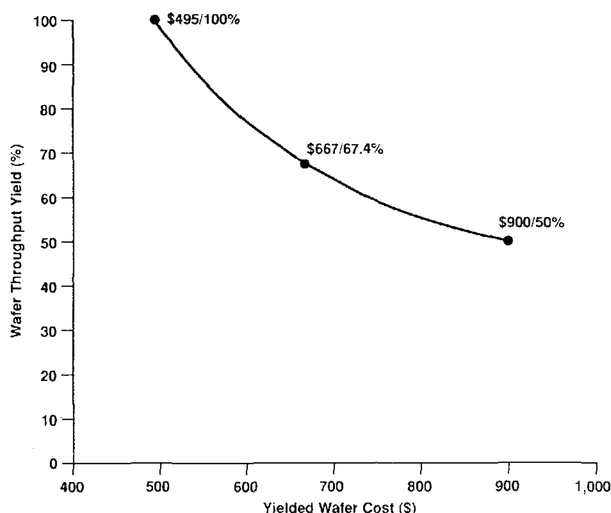

Figure 6. GaAs yielded wafer cost versus throughput yield.

this would result in a wafer cost of $510.00 (Figure 6). While still much higher than the cost of a silicon wafer, this cost would make gallium-arsenide much more competitive on a cost-performance basis, at least in the markets for larger chips. For smaller chips, the die cost is small compared to packaging and testing costs.

Probe Yields

Gallium-arsenide operations typically experience much lower probe yields than silicon operations. State-of-the-art silicon processes with mask levels in the higher teens typically have probe yields corresponding to defect densities of less than 1 defect per square centimeter. A process such as the one described in Figure 4 would have a defect density of 1.5, corresponding to a die sort yield of almost 50 percent (Figure 7).

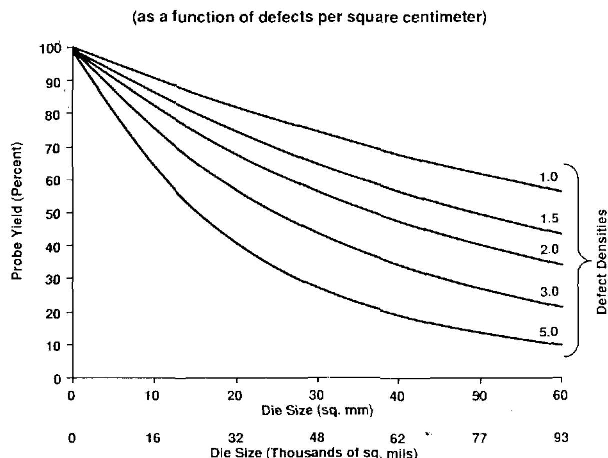

Figure 7. Murphy's probe yield forecast.

Direct Labor Rate	$10.00/hr.
Manufacturing Overhead	300%
Laser Cost	$500K
Tester Cost	$500K
Contract Assembly Used	

Figure 8. Back end cost model assumptions.

Gallium-arsenide operations typically experience defect densities of 5 defects per square centimeter, or greater. Given the shapes of the curves in Murphy's model, a 1600 square mil microwave converter gallium-arsenide wafer would have a die sort yield approaching 100 percent. In actual practice, these wafers would probably not be probed at all.

For larger die sizes however, a defect density of 5 results in almost unacceptable yields. At 40,000 square mils this defect density would correspond to a die sort yield of around 35 percent; at 80,000 square mils it could correspond to less than 20 percent (Figure 7).

Back End (Assembly and Test) Costs

The assumptions used in calculating the back end costs for both the silicon and gallium-arsenide products are shown in Figure 8. Applying these assumed costs to the individual products results in the product costs in Figures 9 and 10. Figure 9 is based on the yields corresponding to a defect density of 5 and wafer costs of $900.00 and $510.00 (throughput yields of 67 percent and 95 percent, respectively). Figure 10 is based on yields corresponding to a defect density of 1.5 and the same gallium-arsenide wafer costs used in Figure 9.

The silicon wafer cost shown in Figure 10 is 25 percent higher than was calculated in Figure 4 because it is assumed that the wafer was produced by an offshore foundry and sold to a North American company at a price higher than the cost.

Figure 11 summarizes the calculations displayed in Figures 9 and 10. It is somewhat interesting to note that improvements in wafer throughput yields don't dramatically impact the final cost of the product at the smaller die sizes. In essence, the packaging costs swamp the die costs. At the larger die

(Defect Density = 1.5 Defects/cm^2)

Product	GaAs Microwave Converter		GaAs Microwave Device		GaAs Datacom Chip		GaAs Digital ASIC		Silicon BiCMOS Digital ASIC
Die size (sq. mil)	1600		4000		40,000		80,000		80,000
Potential Die/Wafer	4800		2400		225		110		110
Wafer Cost	$900.00	$510.00	$900.00	$510.00	$900.00	$510.00	$900.00	$510.00	$188.00
Die Sort Cost	0	0	$30.50	$30.50	$30.50	$30.50	$30.50	$30.50	$30.50
Die Sort Yield	100%	100%	96%	96%	70%	70%	60%	60%	60%
Yielded Die Cost	$0.188	$0.106	$0.404	$0.235	$5.89	$3.42	$14.10	$8.19	$3.31
Saw Cost/Die	$0.094	$0.094	$0.119	$0.119	$0.63	$0.63	$1.51	$1.51	$1.51
Package	16-pin Plastic SOIC		Ceramic Microwave		68-pin LCC		144-pin PGA		144-pin PGA
Package Cost	$0.25	$0.25	$4.50	$4.50	$10.00	$10.00	$22.00	$22.00	$22.00
Assembly Cost	$0.35	$0.35	$2.20	$2.20	$5.00	$5.00	$8.50	$8.50	$8.50
Assembly Yield	97%	97%	90%	90%	96%	96%	95%	95%	95%
Assembled Unit Cost	$0.91	$0.825	$8.02	$7.84	$22.42	$19.84	$48.54	$42.32	$37.18
Final Test Cost	$0.26	$0.26	$0.66	$0.66	$0.35	$0.35	$0.87	$0.87	$0.87
Final Test Yield	86%	86%	75%	75%	75%	75%	90%	90%	90%
Product Cost	$1.36	$1.26	$11.57	$11.33	$30.36	$26.92	$54.90	$47.98	$42.28
Price @ 50% Gross Margin	$2.72	$2.52	$23.14	$22.66	$60.72	$53.84	$109.80	$95.94	$84.56

Figure 10. Silicon and GaAs back end cost model.

(Defect Density = 5 Defects/cm^2)

Product	Microwave Converter		Microwave Device		Datacom Chip		Digital ASIC	
Die size (sq. mil)	1600		4000		40,000		80,000	
Potential Die/Wafer	4800		2400		225		110	
Wafer Cost	$900.00	$510.00	$900.00	$510.00	$900.00	$510.00	$900.00	$510.00
Die Sort Cost	0	0	$30.50	$30.50	$30.50	$30.50	$30.50	$30.50
Die Sort Yield	100%	100%	87%	87%	35%	35%	19%	19%
Yielded Die Cost	$0.188	$0.106	$0.446	$0.254	$11.93	$6.80	$44.31	$25.74
Saw Cost/Die	$0.094	$0.094	$0.115	$0.115	$1.28	$1.28	$4.76	$4.76
Package	16-pin Plastic SOIC		Ceramic Microwave		68-pin LCC		144-pin PGA	
Package Cost	$0.25	$0.25	$4.50	$4.50	$10.00	$10.00	$22.00	$22.00
Assembly Cost	$0.35	$0.35	$2.20	$2.20	$5.00	$5.00	$8.50	$8.50
Assembly Yield	97%	97%	90%	90%	96%	96%	95%	95%
Assembled Unit Cost	$0.91	$0.825	$8.07	$7.85	$29.39	$23.08	$83.76	$64.21
Final Test Cost	$0.26	$0.26	$0.66	$0.66	$0.35	$0.35	$0.87	$0.87
Final Test Yield	86%	86%	75%	75%	75%	75%	90%	90%
Product Cost	$1.36	$1.26	$11.64	$11.35	$39.65	$31.24	$94.03	$72.31
Price @ 50% Gross Margin	$2.72	$2.52	$23.28	$22.70	$79.30	$62.48	$188.06	$144.62

Figure 9. GaAs back end cost model.

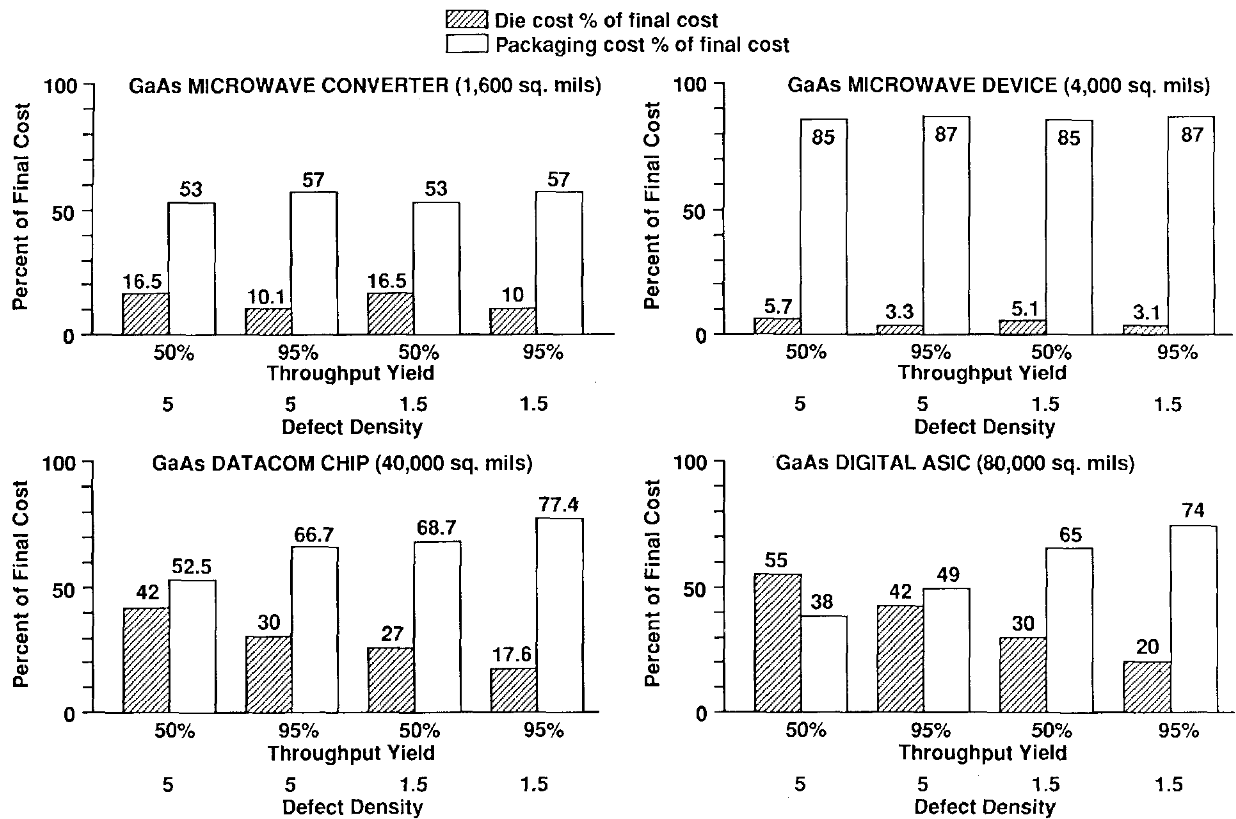

Figure 11. Die cost/packaging cost relationship.

sizes, however, there is a dramatic swing in the impact of the die cost on the total cost as the defect density goes down and the throughput yield increases. In fact, the 80,000 square mil gallium-arsenide ASIC device is only 15 percent more expensive than the 80,000 square mil silicon device.

Having determined what a gallium-arsenide device should cost, it is appropriate to examine the reasonableness of the projection. Silicon manufacturers have achieved almost 100 percent throughput yields on 200mm wafers and defect densities approaching 0.5 defects per square centimeter on processes with nearly twenty mask levels. This suggests that the 95 percent yield and 1.5 defect density used to determine what gallium-arsenide should cost are reasonable goals. But silicon manufacturers have invested extensively in manufacturing training, Statistical Process Control, and automation.

I believe that manufacturing training and Statistical Process Control should be addressed foremost, that automation by itself is not the answer, but that addressing these elements adequately can result in the gallium-arsenide chip costs presented here.

Mr. Skinner *has over 20 years of experience in the semiconductor industry; most recently as President of Lansdale Transistor and Electronics, a manufacturer of power semiconductor components.*

Prior to joining Lansdale, Mr. Skinner had been Vice President and Director of Power Products Operations at Motorola, including profit responsibility for product development, manufacturing, and marketing.

Other assignments at Motorola included Manager of Equipment Engineering, responsible for purchasing and maintaining semiconductor manufacturing equipment.

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