Silicon UHF IC Amplifier for Cellular Applications

The RF community consistently seeks increased performance levels from microwave integrated circuits. The authors describe the precursor to a monolithic amplifier, a silicon UHF hybrid integrated circuit which achieves 20dB gain as well as 20dBm power output.

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Over the past several years silicon microwave monolithic integrated circuits (MMIC) technology has produced steadily increasing levels of performance and complexity. Commercially available silicon MMICs perform a variety of block functions necessary for signal processing and amplification. A wide range of amplifier specifications have been demonstrated for low noise, power and gain.

Large market applications of microwave integrated circuits such as cellular communications will produce spin off products for lower volume applications.

The increasing requirements of users with applications from HF to Microwaves will produce advances similar to those seen in cellular radio but at a rate which is proportional to their respective market size and growth potential. However, despite their market size, applications at these frequencies will continue to benefit from the technological

gains developed for the very wide market represented by cellular/personal communications use.

To allow comparison between different designs, the Power-Gain Product versus Frequency has been plotted and is shown in Figure 1. Commercially available silicon MMICs which produce the highest Power-Gain Product have incorporated collector isolation techniques. Active transistors on these circuits can have the collectors biased individually and use RF feedback paths to increase performance and stability.

Analysis of these reported industry performance levels prompted our firm's establishment of goals for a low cost silicon MMIC which can produce an output of 100 milliwatts (+20 dBm), sufficient to drive a power amplifier stage directly in a cellular phone or similar UHF application.

Additionally, this MMIC should be capable of being driven by a device with a noise figure sufficiently low enough to meet system needs. The driver device may only be capable of producing an output power of about 1 mW (0 dBm) due to this noise constraint. Thereby was the goal established for 20 dB gain/+20 dBm in a cost competitive monolithic design operable from a DC supply voltage of 9.0 volts.

Figure 1 shows the performance of our hybrid amplifier (Model HAMP0572) which was developed to meet these goals. This hybrid is the precursor to a monolithic version which has been designed and is being fabricated with similar characteristics. The properties and design of the initial hybrid design to meet these goals are described in this paper.

There existed a need for a UHF driver having 20dB gain/20dBm power output.

The hybrid approach to a 20 dB gain/+20 dBm power amplifier for the cellular market was chosen to prove the concept of monolithic implementation, as well as to make available sooner this low cost (<$15) amplifier. To realize the hybrid amplifier we selected from our existing silicon MMIC chips the two most suitable designs for a cascaded amplifier chain, together with MOS capacitors, used for DC blocking and RF feedback.

Figure 2 shows the proposed circuit topology for cascading two of the silicon MMIC amplifiers. These die are placed in a low cost, studded screen metallized Beryllium oxide (BeO) package, referred to in the industry as an X072 package, which provides a suitable heat sink for power dissipation. This package has four leads (Figure 3) input, output, ground and a second D.C. power connection.

The reason for this second power lead is that at higher powers even the input section of the amplifier draws a significant amount of current, requiring a low value dropping resistor to maintain a suitable operating voltage. Of course, this resistor would also provide a substantial amount of negative RF feedback to the output, severely reducing the overall amplifier gain. Such an approach would be counter productive.

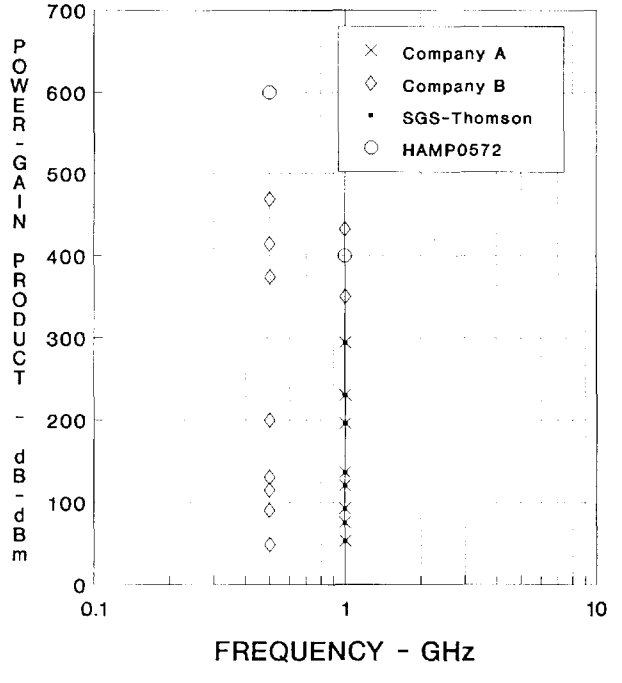

Figure 1. Available silicon MMIC amplifiers' power-gain products versus frequency.

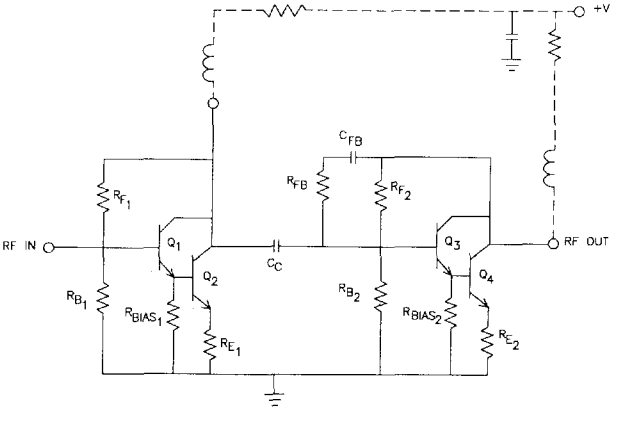

Figure 2. Circuit schematic for the 20dB gain/20dBm power output, hybrid, cascaded amplifier.

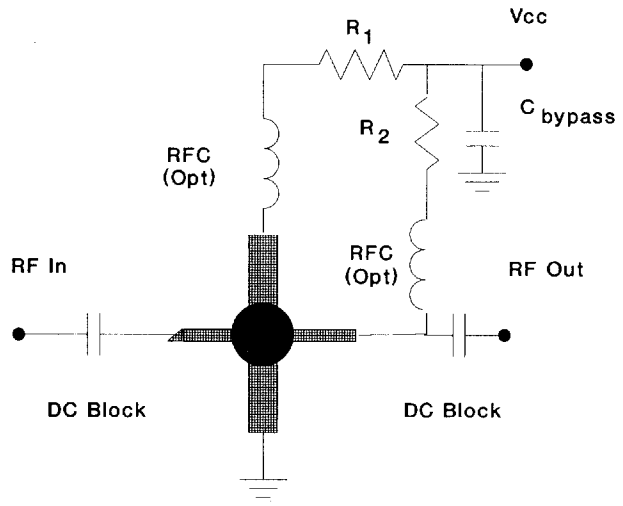

Figure 3. Amplifier lead connections and bias configuration.

One way to provide RF isolation between the two stages is to use a good RF ferrite with a minimum impedance value of 1000 ohms, but even if available, use of a ferrite would substantially increase the hybrid's complexity, size and cost. Instead, a separate AC choked power lead was employed and connected to the package's fourth lead. The remaining leads of this package provide the input, ground and output with bias.

The die are eutectically mounted with two interstage coupling capacitor bonds and two double stitched ground connections to provide a minimum of bond wire inductance. A stabilized epoxy is then used to encapsulate the entire top side of the package or else a low cost ceramic lid is used. This approach is amenable to large volume production. For applications requiring small size and large volume production there is a studless package with an isolated metallized bottom available, that in turn can be soldered to a suitable heatsink.

Even when available single stages suggest suitability as a cascaded amplifier, other considerations must be made.

Our firm's line of 50 ohm cascadable silicon MMIC amplifiers were candidates for the two stages of this hybrid amplifier. As seen in Table 1 the model C with 1 dB power compression point of +23 dBm is an obvious choice for use as the output device. However, the first, driver, stage was not obvious.

Table 1. Single stage amplifiers considered for the 20/20 hybrid cascaded amplifier design.

Amplifier	*Gain @1GHZ (dB)*	*P 1dB (dBm)*	*Id (mA)*
A (AMP 19)	15.0	14	45
B (AMP 11)	11.5	17	60
C (AMP 5)	8.5	23	165

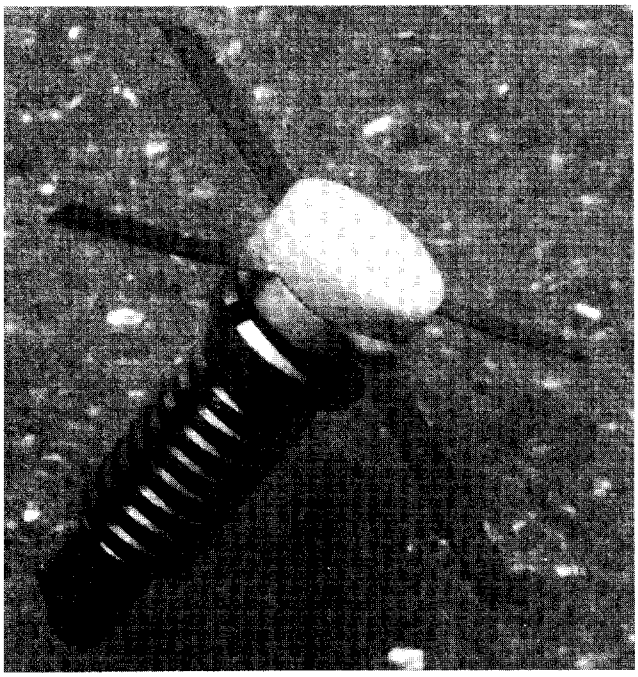

Figure 4. The Beryllium oxide XO72 package.

To achieve the goal of an overall gain of 20 dB, it appears that either combination of amplifiers A/C or B/C would have sufficed. The problem is that the XO72 package is substantially larger, for heat dissipation requirements, than the standard MMIC packages, and thus requires longer bond wires.

The longer associated bond wires have a deleterious effect on gain when used to connect the ground pads of the Darlington MMICs to the package ground; their effect would be more negative feedback. The longer bond wires together with the extra length in the screened ground lead would reduce the overall gain of a B/C combination. In fact, a computer simulation in which we included a simple model of the bond wires and the parasitic package capacitance showed that the gain performance would fall below the desired 20dB. While this combination had adequate power handling capabilities; (i.e., a +17 dBm amplifier driving a +23 dBm device) it fell short on gain. Moreover, the alternate A/C combination had the opposite problem, suffi-

cient gain, even with package parasitics, but insufficient power.

A consideration of the cascaded hybrid amplifier's characteristics led us to investigate the relationship between the 3rd order intercept point and the -1 dB power compression point of a Class A amplifier. This resulted in the two properties being related as shown below.

$$Pi = P1dB + 10.6\ dBm$$

where Pi is the third order intercept point and P1db is the 1 db gain compression point. Predicting Class A cascaded amplifier performance is shown in Appendix A along with some numerical examples.

The solution to this problem illustrates the design complexity that would otherwise fall to the user were a cascaded amplifier part not available and the user were required to realize one by combining available single stage parts such as these.

The A/C combination has sufficient gain but is marginal on power. A solution to this problem is to increase the output power of the first stage by raising the bias point, allowing a larger dynamic current swing. This is workable only if increasing the device current does not significantly lower the Ft or raise the junction temperature of the device to an unacceptable level. Since the A amplifier was originally designed for use in an alumina package, whereas the new cascaded amplifier will be housed in the XO-72 beryllium oxide package, a much lower overall thermal resistance will be realized. Thus the die can handle a higher collector current. Furthermore it was found that increasing the output transistor current from 45 to 60 mA actually improved the cutoff frequency (Ft). Accordingly, the 1 dB power compression point could be increased to achieve the power margin needed.

The choice of gain stages is affected by whether the cascaded amplifier will be realized as a hybrid or a monolithic integrated circuit.

From both theoretical and empirical evaluations the A/C combination was found to be more suited to the 20 dB gain/+20 dBm power goal than the B/C combination. Figure 5 shows the broad band power gain performance of the A/C combination, which is in excess of 20 dB at 1.0 GHz. The frequency response of the hybrid amplifier's -1dB power compression point (> +20 dBM a 1.0 GHz) is represented by Figure 6. Additionally, the overall amplifier noise figure is lower for the A/C compared to the B/C. Figure 7 shows the noise figure response of the A/C amplifier, henceforth designated the hybrid amplifier.

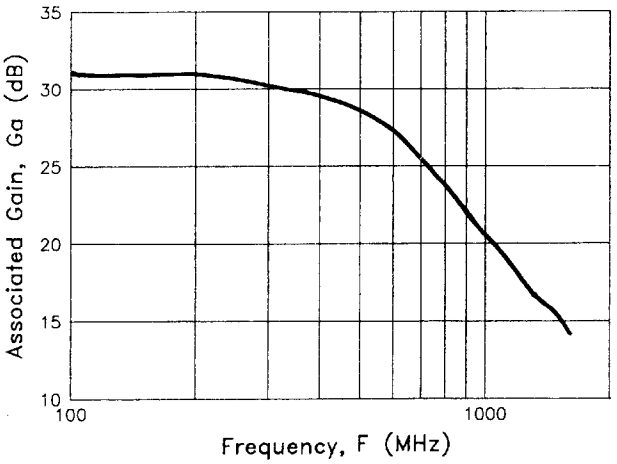

Figure 5. Hybrid amplifier associated gain versus frequency.

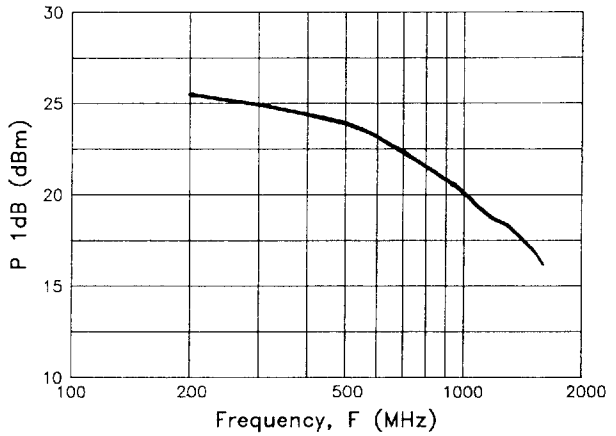

Figure 6. Hybrid amplifier 1dB power compression point versus frequency.

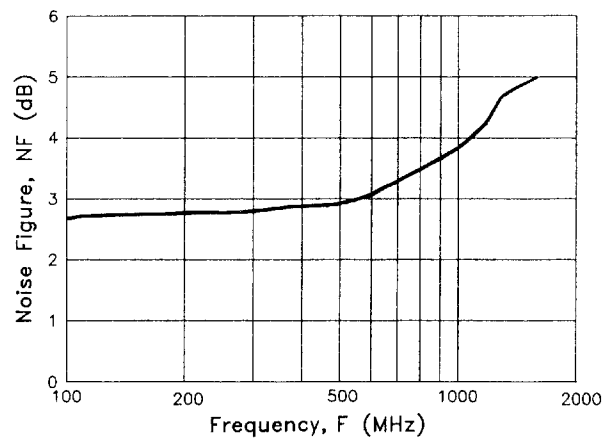

Figure 7. Hybrid amplifier noise figure versus frequency.

At this point it is appropriate to note that intermodulation test definitions differ between military and commercial applications. According to the military standard (Ref 2,) (1131 A-2204B), the distortion products are referenced to one of the two tones of the test signal. However, for the commercial EIA standard, such as EIA 19 (Ref 2), the amplitudes of the distortion products are referenced to the peak envelope power, which is 6 dB higher than the power of either of the two tones. Thus for example, an amplifier that meets the military IMD spec of -30 dB is equivalent to an EIA IMD spec of -36 dB. In terms of IMD, we choose to specify according to the more conservative military standard, approximately 31 dBm for this hybrid amplifier.

For the monolithic approach, which would be totally repackaged, we choose the B/C combination to better ensure sufficient output power margin. The output transistor of the B amplifier (a Darlington pair stage) has been increased in size to achieve increased power capability. The bias resistor (Rbias1) across the base emitter junction of the output device was changed, (reference Figure 2), to bias the Darlington pair to the same designed current point at approximately 9 volts. In addition the emitter resistor (Re1) was optimized for bias stability, power capability, and gain.

The pitch of the emitter fingers of the C stage design was decreased for the monolithic design, resulting in a reduction in the base area. This reduces the collector base capacitance, which in turn increases Ft and with it the gain.

Also, the bias point is shifted to operate from an internal 9 volts, rather than 12.5 Volts. The B/C combination is potentially low on gain; therefore, the emitter resistor (Re2) of the C stage is further reduced to increase the gain of this stage. As these designs require a specific operating current, a dropping resistor is used to approximate a constant current source with a voltage supply. This means that this monolithic version will be ideally suited to operate from a 12 volt external supply.

Process Description

The fabrication of silicon MMICs has evolved into a cost effective solution for many RF and IF applications. A variety of circuit elements can be fabricated concurrently with the active device structures. The design of circuits with complex silicon MMICs can increase system manufacturability, performance, and reliability over printed circuit or hybrid integrated circuit approaches.

A fully ion implanted device fabrication sequence is used to produce devices with an Ft in excess of 10 GHz. This device profile is incorporated into a fine line interdigitated transistor structure.

The process uses 1.0 micron metal fingers and spaces, which produce a device with a 4.0 micron emitter-to-emitter pitch. The fine line emitter and base openings are less than one half micron (typically 0.4 microns), which produce low emitter base junction capacitance and allow an increased frequency of operation. Utilization of these structures produces a high packing density which can be expressed as the emitter periphery to base area which is equal to 0.43/micron (11/mil). The higher this ratio, the lower is the associated collector base junction capacitance for the required emitter periphery.

A high ratio of the emitter periphery to base area of a transistor results in a design with low collector base junction capacitance.

The resistors of the circuit are fabricated using ion implanted LPCVD polycrystalline silicon which allows precise control of their values. Additionally, the fabrication of resistors with different resisitivity properties is easily achieved with the use of selective implantation. Film thickness and doping levels in the polycrystalline silicon can be varied to achieve a desired current density through the resistor, which is not possible with the use of thin film metals. This is important because high current density in metal films directly reduces device reliability and operating life.

A refractory barriered/gold metallization promotes high reliability. The system that we use was life tested under accelerated RF operating conditions, indicating a projected mean-time-to-failure (MTTF) of more than 1 million hours at a junction temperature of 200 degrees Celcius. All contacts to the silicon areas of this MMIC amplifier use this metallization, to yield the same expected reliability.

Refractory/gold metallization promotes a mean time to failure expectation of one million hours at 200C.

Collector isolation is achieved using a trenched epitaxial structure with air bridge interconnects. A cross section of this is shown in Figure 8. Additionally a parallel technique which uses undoped polysilicon to refill the trench is being investigated. The reduced dielectric constant of this material will be contrasted against the advantages of planar processing which it provides. The substrate of the chip is eutectically mounted to the ground plane and collector contacts for the individual n-type epitaxial regions are brought to the surface.

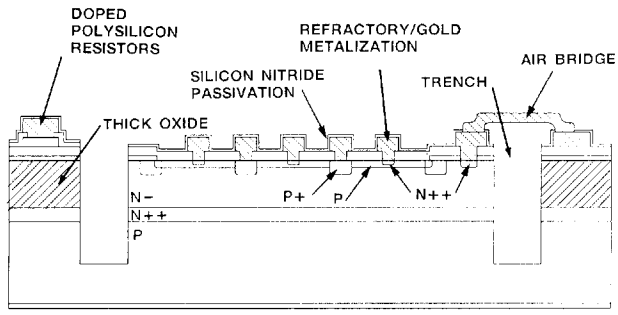

Figure 8. Cross section of isolated collector structure.

Device Layout

The layout of a full monolithic two stage Darlington was accomplished after taking into account various electrical and thermal considerations. Minimization of the thermal effects due to the power dissipated in the output device was achieved by splitting the device into two halves. Resistive finger ballasting to the emitter sections was used to provide current sharing in the output devices; this improves thermal stability. The addition of resistance in the emitter causes a proportional voltage drop to areas which demand increased current due to a localized temperature rise that, uncompensated, could result in thermal runaway and device damage. This distributed resistance tends to equalize current, minimizing hot spots across the active device areas on the chip.

The final monolithic amplifier, with two Darlington pair stages, will fit on a chip only 20 x 30 mils.

A die size of 500 x 600 microns (about 20 x 24 mils) was chosen to allow assembly in a 200 mil diameter, BeO, hermetic solder sealed package. A package of this type can support screening to all of the various quality assurance levels required for electronic amplifier applications.

References
1. Maas, Stephen, Non-Linear Microwave Circuits, Artech House 1988, pp 171-172.
2. Hawkins, Ricky E, PE, "Combining gain, noise figure and intercept points for cascaded circuit elements," RF design March 1990, pp 77 - 81.
3. Granberg, Helge, "Measuring the intermodulation distortion of the linear amplifiers," Motorola application note EB38.
4. Portions of this paper where described by the authors in the paper presented at the 1991 RF Expo East entitled "Silicon MMIC amplifier hits the 20/20 gain/power(dBm) mark at UHF."

Mr. Green *received his B.S. degree in Electrical Engineering from the University of British Columbia, Canada, in 1985 with specialization in RF and semiconductor physics. While at U.B.C. he worked in the C.A.T.V and Satellite receiving industries. In 1985 he joined the RF power amplifier group at Novatel Cellular Communications, and was awarded two patents on RF power detectors for AGC circuits. Other areas of his research include RF non-linear active and passive device simulation. He has been associated with device characterization for the Silicon MMIC team at SGS-Thomson Microelectronics since 1990.*

Mr. Osika *received his B.S. degree in Electrical engineering from Drexel University in 1985 with concentration in semiconductor device physics and computers. While at Drexel he worked at the U.S. Army Satellite Communication Div. in Fort Monmouth, New Jersey. In 1985 he joined Microwave Semiconductor Corporation and has worked on transient and steady state temperature modeling, automated testing, life testing, and power device design of BJTs and Static Induction Transistors (SITs). In 1989 he joined the Silicon MMIC group, then recently formed, to provide device design and modeling. SGS-Thomson Microelectronics acquired MSC in 1990 and he has continued in the development of a collector isolation process for silicon MMICs.*

APPENDIX A:

One way to find the cascaded 1 dB compression point is to find the cascaded intercept point and subtract about 10.6 dB to find the compression point. A worst case assumption is made that the distortion products will add in phase yielding the 3rd order cascaded intercept point for two stages from (Ref 1 & 2)

$$I_p^{(3)} = -10 \log \left[\frac{1}{i_1 g_2} + \frac{1}{i_2} \right]$$

WHERE

$i = 10^{[I(dBm)/10]}$ to convert from dBm to linear.

$g_2 = 10^{G_2/10}$ and

G_2 is the gain of the output stage dB.

i_1 is the output intercept point of the first stage.

i_2 is the output intercept point of the second stage.

NOTE:

Variables with capital letters have units in dB and dBm.

Variables with small letters have linear units; i.e., watts.

Another way to use this equation is to take the output intercept of the first stage (i_o) and input intercept (i_i) of output stage to find the interstage intercept I_{INT}.

$$I_{INT} = -10 \log \left[\frac{1}{i_o} + \frac{1}{i_i} \right]$$

The interstage intercept point can be added to the ideal gain of the output stage to obtain the output intercept point $I_p^{(3)}$

$$I_p^{(3)} = I_{INT} + G2$$

However, what we really want is the cascaded compression point. As there is only a fixed offset between the 3rd order intercept point and 1 dB power compression point, we can use the same interstage approach for the 1 dB point as well. Therefore, the effective interstage compression point is

$$P_{1dB\ INT} = -10 \log \left[\frac{1}{p_i} + \frac{1}{p_o} \right]$$

WHERE

$P_i = P_2 - G_2$ in dBm

P_i is the input 1dB compression point of the output stage (dBm)

G_2 is the gain (in dB) of the output stage

P_2 is the 1dB compression point of the output stage (dBm)

p_o is the linear output compression point of the first stage (mw)

p_i is the linear input compression point of the second stage (mw)

Then the combined 2 stage compression points is

$$P_{1dB} = P_{1dB\ INT} + G_2$$

For example, a two stage cascaded amplifier has an input stage capable of 14dB gain and 14dBm P1dBm compression point. The output stage performance is 8.5dB gain and 23dBm P1dB

Then the input compression point of the output stage can be shown to be

$$+23 \text{ dBm} - 8.5 \text{ dB} = +14.5 \text{ dBm}$$

$$p_i = 10^{14.5/10} = 28.18$$

$$p_o = 10^{14/10} = 25.12$$

The interstage compression point is

$$P_{1dB\ INT} = -10 \log \left[\frac{1}{25.12} + \frac{1}{28.18} \right]$$

$$= +11.23 \text{ dBm}$$

Therefore the overall 1 dB power compression point of the two cascaded amplifiers is

$$P_{1dB} = +11.23 + 8.5 = +19.7 \text{ dBm}$$