

Electronically Tuned L-S Band Filters

The authors describe active tunable Gallium Arsenide filters built as 3.1 x 1.6 mm monolithic integrated circuits using 1 micron geometry obtainable in most foundries. The filters cover the 1.34 to 2.2 and the 1.84 to 2.7 GHz bands with -3 dB bandwidths of about 5 percent.

V. Aparin
P. Katzin
*Hittite Microwave Corporation
Woburn, Massachusetts*

Separate, 3-section band-pass filters covering the 1.34-2.2 GHz and 1.84-2.7 GHz bands, with -3 dB bandwidths of 86 ± 6 MHz and 126 ± 10 MHz, respectively, and matched closed-loop control circuits are described in this paper. The filters and control circuits are both fabricated using a standard 1 micron GaAs MESFET foundry process.

The control circuits generate filter tuning and Q-control bias voltages by tracking a sub-harmonic reference signal. The circuits automatically maintain the filter insertion loss to within ± 0.5 dB over more than a 1.3:1 frequency-tuning range, and regulate the center-frequency and insertion loss to within better than ± 1.2 MHz and ± 0.3 dB over a temperature range of -50°C to $+75^\circ\text{C}$.

Background

The integration of narrow-band filters in MMIC form offers the attractive advantages of small size and tunability. A further advantage is the integration of such filters with some other functions such as amplification and frequency conversion. This allows a complete module (for example, a microwave receiver) to be fabricated

as a single chip resulting in a further size/cost reduction.

To compensate passive components losses that are relatively high in MMIC implementation, several Q-enhancement techniques have been used in filter design[1-5]. These techniques allow to achieve 0 dB passband insertion loss by introducing negative resistance in filter resonators. Unfortunately, such a Q-enhancement makes MMIC filter performance very sensitive to fluctuations in operating temperature and fabrication process. The filter passband insertion loss becomes very inconsistent over a tuning range without external adjustments.

A further design challenge is that narrow bandwidth filters intrinsically need accurate center-frequency control. To our knowledge, none of the published active MMIC filters have been designed to provide stable passband characteristics without external manual adjustments. This is accomplished here for an active 3-section band-pass filter design through using a closed-loop, master-slave control circuit[3, 6]. This circuit generates and automatically adjusts Q-factor and frequency control bias voltages by tracking a frequency reference signal, resulting in a self-adjusting filter.

In this paper, we present a monolithic implementation of such a control circuit with all its active components integrated on a single MMIC chip. The filter and control ICs were mounted in a common 0.27 x 0.27 x 0.07 inch package, thereby providing by far the most compact reference-tracking microwave filter circuit ever reported.

Filter Circuit Design

The basic topology of the band-pass tunable MMIC filters is shown in Figure 1. It uses three lumped-element LC resonators with Q-enhancement. Filter tuning to the desired center-frequency (f_0) is accomplished through varying the shunt capacitors in the resonators. This type of capacitively-coupled multi-section band-pass filter topology is well suited for MMIC integration but, as can be seen from previous work[4], its 3 dB bandwidth increases roughly as $f_0^{3.5}$ unless coupling elements C_{i_0} and C_c are tuned in unison with the resonator capacitors C_a and C_b .

At the outset it was desired to maintain relatively constant filter bandwidth and ripple characteristics over the tuning range. To achieve this, it can be shown that capacitors C_a , C_b , and C_{i_0} must be tuned together with approximately linear proportionality, whereas inter-resonator coupling capacitors C_c must vary in proportion to

$C_a^{1.5}$. For a single tuning voltage, a good approximation of this function is obtained by implementing C_a , C_b , and C_{i_0} using an appropriate combination of fixed and electronically variable capacitances, the latter realized using varactor diodes.

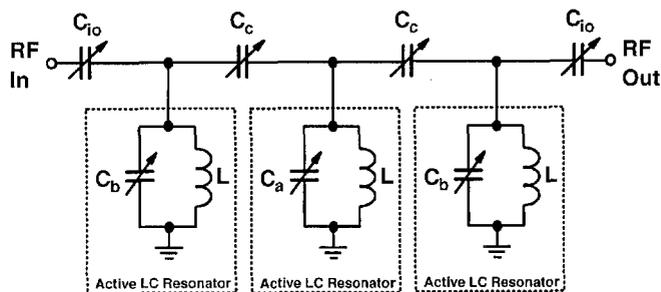


Figure 1. Basic topology of the 3-section tunable band-pass filter.

A schematic of the active filter sections is shown in Figure 2. The FET T_1 in conjunction with the inductor pair L_1 - L_2 generates a negative resistance. This resistance is adjusted by adding a small amount of loss through the FET T_2 that operates as a voltage-controlled resistor. A triple-gate device was used for this FET to enhance its linearity at high signal levels. The inductor pair L_1 - L_2 was implemented as a single tapped coil, to minimize loss and save space.

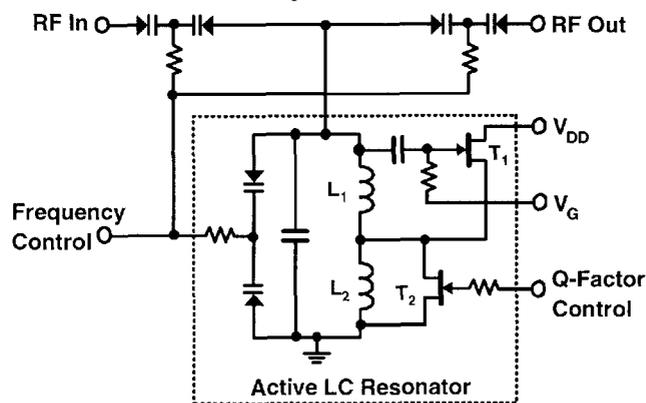


Figure 2. Simplified schematic of active band-pass filter sections.

Equalization networks (not shown in Figure 2) were also included in the circuit to reduce the passband gain slope, due to the frequency-dependence of the negative resistance. All varactors were configured as antiparallel diode pairs to minimize distortion under large-signal conditions. The diode peripheries were scaled for each of the different capacitive elements shown in Figure 1. Thin-film capacitors in conjunction with the parasitics associated with the inductors and FETs in each resonator were used to approximate the desired proportionality between the C_c elements and other tuning capacitors.

We designed separate MMIC filter chips to cover frequency ranges of approximately 1.5-2.0 GHz and 2.0-

2.6 GHz. Drain-supply and bias control-line decoupling networks were included on-chip to reduce the number of external components required and minimize spurious responses.

Filter Control Circuit Design

Separate control circuits were designed to match each of the two filters. The purpose of the control circuits is to generate control bias voltages for the matched filters and automatically adjust these voltages to maintain 0dB passband insertion loss and stable center frequency of the filters in the presence of temperature variations and process tolerance. This is achieved by using the master-slave control scheme shown in Figure 3.

Each control circuit contains a master voltage-controlled oscillator which is identical to a slave filter section. This means that the pole frequency of the master oscillator is equal to the slave filter center frequency. The master VCO is also isolated from any significant external losses so its Q-factor is equal to the unloaded Q-factor of the slave filter sections. To achieve harmonic oscillations with a constant amplitude, the master oscillator Q-factor should be infinite. An infinite unloaded Q is also required for the slave filter sections to provide 0dB passband insertion loss. An appropriate Q-control voltage for both the slave filter and master oscillator is generated by the gain (negative resistance) control loop. This loop limits the oscillation amplitude at a level low enough to ensure small-signal characteristics of the master oscillator active devices and tuning varactors.

A PLL locks the oscillation frequency (f_{osc}) of the master oscillator to a sub-harmonic frequency (f_{ref}) of an external reference signal generated by a stable crystal oscillator so that $f_{osc} = f_{ref} \times N$, where N is the division ratio of the frequency dividers used in the PLLs (N=28 for the L-band control circuit and N=40 for the S-band control circuit). The frequency control voltage generated by the PLL is also applied to the slave filter so that its center frequency is equal to the locked oscillation frequency of the master VCO.

The use of sub-harmonic reference signals in the VHF frequency range allows the control and filter circuits to be mounted in a common package without introducing excessive levels of in-band spurious signal leakage. Also, the lower reference signal frequency enables use of a digital phase-frequency detector (PFD) in the frequency control loop, providing much better pull-in characteristics than the diode mixer phase detector used previously [3].

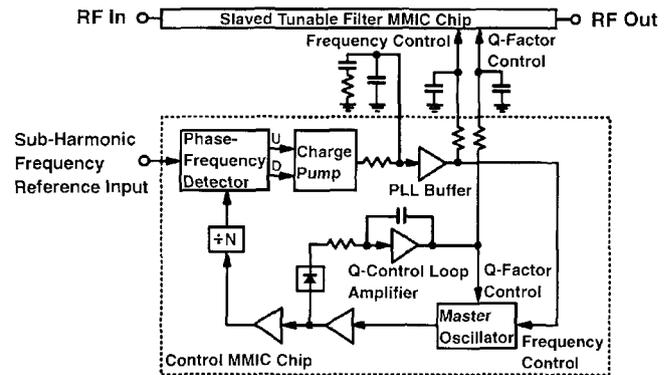


Figure 3. Block diagram of the dual-loop master-slave filter control scheme.

As illustrated in Figure 3, all active components for each control circuit were integrated on a single MMIC chip including: the master oscillator, RF amplifiers, an amplitude detector and operational amplifier for the Q-control loop, digital dividers, a PFD with charge-pump output driver and source-follower buffer for the PLL. A few resistors and capacitors are required off-chip for supply bypassing, the PLL low-pass filter, DC bias adjustment, and control-line filtering.

The digital $\div 28$ and $\div 40$ divider circuits were implemented using source-coupled FET logic (SCFL) static flip-flop cells developed by the GaAs IC foundry. A higher frequency dynamic $\div 2$ prescaler circuit, similar to that described in [7], was used as the front-end of the $\div 40$ design. The PFD and charge-pump output driver circuit designs are described in another paper [8]. The filter and control circuits were designed to operate with ± 5 V supplies.

Fabrication

Both the filter and control GaAs MMICs were fabricated using a 1 μm gate-length E-D MESFET foundry process with via-hole grounds. The varactor diodes were realized using MESFETs with -2 V nominal pinchoff, by connecting their source and drain electrodes together. Figures 4 and 5 are pictures of the 2.0-2.6 GHz band-pass filter and filter-control MMIC chips, respectively. The picture in Figure 6 shows the two chips mounted in a 10-lead kovar-base package measuring only 0.27 x 0.27 x 0.07 inches (excluding leads) together with some of the off-chip passive components discussed above.

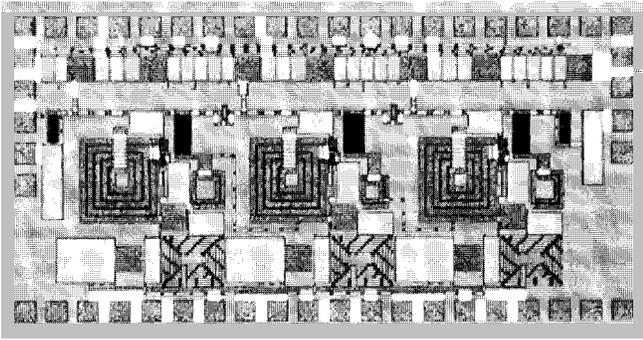


Figure 4. Photograph of the three-section band-pass filter MMIC. Chip dimensions are 3.1 x 1.6 mm.

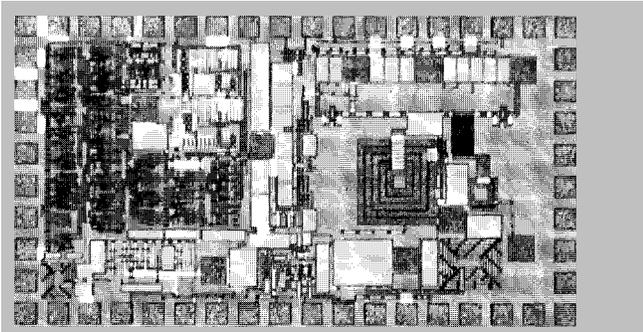


Figure 5. Photograph of the MMIC control circuit. Chip dimensions are 2.8 x 1.6 mm.

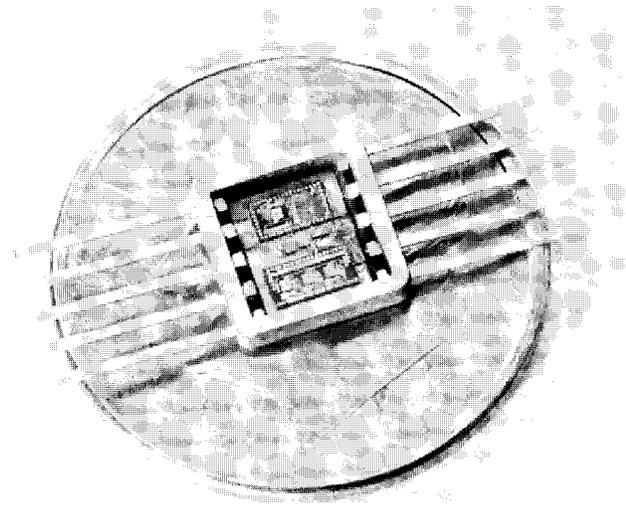


Figure 6. Photograph of the filter and control MMICs mounted in a common package.

Measured Performance

The two band-pass filter MMIC chips were initially evaluated in a test fixture with a Q-control voltage adjusted manually to achieve a mean passband insertion loss of 0 dB for a given frequency control voltage. The measured maximum tuning ranges of the low- and high-band filters are 1.34-2.2 GHz and 1.84-2.7 GHz, respec-

tively. The rest of the measured results presented here were obtained for the filters slaved to the matched control circuits mounted in the same package (Figure 6). The filter tuning range in this configuration is determined by the capture range of the PLL used in the matched control circuit. This range is 1.5-2 GHz for the low-band filter and 1.96-2.64 GHz for the high-band filter.

Figures 7 and 8 show measured transmission responses of the low- and high-band filters, respectively. The corresponding f_0/N reference signal frequencies are 54, 60, 66, and 72 MHz for the low-band filter and 49, 54, 60, and 66 MHz for the high-band filter. The -3 dB bandwidths over the closed-loop tuning ranges are 86 ± 6 MHz and 126 ± 10 MHz for the low- and high-band circuits, respectively, which corresponds to less than $\pm 8\%$ variation. The control circuits maintain the mean passband insertion loss to within ± 0.5 dB at each tuning frequency. Passband ripple is better than 0.6 dB over the tuning range of each filter.

Figure 9 demonstrates return losses of the high-band filter. A transmission response of the same filter over a broad frequency range is shown in Figure 10. Out-of-band rejection is better than 40 dB up to 9.5 GHz and better than 28 dB up to 26 GHz for both filter chips. Figure 11 indicates the response of the high-band filter over a -50 C to +75 C temperature range, with a 55 MHz reference signal. It can be seen that the control circuit maintains the center-frequency and passband insertion loss to within better than ± 1.2 MHz and ± 0.3 dB, respectively, over this temperature range.

The passband output signal power level for -1 dB gain compression is about +1 dBm for both filters over their closed-loop tuning ranges. The minimum noise figures are 17 dB and 18 dB for the low- and high-band filters, respectively. The total, double-sideband, transmission phase-noise introduced by the high-band filter and control circuits is -100 ± 5 dBc/Hz at 1 KHz offset over the tuning range. In-band master oscillator signal feedthrough is less than -80 dBm and -76 dBm for the low- and high-band circuits, respectively. The measured tuning speed of these self-adjusting filters is better than 10 μ s (to within 2° of steady-state transmission phase) for frequency-hop spans up to the full closed-loop tuning range. This speed could be improved by about an order of magnitude by modifying the designs of the bias control-line decoupling networks and of the PLL buffer. DC power consumptions of the filter and control MMICs are 0.3 W and 0.6-0.7 W, respectively.

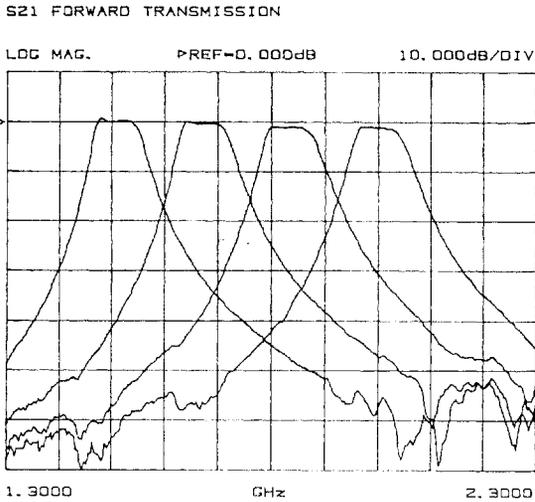


Figure 7. Transmission responses of the low-band MMIC filter slaved to a matched control MMIC in the same package.

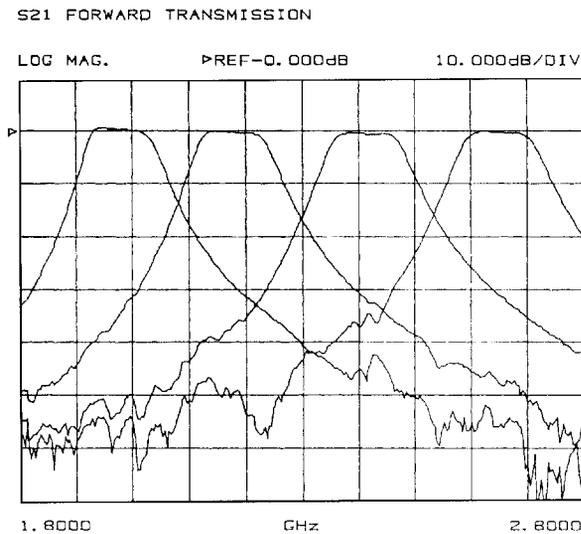


Figure 8. Transmission responses of the high-band MMIC filter slaved to a matched control MMIC in the same package.

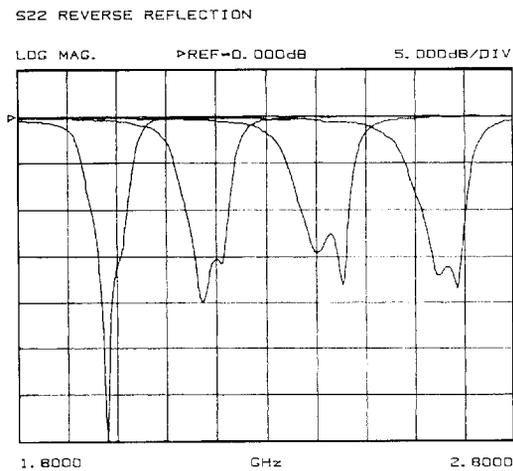


Figure 9. Return-loss responses of the high-band MMIC filter slaved to a matched control MMIC in the same package.

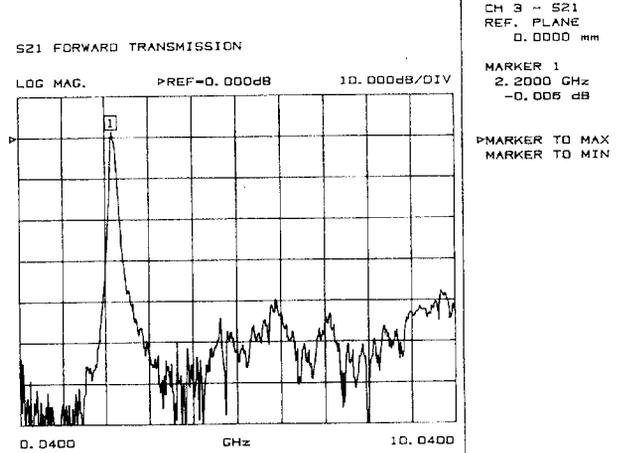


Figure 10. Out-of-band rejection performance of the packaged high-band filter.

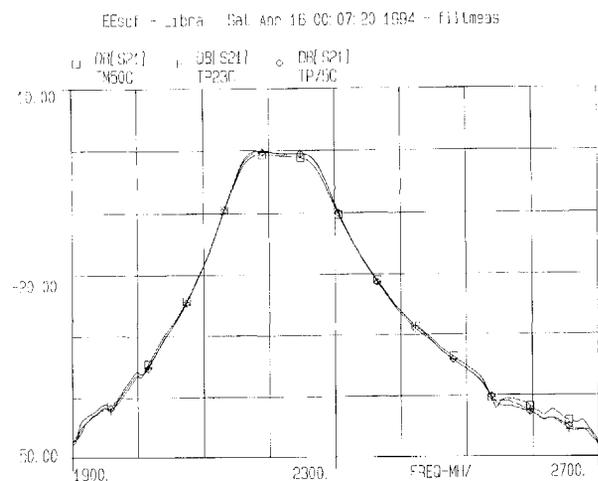


Figure 11. Response of the packaged high-band MMIC filter/control circuits over temperature.

This work demonstrates the feasibility of MMIC integration of tunable band-pass filters with stable passband characteristics over greater than 1.3:1 frequency-tuning range in the L-S microwave band, using a standard 1 μ m GaAs foundry process. This could be an enabling approach in the design of systems for which both small circuit size and filter tunability are essential.

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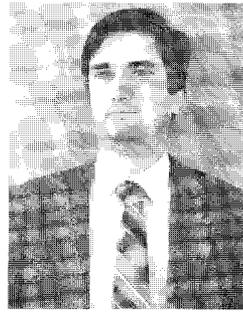
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Vladimir Aparin, born in Tula, Russian Federation in 1966, received the Diploma Degree in Electronics and Automatics with honors from the Moscow Institute of Electronic Engineering (MIEE) in 1989.

In 1987 he joined the GaAs IC Design Group at the MIEE where he was involved in the design and testing of high-speed GaAs ICs for measurement equipment, in device modeling and characterization. Since 1992 he has been with Hitrite Microwave Corporation, Woburn, MA, where he is engaged in the design and development of GaAs MMICs for communication systems.

Vladimir Aparin is a coauthor of one USSR patent and several technical papers.



Peter Katzin received a BS Degree in Physics and Electrical Engineering from the University of Manchester, England in 1979. He received a MEng Degree in Electrical Engineering in 1983 at Cornell University where he designed, fabricated and characterized a low noise KU-band GaAs MESFET amplifier.

From 1980 to 1981 he contributed to the design and testing of the Attitude Control and the microwave Command, Tracking, and Ranging systems of communication satellites at Hughes Aircraft Company, Space and Communications Division. He joined the Research Division of the Raytheon Company in 1983 where he participated in the evaluation, design, and CAD modelling of GaAs MMIC components and circuits. He was program manager for a 44 GHz MMIC power amplifier program and high-efficiency S-band MMIC switching power amplifier program.

In 1987 he joined Hitrite Microwave Corporation, where he has managed several programs aimed at MMIC implementations of tunable filters, wide band circulators, and high-power switches. He also works in the development of communication and ranging systems based on MMIC technology. He is a member of IEEE and author/contributor of several technical papers.