2-6 GHz Commercial Power Amplifier

This unique amplifier uses lossy matching networks for broadbanding, exceptional gain flatness, low input VSWR, high efficiency and small size. It achieves over 1 watt with 19dB of linear gain, input VSWR below 1.7, power- added efficiency of 25% and chip area less than 4.4mm2.

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There are numerous commercial applications for a power amplifier in the 2-6 GHz frequency range. These include sockets in radar altimeters, local area networks (LANs), microwave landing systems (MLS) as well as personal communication networks (PCNs) and various communication systems.

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In this paper we describe a 1 watt, broadband MMIC power amplifier design using lossy matching networks in the form of a bridged-T all-pass network. This approach offers the advantage of exceptional gain flatness, low input VSWR, high efficiency and small size. A two stage amplifier is described that delivers greater than 1 watt across the 2 to 6 GHz range with a linear gain of 19dB, an input VSWR below 1.7, a power-added efficiency of 25% and a chip area less than 4.4mm^2.

The key to the design is flat gain and good input match.

In broadband power amplifier design, a key element is maintaining flat gain over the band while achieving a well matched input (good input VSWR). Commonly this is addressed using the balanced amplifier approach, whereby the input is reactively matched for gain sloping (equalization) and quadrature couplers provide a good match when two similar amplifier stages are placed between them. Although very common in hybrid microwave integrated circuits (MICs), the quarter wavelength size of the couplers is usually not practical for monolithic MICs (MMICs).

Another approach often used with MMICs is the distributed amplifier having the advantage of large bandwidth, excellent gain flatness and low input VSWR. But it has low gain, low efficiency and requires a relatively large chip size.

The approach uses lossy matching networks that absorb the MESFET capacitance into a simple filter network.

This paper describes the use of lossy matching networks that absorb the MESFET input capacitance into a simple filter network to provide simultaneous gain flatness, good input and interstage match for a two stage, GaAs MMIC, power amplifier, an approach previously used for input matching and gain equalization of low level amplifier stages [1,2,3].

Theory

The second-order all-pass network with its normalized element values is shown in Figure 1 [3,4]. Figure 2 shows a simplified linear MESFET model. Neglecting Ri, Cds and taking into account Miller Effect, we obtain the further simplified model of Figure 3, wherein Cin is the equivalent input capacitance and RL is the load impedance presented to the FET stage.

Combining the Figure 3 circuit with that of Figure 1, and using Cin as C2 we obtain the all-pass matching network of Figure 4. This network provides a broadband resistive match as well as gain equalization up to the frequency of f1. Although

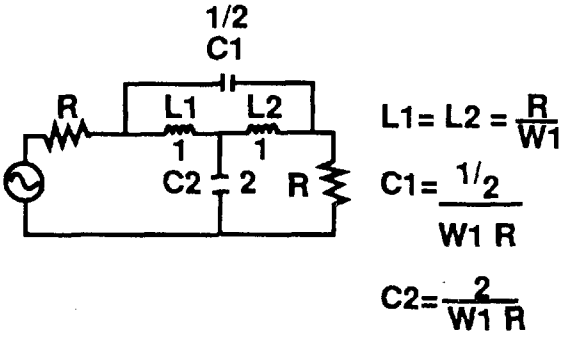

Figure 1. Second order all-pass network.

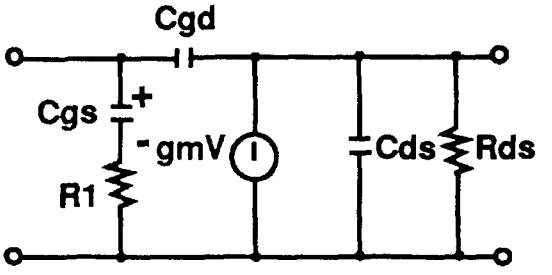

Figure 2. Simplified MESFET Linear Model.

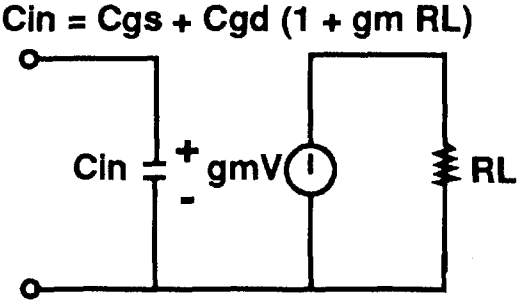

Figure 3. Further simplified model with equivalent input capacitance.

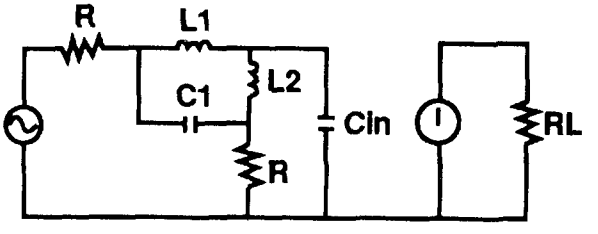

Figure 4. All-pass filter matching network.

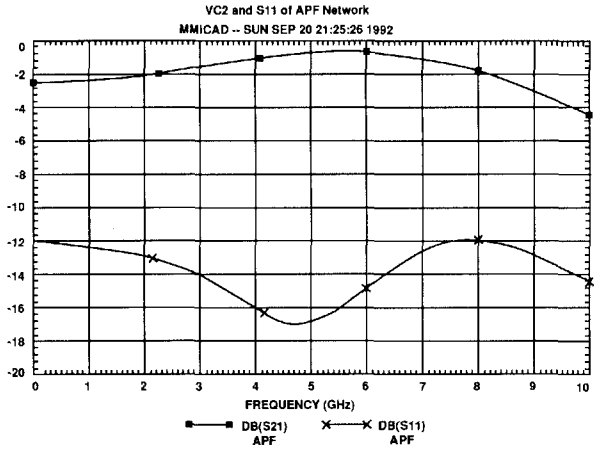

Figure 5. Gain compensation and impedance match of 1.2mm FET using all-pass network.

the all-pass network itself has a flat amplitude response with no real cutoff frequency, the voltage across C2 (or Cin) however does decrease above f1, the frequency of 180 degree phase shift.

This voltage directly corresponds to the linear gain of the FET stage, since this is the control voltage for the voltage controlled current source in the FET model. For a given Cin, f1 can be increased by reducing R. Figure 5 shows the gain compensation (voltage across C2) of a 1.2mm FET with R (at input of Figure 1) equal to 30 ohms.

Note the relatively flat amplitude response from DC to approximately f1 and the minimum return-loss of 12dB, corresponding to a mismatch of 30 ohms in a 50 ohm system. In some cases a higher cut-off frequency can be obtained with a compromise in input VSWR (as illustrated above), but for large periphery FET stages an additional impedance matching network must be used to transform up to the desired impedance level (Figure 6). Although this increases the circuit's complexity, the impedance matching problem is easier to treat than with the customary reactive match approach, since matching is between real impedances at the input and real to complex on the interstage rather than complex to real and complex to complex respectively. In addition, since gain compensation is achieved via the lossy network, simultaneous impedance match and uniform gain with frequency response is possible.

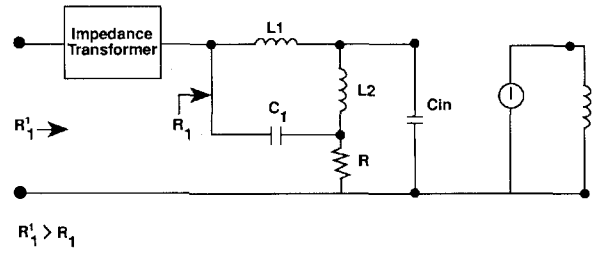

Figure 6. Matching approach for large periphery FET.

Design Example

Using this approach a two stage, 1 watt, 2-6 GHz amplifier was designed for the 0.5 micron MBE power process used within the foundry service offered by our firm in alliance with AT&T. The design employed the all-pass network on the input and a degenerate form in the interstage network (Figure 7).

To obtain the desired output power, two parallel 1.5mm FET cells were used for the second stage. To ensure adequate drive a 1.2mm cell was used as the first stage. The output network was synthesized from load-line considerations in a manner similar to that described in [5].

The input network was a direct application of the all-pass network realized with spiral inductors for both L1 and L2. The input impedance of 30 ohms was chosen to extend the frequency band beyond 6 GHz while providing a reasonably well matched input (return-loss of 12dB or better).

The interstage network design started as an all-pass network but during linear simulation and optimization using MMICAD [TM of OPTOTEK, Ltd.], it was found that the C1 element essentially went to zero, thereby degenerating into a low- pass filter topology. Analysis showed that the gain compensation (i.e. flatness of the voltage across C2 in Figure 1 or Cin in Figure 4) is essentially identical to that obtained with the all-pass form at low frequency and departs somewhat at f1, at which there is an increase in VSWR as the input becomes reactive (Figure 8).

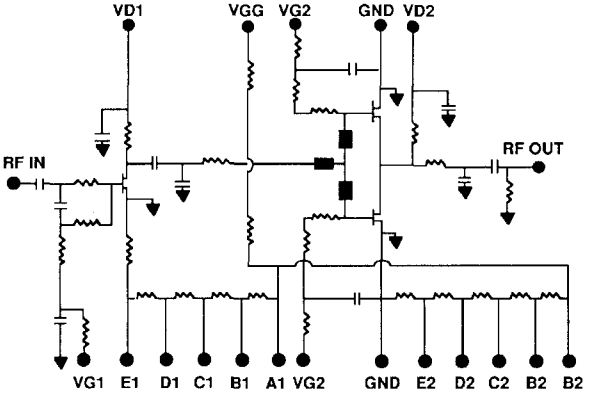

Figure 7. Simplified schematic of the Amplifier Chip.

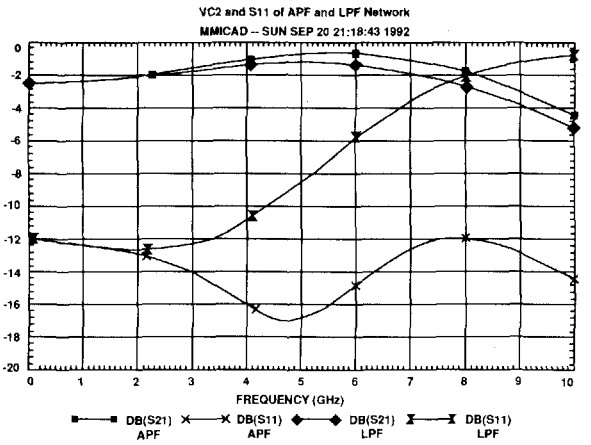

Figure 8. Comparison of all-pass network and low-pass network gain compensation and impedance match for 1.2mm FET.

With impedance matching, the two sets of responses would be very similar. The network is realized on each of the 1.5mm cells with a distributed line for L1 and a spiral inductor for L2. This was proceeded by an impedance transformer consisting of a high and low-pass section to raise the impedance presented to the output of the 1.2mm cell to about 45 ohms.

A final non-linear simulation and tuning was done using harmonic balance on LIBRA [TM, Essof Inc.]. Figure 9 shows the chip layout with a total chip area of less than 4.4mm2, which was made possible as a result of the simplicity of the matching approach.

Experimental Results

A MMICAD plot of simulated response compared with measured results for the linear gain and input VSWR is shown in Figure 10, revealing that theory and experiment are in close agreement. The measured linear gain was 19dB with a flatness of +/-1dB, and the measured input VSWR was below 1.7 across the full band.

Theory and experiment are in close agreement; linear gain of 19dB, flatness of +/-1dB and input VSWR below 1.7.

The output power and power-added efficiency, both simulated and measured under the condition of an input power of +15dBm, are shown in Figure 11, also demonstrating good agreement between theory and practice.

The saturated output power was greater than 1 watt, exceptionally flat within 0.5dB. The associated power-added efficiency measured about 25%, outstanding in view of the 3:1 operating bandwidth. These measurements were obtained with a bias of Vds = 9volts and Id = 40%Idss (450mA). To our knowledge this amplifier has the best performance with respect to the combination of power, flatness, efficiency and VSWR reported for this frequency band.

Saturated output power is over 1 watt, flat within 0.5dB; power added efficiency is 25% at 8V and 450mA; outstanding in view of the 3:1 bandwidth.

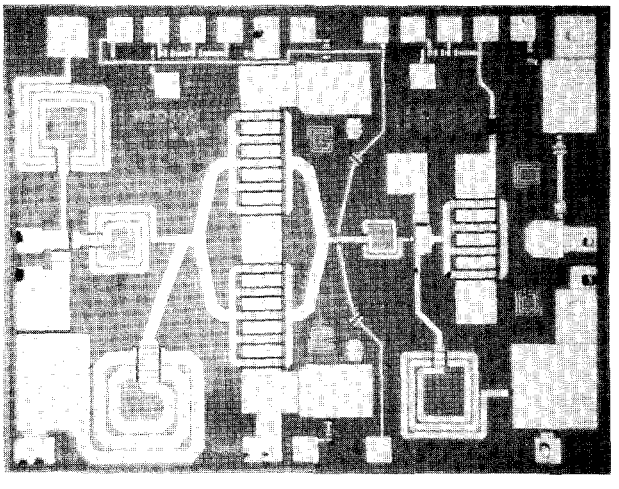

Figure 9. 2-6 Ghz, 1 watt amplifier chip.

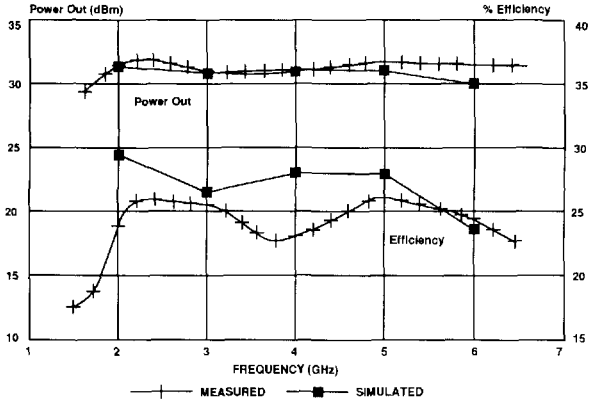

Figure 10. Measured versus simulated linear gain.

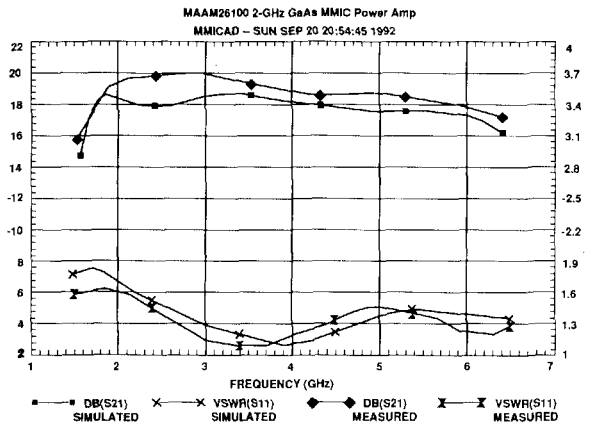

Figure 11. Measured versus simulated power output and power added efficiency.

Acknowledgments

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Thomas Arell *received the BSEE degree from Pratt Institute, Brooklyn New York in 1971 and the MSEE degree from Northeastern University, Boston Massachusetts in 1984.*

From 1971 to 1974 he was with Microwave Semiconductor Corporation in Somersett, New Jersey engaged in the design and development of numerous MIC L-band and S- band power amplifiers using silicon bipolar technology.

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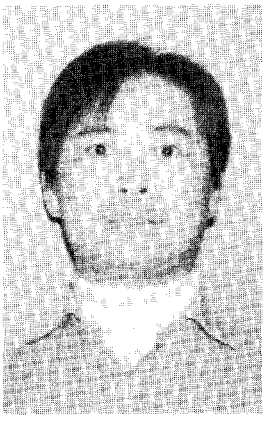
He joined M/A-COM in 1978 (then Microwave Associates) and has held key positions, developing MIC components and subsystems through 20 Ghz.

Since 1986 he has been focusing on MMIC design and presently is a Principal Engineer at M/A-COM's IC Design Center of the Microelectronics Division responsible for GaAs MMIC power amplifier development.



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Lucky came to IC Design Center from the Semiconductor Center of Adams-Russell Electronics, where he worked in GaAs MMICs. Before joining the Semiconductor Center he worked with subassemblies, phase modulators and logarithmic amplifiers at the Anzac Division of Adams-Russell Electronics.

He earned a B.S. in Electrical Engineering from the University of Lowell in 1984. He is a member of the IEEE and past vice-chairman of the IEEE student chapter at the University of Lowell in 1983-4.