Frequency Translation by Phase Shifting

If the phase of a carrier signal is changed linearly using a phase shifter -the result is similar to frequency modulation, except in this case the base frequency is preserved perfectly. The authors describe a 6-18 GHz serrodyne application achieving over 22 dB of carrier and spurious signal suppression.

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Frequency translation is utilized in military electronic countermeasure (ECM) applications to generate a false target signal, thereby to subvert the velocity related functions of a hostile radar system. Figure 1 shows Doppler frequency shifts observed at various carrier frequencies as a function of relative velocity of a moving target. For example, if the relative velocity of a target is 6000 feet per second (fps), or 4,091 mph (approximately Mach 5) then the corresponding Doppler frequency shift is about 73 kHz for a carrier frequency of 6 GHz, or 220 kHz for a carrier frequency of 18 GHz.

From the velocity deception point of view, let us assume that a target signal is returned to a hostile radar after 25 kHz of additional Doppler shift (up or down) to a carrier frequency of 12 GHz. This will introduce about ±1000 fps, or +/- 680 mph of uncertainty in the relative velocity of the target as indicated by an unsuspecting or *dumb* hostile radar system.

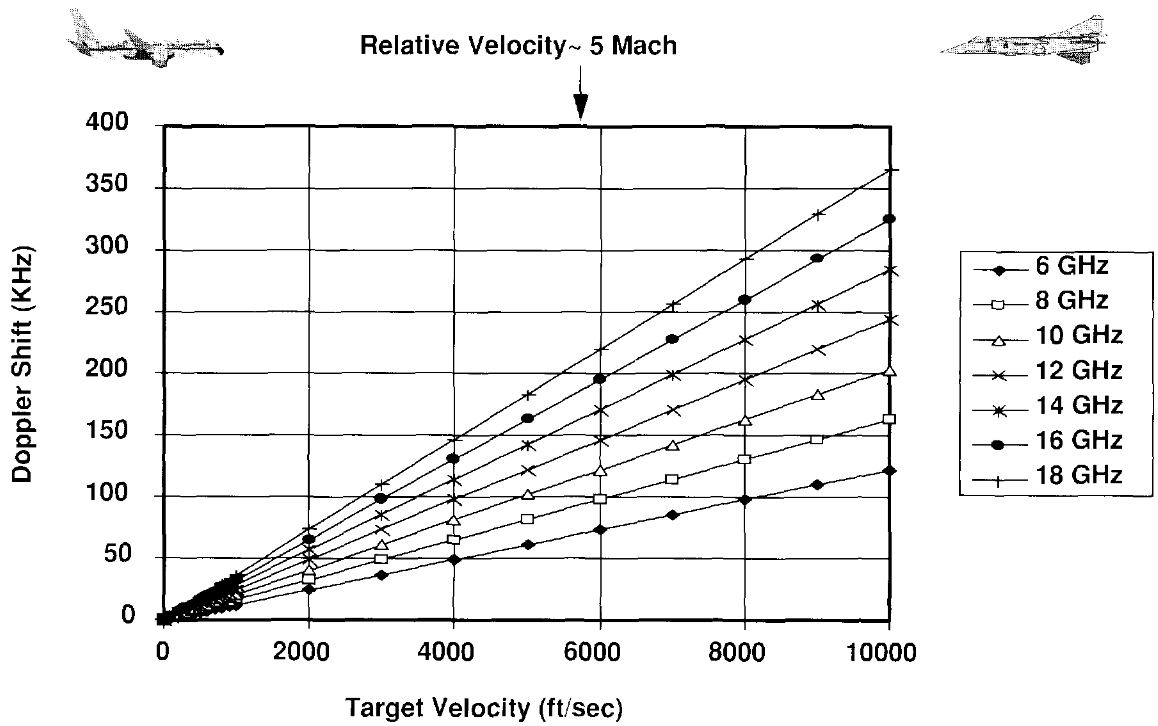


Figure 1. Doppler frequency shift versus target velocity for carrier frequencies from 6 GHz to 18 GHz.

A frequency translator device shifts up or down the frequency of an input signal by some desired amount (usually less than few hundred kilohertz). Ideally it provides output only at the shifted (translated) carrier frequency with minimum signal loss and, also ideally, without generating any spurious frequencies. In practice, as we shall describe, real translators perform with figures of merit described by how much the original carrier is suppressed and how low the spurious signals are kept.

In the first type, similar to a single sideband modulator (Figure 2), the translator may consist of a pair of balanced mixers located in phase quadrature and driven by a pair of quadrature modulation signals (at the desired translation, or deception) frequency. In this type of translator, due to the mixing process and also since translation frequencies are usually a very small fraction of the carrier signal, it is extremely difficult to suppress the unwanted sidebands to levels below 15 dB of the translated carrier level.

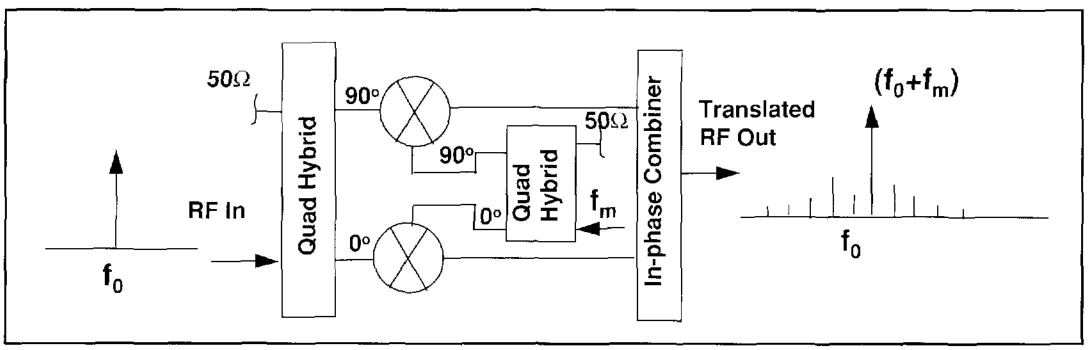


Figure 2. Mixer based frequency translator.

Basically, there are three types of frequency translators usually considered, using (1) mixers (2) analog phase shifters and (3) digital phase shifters. Actually the last class should be called binary phase shifters, because their increments are binarily related rather than to base 10, however the term digital phase shifter is used herein because it is the conventional terminology.

Translators using phase shifters are based on the principle of phase modulation. When the phase angle of an input RF signal of frequency f_0 is varied linearly with time (having a phase versus time slope corresponding to a frequency of f_m) then the frequency of the resultant output signal is *translated up* to (f_o+f_m) as depicted in Figure 3(a). It may be noted that for a negative slope of the phase function, the output frequency will be *translated down* to (f_o-f_m).

Ideal frequency translation can also be performed by using a periodic *sawtooth* phase function, which snaps back and repeats after a phase change of 360 degrees, as shown in Figure 3(b). This technique is also known as *serrodyne* frequency translation.

The best stepped approximation to the ideal 0 to 360 degree function is obtained with binary (equal phase) steps and equal time steps. This is achieved using cascaded phase shifter bits of 180, 90, 45, 22.5, 11.25 .... degrees.

For example, a 3-bit phase function corresponds to use of 180, 90 and 45 degree bits to approximate the 0 to 360 degree cycle by 8 steps of 0, 45, 90, 135, 180, 225, 270 and 315 degrees. Similarly, for 5-bit approximation there are 32 steps of 11.25 degrees each in the phase shift staircase.

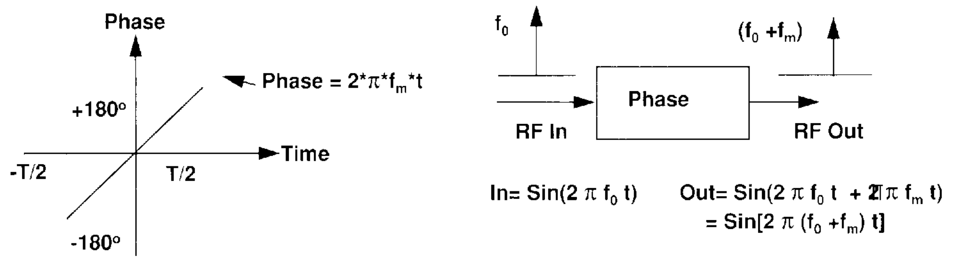


Figure 3(a). Linear phase function.

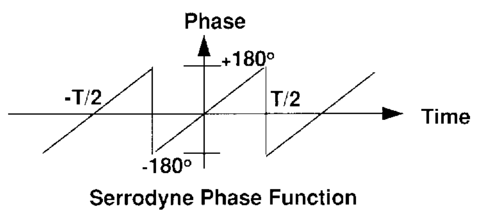


Figure 3(b). Serrodyne phase function.

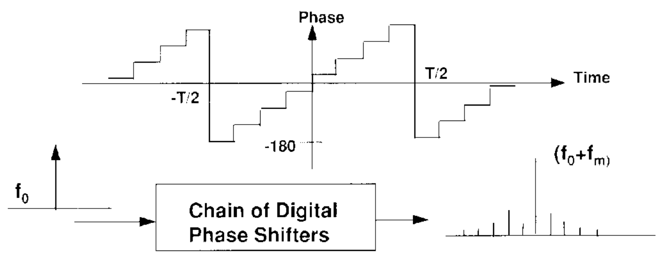


Figure 3(c). Staircase approximation of the serrodyne phase function.

Translators employing analog continuous 360 degree phase shifts are usually realized using varactor diodes. However this is impractical for a translator which must operate over a broad microwave bandwidth for two reasons. First, the junction capacitance of varactor diodes is a non-linear function of the drive voltage and, second, the phase change introduced by a capacitor in a microwave circuit is not itself a simple function of capacitance. Accordingly, we chose to use a digital phase shifting technique.

Practical digital frequency translators are realized using a cascade of binarily related phase shifters to approximate the desired continuous 0 to 360 degree sawtooth phase function by a stepped-phase shift *staircase* as shown in Figure 3(c). It can be shown by Fourier analysis that at least 3 phase steps (resulting in 120 degree equal steps) are required to achieve frequency translation with suppression of the carrier and first symmetrical sideband.

Characteristics of a frequency translator using phase shifters have been discussed [1-5] and performance reported over narrow bands. For example, over 7 to 11 GHz, spurious suppression of 22 dB was reported [3].

Frequency translators operating over the full 6 to 18 GHz countermeasure band have not previously been available. Furthermore, although effects of amplitude and phase errors on various spurious sideband levels have been discussed [1-4], a quantitative trade-off of the errors as a function of number of bits has not published.

In the following, trade-off of maximum amplitude and phase errors that can be tolerated, as a function of the number of bits, without exceeding the spurious levels (corresponding to the ideal, equal step and constant amplitude staircase) is provided. This is accompanied by a description of the performances over 6 to 18 GHz of the translator we realized as a 5-bit MMIC binary phase shifter.

The motives for the development of this MMIC based approach are

(1) A single module wideband 6 to 18 GHz performance can replace existing multiple-module, narrowband MIC designs and

(2) There is an inherently lower cost for a MMIC based design for which labor in tuning costs (currently incurred in the MIC PIN diode based narrowband designs) is eliminated.

Characteristics of Digital Phase Shifter Translators

The staircase approximation of the ideal linear phase function results in unwanted spurious signals whose levels are determined by the following factors: (1) number of phase steps (determined by the number of phase bits, (2) insertion loss variations versus phase state in the bits, (3) phase errors in the bits and, (4) switching time of the phase bits.

The following summarizes the characteristics of a frequency translator on the basis of Fourier analysis of the staircase approximation of the phase function of an RF signal[1-4]:

(a) Spurious versus number of phase steps

When there are no amplitude and phase errors, it is found that the input frequency (f_0) and all undesired harmonics of f_m (translation frequency) are completely suppressed except those frequencies given by:

(1) $$f_{out}=f_o - C(1 \pm k.N)f_o = f_o - n.f_m$$

where, C=+1 or -1 for translation "up" or "down" respectively, N=number of steps, k=0,1,2..., n=(1±k.N)=spectrum number and + or - corresponds to upper or lower sidebands. It may be noted that for the binary 5-bit case, $N=2^5=32$ and spectral components present are n= -1 for downward translated carrier and spurious signals are at n= +31, +63, +95.... and -33, -65, -97...etc.

The amplitudes of the spectral components given by equation (1) are expressed as:

(2) $$C_n=[\sin(\Pi/N)] / [(kN\pm 1)(\Pi/N)]$$

and are shown in Figure 4 for 5-Bit approximations.

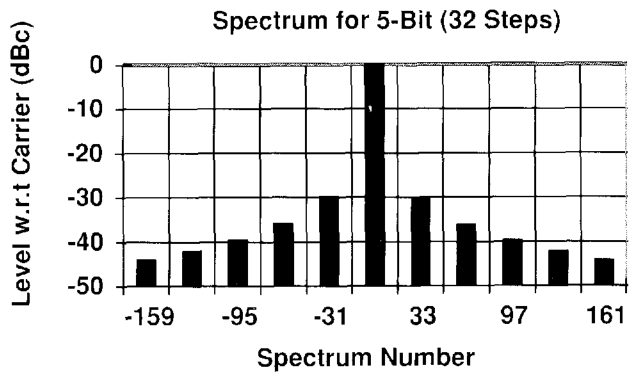


Figure 4. Ideal spectrum of translator based on 5-Bit phase shifter.

Figure 5 shows the worst spurious sideband level (corresponding to k=1 in equation (2)) as a function of the number of ideal phase bits. For example, for a 3-Bit (or 8-step) approximation of the 360 degree range, assuming no amplitude and phase errors, the spurious sideband levels cannot be less than -16.9 dBc with respect to the translated carrier; whereas, for a 5-Bit, or 32-step case, the spurious sideband levels cannot be less than -29.8 dBc with respect to the translated carrier. In general the spurious levels relative to the translated carrier are given by 20*Log(N-1) dBc, where N=number of phase steps. A rule of thumb is to expect about a 6 dB improvement in the spurious level for every added phase shift bit (with consequent doubling of phase shift steps).

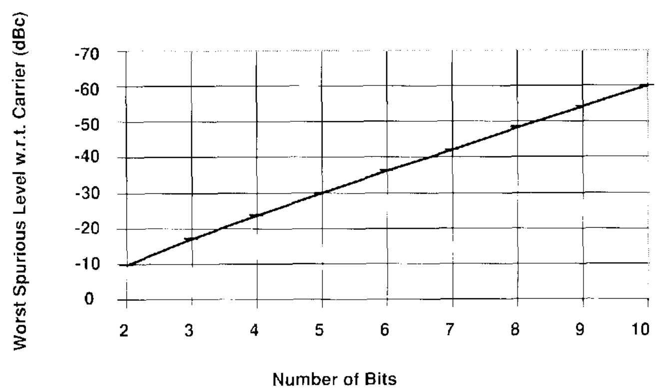


Figure 5. Ideal spurious suppression versus the number of phase shift bits.

(b) Effects of amplitude and phase errors

The effects of errors in the amplitude and phase of the digital phase bits are to degrade the other spurious levels. From a Fourier analysis of the stepped phase approximation some very interesting characteristics have been observed and these are summarized as follows:

(1) Errors in the 180 degree phase bit degrade only the carrier and the even sidebands, i.e., the spectrum numbers affected are: n=±2p, where p=0,1,2,....

(2) Errors in the 90 degree phase bit degrade only the odd sidebands spaced by $4f_m$, i.e., the spectrum numbers affected are: n=c ±4p, where p=0,1,2,....and c=-1 (or +1) for translation up (or down) case.

(3) Errors in the 45 degree phase bit degrade only the odd sidebands spaced by $8f_m$, i.e., spectrum numbers n=3c ±8p, where p=0,1,2,...

(4) Errors in the 22.5 degree phase bit degrades only the odd sidebands spaced by $16f_m$, i.e., spectrum numbers n=7c ±16p, where p=0,1,2,... and so on for other phase bits.

An example identifying various spectrum numbers affected by errors in a particular phase bit is shown in Figure 6.

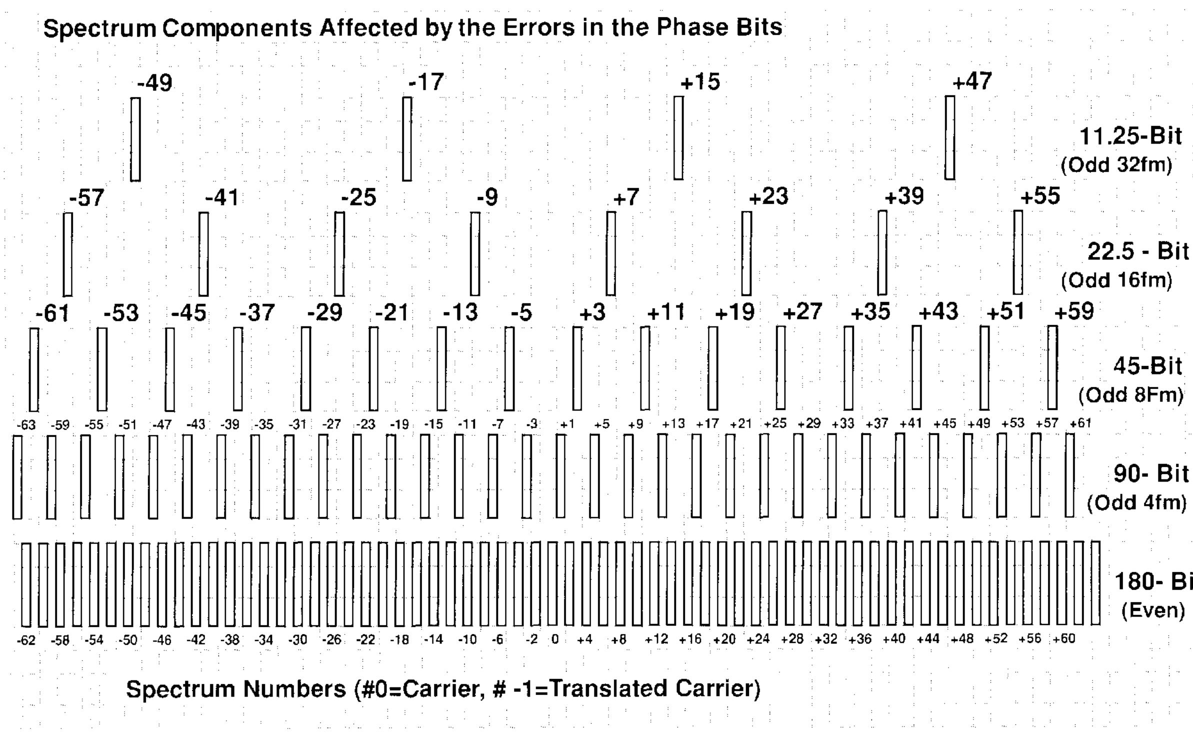


Figure 6. Effects of amplitude and phase errors of the phase bits on the spurious levels.

By extending the Fourier analysis to the general case of including the amplitude and phase errors of the phase bits, effects of these errors on the spurious levels have been studied. A trade-off of the maximum amplitude and phase errors that can be tolerated (versus number of phase bits) without exceeding the spurious levels (corresponding to ideal staircase) is shown in Figure 7, where contours for each number of bits are plotted using amplitude errors as the x-axis and the phase errors as the y-axis. From this it can be seen that for the 5-bit case (least significant bit=11.25 degrees and ideal worst spurious= -29.8 dBc), the amplitude errors must be within ±0.83 dB) and the phase errors must be within ±5.65 degrees (less than half the phase shift of the least significant bit).

Effects of Switching Time

Because the switching time between the two states of a phase bit is not zero, additional degradation in terms of the unwanted spurious levels occurs.

Requirements which dictate the maximum levels of unwanted spurious signals serve to determine the minimum number of phase bits to be employed in the design of a translator. On the other hand, the translation frequency requirement establishes the time period within which all phase steps must be switched. As an example, for a translation frequency of 100 kHz, the time period is 10 Microseconds. Thus , for a 5-Bit (32 steps) phase shifter case, each bit duration is 312.5 nanoseconds.

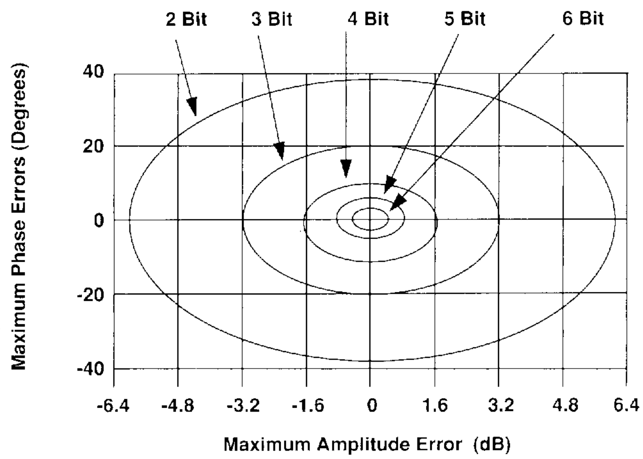


Figure 7. Trade-off of maximum amplitute and phase errors versus number of bits.

Clearly, the switching times between the two states of any phase bit should be small compared to this duration. As a rule of thumb, it is desirable to keep the transition time to less than 10% of the bit duration, or in this case less than 30 nanoseconds in order to keep the spurious levels due to switching time below those due to the effects described for phase shift and amplitude errors.

Digital Phase Shifter Configurations[7]

For the serrodyne frequency translator application, phase shifter bits must provide fairly constant phase shift throughout the entire microwave band of the translator. Basically there are four types of phase shifter configurations that are considered for this application. These include the *Switched line, Reflection type, Loaded-line and High/Low-pass* types, as depicted in Figures 8a to 8d.

A switched line phase shifter utilizes SPDT switches to switch between two paths which differ in length by the required phase shift.

A wideband reflection type phase shifter uses a circulator (or a 3-dB quadrature coupler). The required phase shift is realized by switching between two identical reflective loads of phase values which differ to the extent of the desired phase shift for the bit.

The loaded line phase shifters are realized by switching between inductive and capacitive susceptances shunting a transmission line (usually at locations spaced about a quarter-wavelength apart for transmission match purposes)

A low/high pass type phase shifter provides differential phase shift by switching between a low-pass and high-pass filter circuits.. A low-pass filter circuit containing shunt capacitance and series inductance provides a phase delay to a signal passing through it, whereas, a high-pass filter circuit, containing shunt inductances and series capacitances provides a phase advance. By judicious selection of the two circuits a nearly constant phase shift over a broad frequency band is obtainable by switching between the two filter circuits. Switching may be performed by utilizing SPDT switches employing PIN diodes or, in gallium arsenide MMIC based designs, by field effect transistors (FETs) used as switches.

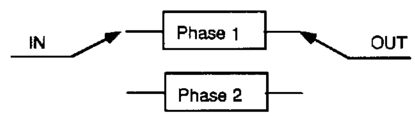


Figure 8a. Switched line phase shifter.

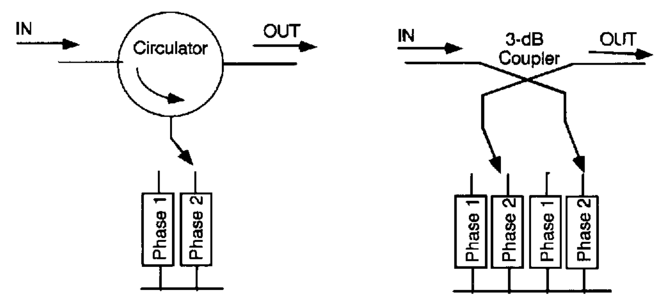


Figure 8b. Reflection type phase shifter.

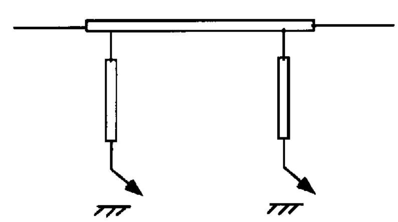


Figure 8c. Loaded line phase shifter.

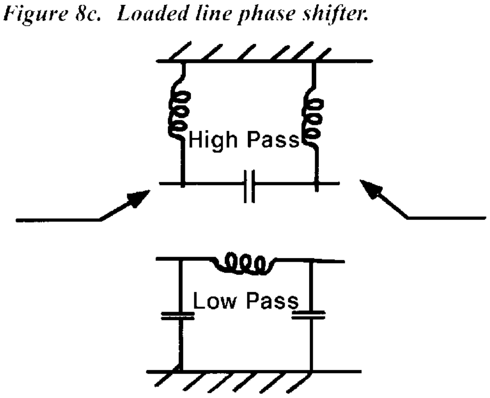


Figure 8d. High/low-pass phase shifter.

Practical Results

The layout of our 5-bit phase shifter is shown in Figure 9. The design is based on the high/low-pass filter circuit [6-7] and utilizes FETs to switch between phase states. At a particular phase state of each bit, a group of FETs is turned "ON" and another group of FETs is turned "OFF". In the second phase state of the bit, the first group of FETs is now turned off with the second group of FETs being simultaneously turned on. A FET is turned on or off when the gate to source voltage is equal to zero or the pinch-off voltage, respectively. Thus, every phase bit requires two complementary control signals, i.e., when one is at 0 volts, the other is at pinch-off (typically less than -5 V) and vice versa.

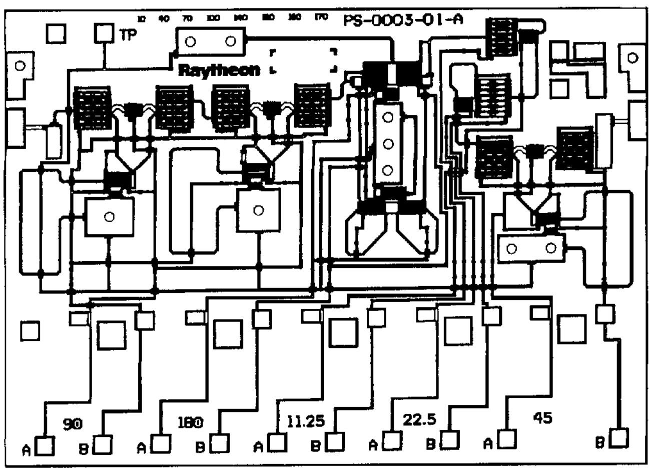
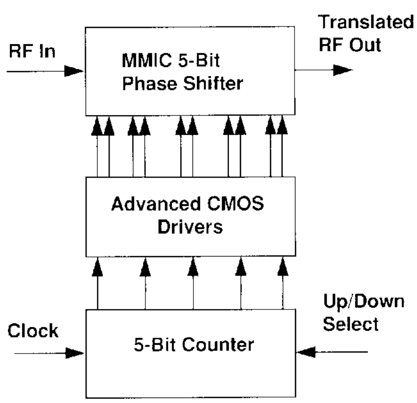


Figure 9. Layout of the MMIC 5-Bit phase shifter.

The block diagram of the frequency translator utilizing the MMIC 5-bit phase shifter chip shown in Figure 9 is shown in Figure 10.



Block Diagram

Figure 10. Block diagram of the frequency translator.

The control signal for sequentially stepping through the 32 steps of the 5-bit phase shifter is generated using a 5-bit counter circuit followed by drivers using TTL HEX inverter gates of the advanced CMOS type (Figure 11). This approach allowed operation of the interface circuitry at a high clock frequency, close to 15 MHz, thus extending translation frequency to as much as about 500 kHz.

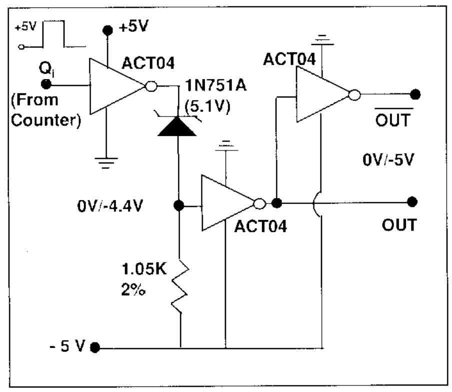
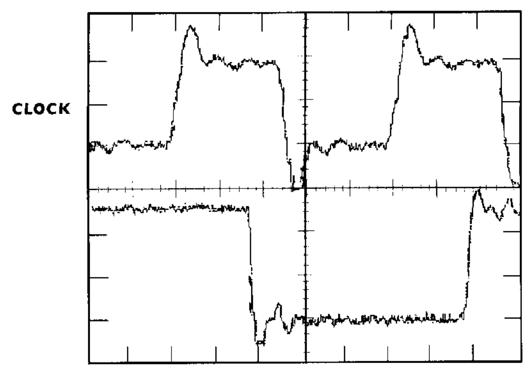


Figure 11a. Schematic of driver circuit for MMIC phase shifter.



(VERT: 2V/div; HOR: 20ns/div)

Figure 11b. Driver output waveform.

A photograph of the translator circuit is shown in Figure 12, wherein the control and interface driver circuitry are realized on thick-film alumina substrate.

Performance of the 5-Bit phase shifter was first evaluated by statically setting the control signals corresponding to each of the 32 steps of the phase shifter. Figure 13 and 14 show the insertion loss and differential phase shifts of all the 32 steps of the phase shifter over the 6 to 18 GHz microwave bandwidth.

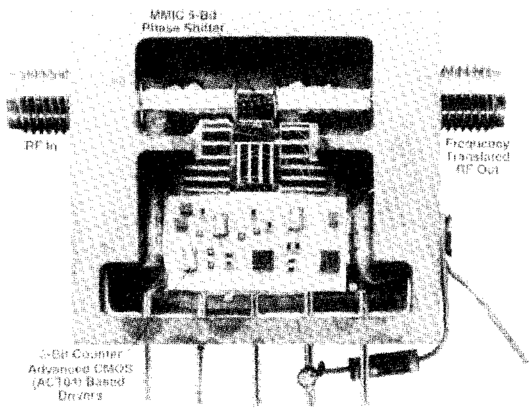


Figure 12. Photograph of the 5-Bit phase shifter based frequency translator.

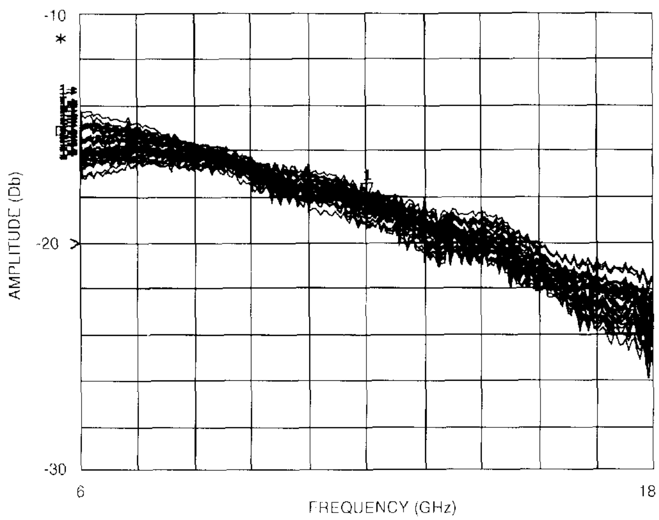


Figure 13. Insertion losses at 32 steps of the 5-Bit phase shifter.

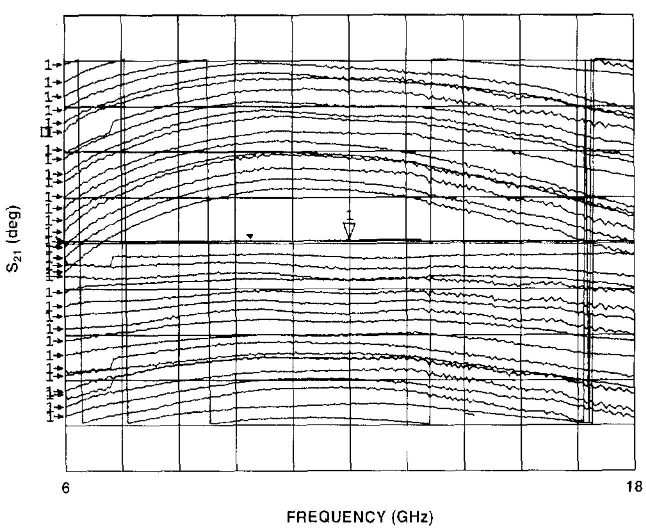


Figure 14. Differential phase shifts of 32 steps of the 5-Bit phase shifter.

The insertion loss of the phase shifter varies from a nominal 6 dB at 6 GHz to about 14 dB at 18 GHz with loss variation among the 32 states at any intermediate frequency of less than ±1.5 dB. The errors in the differential phase shifts appear to be quite large, yet they measured to be less than <±10 degrees over most of the band within 6 to 18 GHz.

Performance of the phase shifter as a frequency translator was then evaluated by dynamically changing the control signals and observing the output spectrum corresponding to a particular carrier frequency. Figure 15 shows a typical spectrum observed for an input carrier frequency of 6.5 GHz. The output signal is translated downward by about 300 kHz when the control circuit was driven at a clock frequency of about 10 MHz. It can be observed that the carrier and other unwanted sidebands are suppressed by more than 22 dB. Figure 16 shows similar performance for an input frequency of 18 GHz.

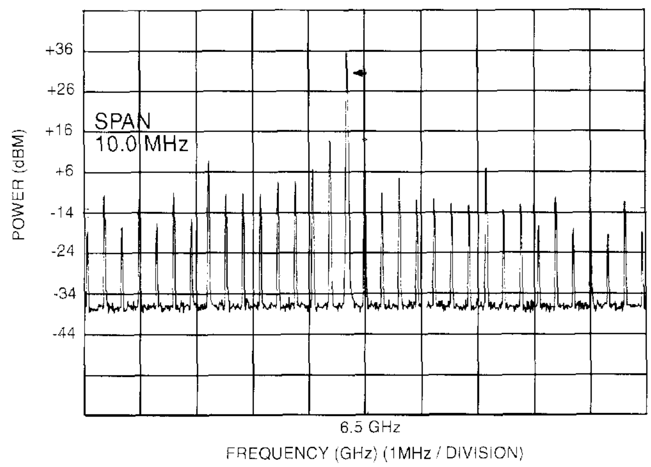


Figure 15. Output spectrum of the translator at 6.5 GHz.

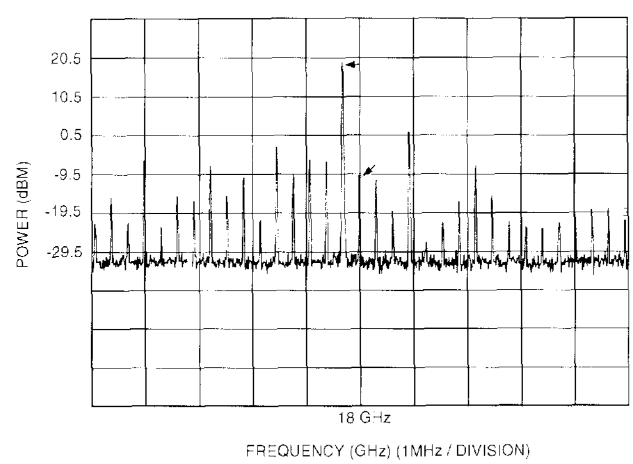


Figure 16. Measured output spectrum of the translator at 18 GHz.

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His research activities, publications and significant contributions have concentrated on microwave power transistor characterization and amplifier designs, performance improvement of power amplifiers by harmonic tuning, novel phase shifter configuration and bi-phase modulator, and frequency translators.

Carl Isham received the Bachelor of Science degree in Physics in 1969 from the University of New Hampshire. He has worked at Omni-Spectra, Sanders Associates, Alpha Industries, B&W Associates and Adams-Russell Company where he was engaged in the development of hybrid control circuitry, microwave components and subsystems. Since 1980, he has been with Raytheon Company, and is currently a Senior Design Engineer in the Electronic Systems Division, Tewksbury, MA.

He has developed hybrid switch drivers, employed SPICE circuits and is knowledgeable in surface mount technology. He has developed designs for logic, programmable logic, and analog circuitry including high speed, low level and high current circuitry for integration with microwave semiconductor components and subsystems such as PIN diode based components, FETs and MMIC based subsystems for commercial and ECM applications. He disclosed novel concept and successfully developed a low level, high speed and highly accurate BIT detector circuit for ECM module application.