High Power 2-18 GHz MMIC TR Switch

Asymmetrical design of the Transmit and Receive arms, dual gate FETs, and large FET peripheries yield a TR switch with power handling better than 3 watts, 8 dB higher than any previously reported for comparable bandwidth MMIC's.

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At rf frequencies, power handling in switch FETs is limited by voltage swing in the "off" state (the capacitive state) and current saturation in the "on" state (resistive state) [1]. The present state of the art power handling for broadband (such as 6-18 GHz and dc-20 GHz) MMIC switches is 24 to 27 dBm[2][3]. Over narrow frequency bands (10% bandwidth), up to 10 watt power handling has been demonstrated by transforming impedances to reduce current at some FETs and voltage at others [4]. However this technique is not practical over a bandwidth as large as 2-18 GHz.

The present state of the art is 24 to 27 dBm.

The use of stacked FETs has been reported in a very high power switch operating at lower frequencies (1-2 GHz) [5]. Reactive tuning elements were incorporated to balance the rf voltage distribution across the FETs in the stack. While this method cannot be applied as effectively over 2-18 GHz, the stacked FETs are analogous to the dual gate FETs used in this work.

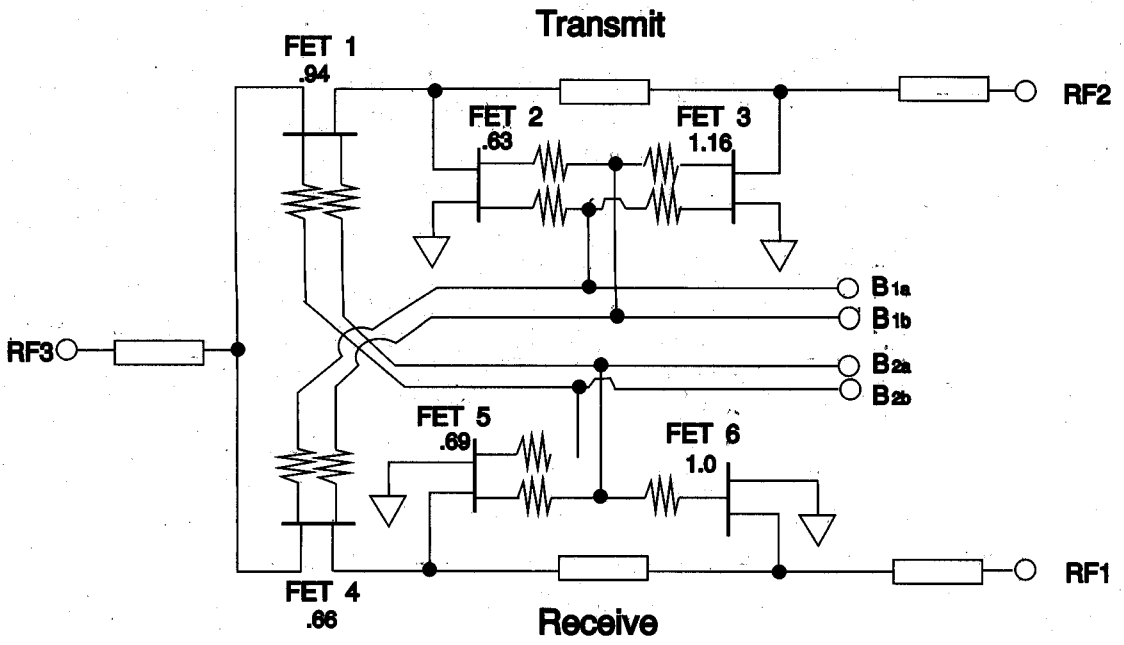

Figure 1. Schematic of the 2-18 GHz high power T/R switch.

The use of dual gate FETs in place of a stack of individual FETs reduces device area with a resulting reduction in parasitic series inductance through the FET and shunt capacitance from the FET to ground. These parasitics must be minimized in order to ensure low insertion loss to 18 GHz. Power handling is somewhat lower for the dual gate FET than for the stacked FETs, since rf voltage cannot be distributed as uniformly across the gates. Off state capacitance is higher for a dual gate FET than a stacked FET, since the close proximity of the elements leads to additional parasitic capacitances.

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Design approach

Conventional broadband 1 x 2 switches use a combination of series and shunt switch FETs, and typically provide 27 dBm of power handling. Insertion loss is typically less than 2 dB, and isolation is at least 30 dB [3]. In the design of the 2-18 GHz high power T/R switch presented in this paper, the same basic circuit approach used in conventional lower power switches was used, but three techniques were employed to increase power handling.

Three techniques were employed to increase power handling.

The first is the replacement of conventional single switch FETs with dual gate FETs in some circuit locations. In a simplified analysis a dual gate FET can be considered comparable to two single gate FETs in series. The rf voltage swing can be distributed across these two devices, extending power limits imposed by voltage limiting. In reality, there is significant capacitive coupling between the two FETs within a dual gate FET. This cross coupling decreases power handling slightly, on the order of 1 dB.

The first is the use of dual gate rather than conventional FETs.

Compared to the single gate FETs used in conventional series and shunt FET broadband switches, the on state resistance (Ron) of a dual gate FET is considerably higher. In order to maintain a reasonably low insertion loss, it is necessary to increase the periphery of these devices considerably. However, as will be seen, the periphery of a dual gate FET can be considerably larger than the periphery of a single gate FET.

The second technique is to increase the periphery of some FETs. Large peripheries are used to provide higher rf current handling. A problem with increasing peripheries is the resulting increase in the off state capacitance (Coff). Nevertheless, high values of Coff cannot be accommodated by the switch circuit without resulting in much higher insertion loss. In

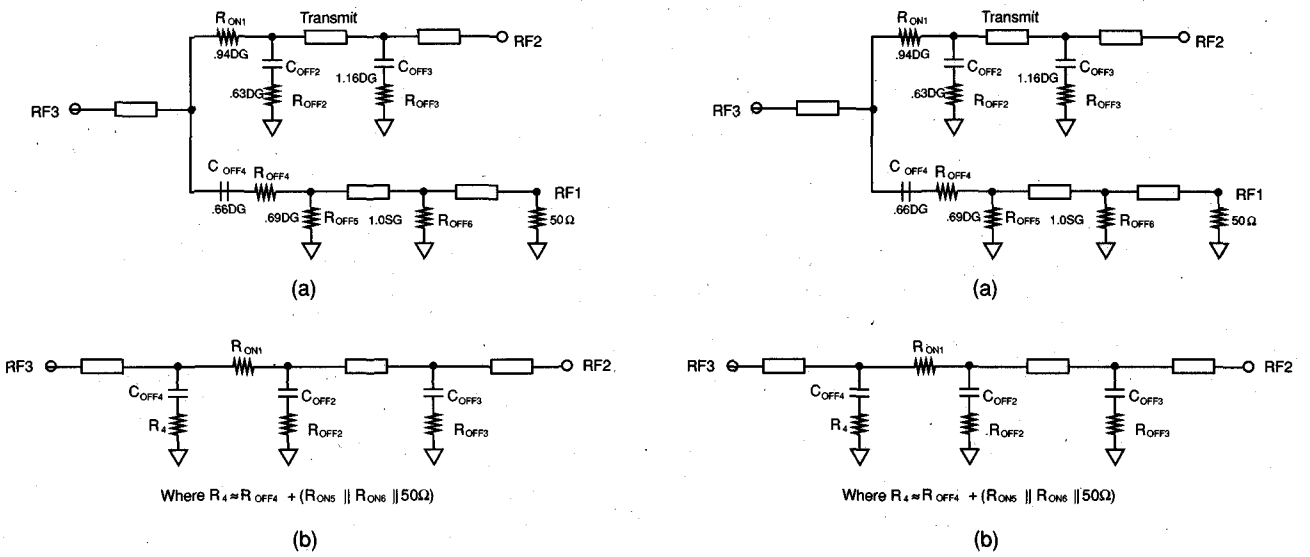

Figure 2 (a) Complete equivalent circuit of the switch in Transmit mode, (b) simplified equivalent circuit.

order to incorporate large peripheries, without increasing insertion loss, dual gate FETs are used, since their Coff in considerably lower than that of a single gate FET.

The second technique is to increase the FET periphery.

The third technique is the use of an asymmetrical switch design in which the circuit is designed so that the Transmit and Receive arms are different. For example, the shunt FETs in the Transmit arm and the series FET in the Receive arm must handle the largest rf voltage swings, therefore dual gates are used. The series FET in the Transmit arm and the shunt FETs in the Receive arm must handle the largest rf currents, therefore they should have large peripheries. In some cases, dual gate FETs are used in these locations as well, simply to reduce Coff.

The third technique is to use large FET peripheries in the transmit arm.

The schematic of the 2-18 GHz high power switch is shown in Figure 1. The periphery of each device is indicated. The switch is designed to handle highest

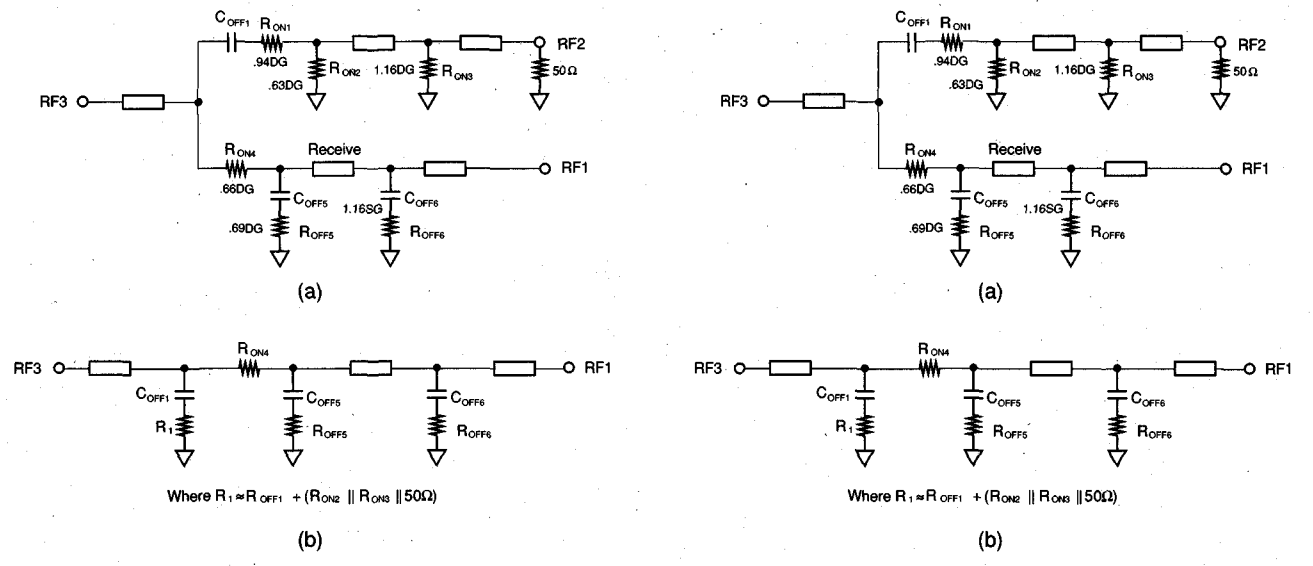

Figure 3 (a) Complete equivalent circuit of the switch in Receive mode, (b) simplified equivalent circuit.

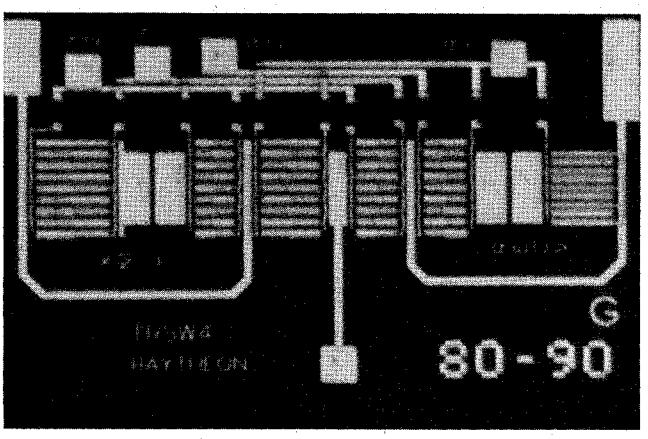

Figure 4. Photograph of the 2-18 GHz high power switch.

power in the Transmit mode. Note that FET2, FET3, and FET4 must all handle large voltage swings, and therefore dual gates are used. The peripheries of these devices are also quite large in order to reduce on resistance. FET1 and to a lesser extent FET5 must handle large currents, therefore periphery must be large. These devices use dual gates to reduce off capacitance. FET6 is the only device not made with dual gates.

The equivalent circuit of the switch in Transmit mode is shown in Figure 2a. The periphery of each device is indicated next to its equivalent circuit element(s). Dual gate FETs are indicated by a "DG", single FETs by an "SG". A simplified switch equivalent circuit is shown in Figure 2b. In this case the receive arm is approximated as a resistance. Loss mechanisms are most apparent in the simplified equivalent circuit.

There are two primary contributors to insertion loss. The first is the on resistance of the series FET, in this case Ron1. The second contributor is loss through the shunt RC elements, similar to gate line loss in a distributed amplifier [6]. The periphery of FET1 is quite large, 0.94 mm, ensuring low insertion loss despite the fact that it is a dual gate device. The shunt elements are all dual gate FETs, since this reduces Coff, this also minimizes insertion loss.

The two primary contributors to loss are series resistance and shunt resistance.

The equivalent circuit of the switch in Receive mode is shown in Figure 3. This figure uses the same format as Figure 2. Note that the series FET in Receive (FET4) has a smaller periphery than the series FET in the Transmit mode (FET1). The resulting difference in Ron causes insertion loss to be higher in the Receive mode. The shunt elements are lossier in the Receive mode as well. Shunt capacitance Coff1 in Receive is higher than Coff4 in Transmit because of larger FET periphery. Coff6 in Receive is higher than Coff3 in Transmit because FET6 is a single gate device and FET3 is a dual gate device. Thus the insertion loss in the Receive mode

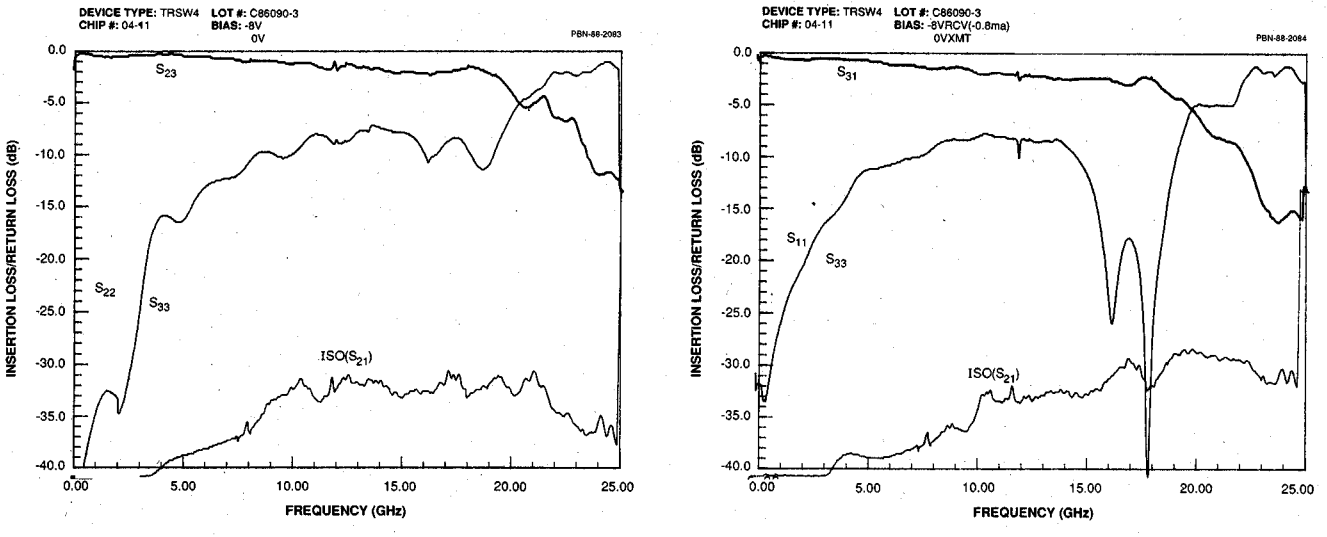

Figure 5. Small signal performance of the T/R switch (a) in Transmit mode and (b) in Receive mode.

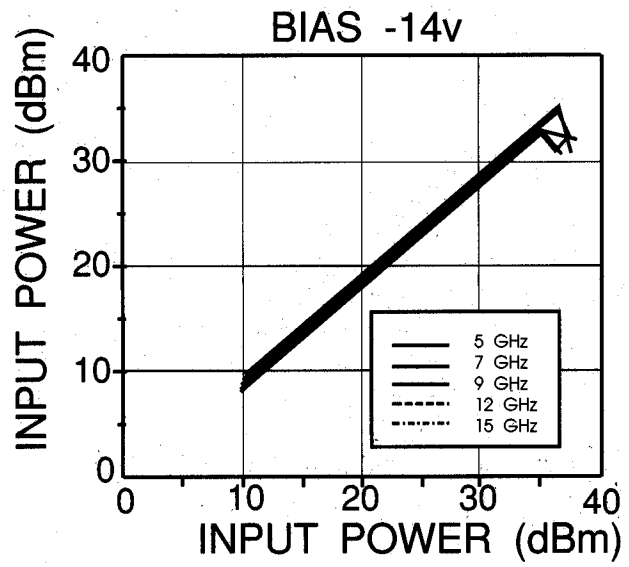

Figure 6. Power transfer curves for the T/R switch in Transmit mode; output versus input power is shown.

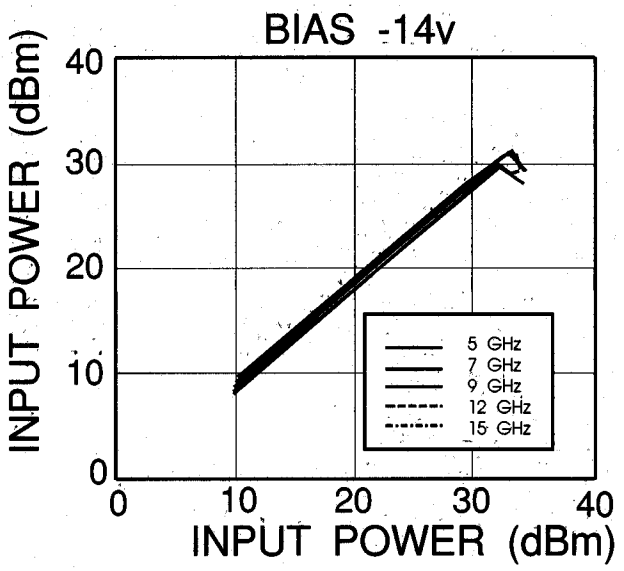

Figure 7. Power transfer curves for the T/R switch in Receive mode; output versus input power is shown.

can be expected to be higher than the insertion loss in the Transmit mode.

The higher loss in the Receive mode is the result of a deliberate design trade- off. The size of the series FETs plays a large role in insertion loss. By increasing the periphery of the series FET in the Transmit mode (FET1), Ron is reduced, which provides a low Transmit insertion loss; Coff is simultaneously increased, which provides a high insertion loss in Receive. Similarly, reducing the periphery of the series FET in Receive mode increases insertion loss in Receive, but decreases insertion loss in Transmit. In the design of the 2-18 GHz T/R switch presented in this paper, minimum insertion loss in the Transmit path was paramount, and was minimized at the cost of Receive insertion loss.

MMIC implementation

The finished MMIC is quite small, 0.9 mm x 1.5 mm or 0.035 x 0.060 inches, as can be seen in Figure 4. The FETs all have 0.5 micron gate length. The nominal source-drain space is 3.5 microns for single gate FETs, 7.5 microns for dual gate FETs. The dual gate FET gate pitch is 4 micron. Vapor phase epitaxial (VPE) material was used with a channel doping of 2 x 10exp17/cc, and an n+ doping of 4 x 10exp18/cc. These circuits were passivated with 2000 Angstroms thickness of silicon nitride.There are no capacitors in this circuit. The wafer was thinned to 100 microns (about 4 mils), and 20 x 100 micron via holes were dry etched.

Both FET gates are biased to the same potential. Only complementary bias is required. No separate driver circuit was needed.

Gate bias is provided through resistors comprised of multiple open gate FETs in series, each 10 microns wide, for a total resistance of approximately 2 kilohms per resistor. Separate gate connections are made for each gate in the dual gate FETs, and independent bias connections were provided. In actual circuit use, both gates of each dual gate FET were biased to the same potential, so only two complementary bias controls were required. No off chip bias circuitry was used.

Results

The measured small signal performance is shown in Figure 5. Figure 5a shows performance for the transmit state, Figure 5b the receive state. In the transmit mode the insertion loss is 2 dB or less from dc to 18 GHz. In the receive mode the insertion loss is 2.5 dB or less from dc to 18 GHz. Isolation is better than 30 dB in both cases. Return losses are generally better than 10 dB to 18 GHz, but reach 8 dB at some points.

The power handling of the switch in the Transmit mode is shown in the transfer curves in Figure 6. Curves are shown for a number of frequencies over the band. Incident power levels up to 35-36 dBm (3.2-4 watts) are handled without significant change in insertion loss. A gate bias voltage of -14 volts was applied; with a bias of -10 volts power handling drops to 32 dBm, and with a bias of -7 volts power handling drops to 29 dBm.

Power handling in the receive mode is shown in the transfer curves in Figure 7. Incident power levels up to 32-33 dBm (1.6-2 watts) are handled without significant degradation in insertion loss. A -14 volt bias was used for this measurement as well.

This combination of power handling enhancement techniques served to increase the power handling capacity of the broadband series and shunt FET switch to 35-36 dBm, more than 8 dB higher than for a conventional circuit. This was accomplished without compromising other switch performance attributes, excepting a small increase in insertion loss in the Receive mode, which is about 0.5 dB higher than for a conventional design.

Acknowledgment

The authors would like to thank P. Hatch for circuit layout, M. Miller and A. Bertrand for MMIC processing, D. Kelly for circuit evaluation and P. Katzin for assistance in circuit design. The authors are grateful to M. Mah, M. Calcaterra, R. Kemerley and R. Carter of the U.S. Air Force, WRDC/ELM, for their support of this effort and their guidance throughout the program.

This work was supported by the U.S. Air Force, WRDC/ELM, Wright-Patterson Air Force Base, Dayton OH, under contract F33615-85-C-1729.

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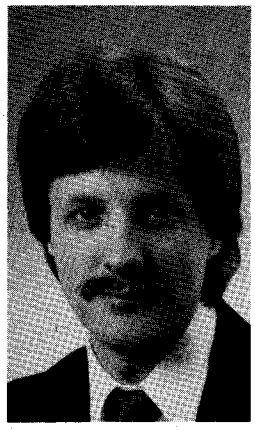
Portions of this paper were presented at the 1990 IEEE MTT International Symposium, Dallas, Texas in a paper entitled "A high power 2-18 GHz T/R Switch."



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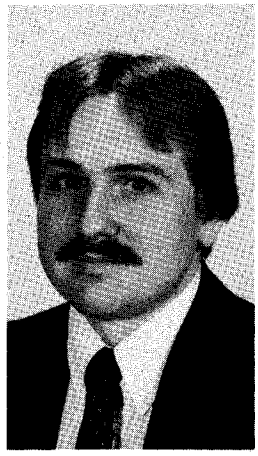

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