The Computer-Aided Design of a Broadband PHEMT Linearizer

Modification of amplitude and phase transfer characteristics allows linear amplifier operation with higher input power

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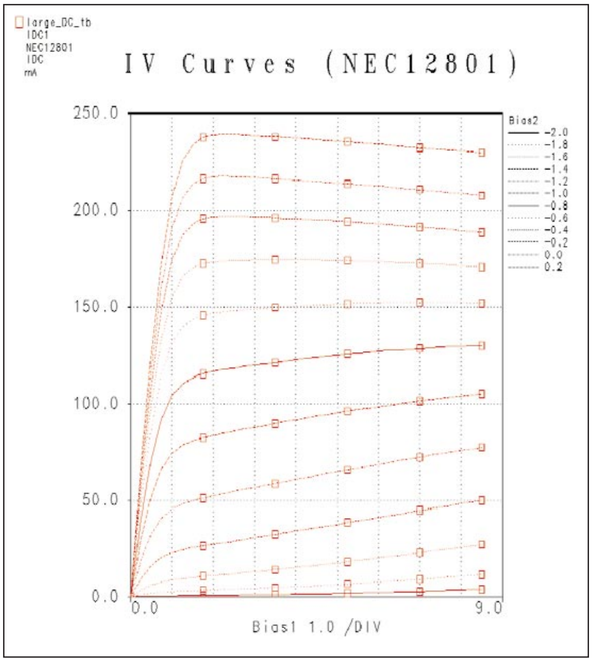
This paper examines a computer aided design (CAD) process for shaping the amplitude and phase transfer characteristics of a linearizer. A systematic design and optimization procedure is described, utilizing a Bias Dependent Large-Signal model of a PHEMT that was implemented in a commercially available software package.

The need for an amplifier to operate at higher input power levels, while keeping its linear power characteristics, is ever increasing. The problem is that the greater the input power to an amplifier, the more it is driven into its non-linear region. Non-linearity creates intermodulation distortion (IMD). The non-linearity is mainly defined by the third order intermodulation distortion (IM_3) [2].

Currently, two methods are used by circuit designers in order to achieve higher linearity: to design an amplifier in the linear region (Class A, AB) or to back off from the 1 dB compression point by 3 dB (3 dB backoff point). Backing off from the 1 dB compression point by 3 dB allows the amplifier to operate in a more linear region, but with some loss of input operating power. The problem that occurs in a power amplifier design is the tradeoff between the operating input power and its linear power gain.

The natural response of a power amplifier is to linearly increase its output power with respect to increasing input power, until it reaches an input power level that causes the output power to compress or become non-linear. The gain of the power amplifier is constant as the output power linearly increases. Similarly, the gain compresses as the output power compresses (gain compression).

The function, then, of a linearizer circuit is to exhibit gain expansion at a particular input power level. The linearizer's gain expansion should cancel with the power amplifier's gain compression in order to create a more constant gain for the power amplifier. Subsequently, this enables the power amplifier to exhibit a larger range of linear power gain.

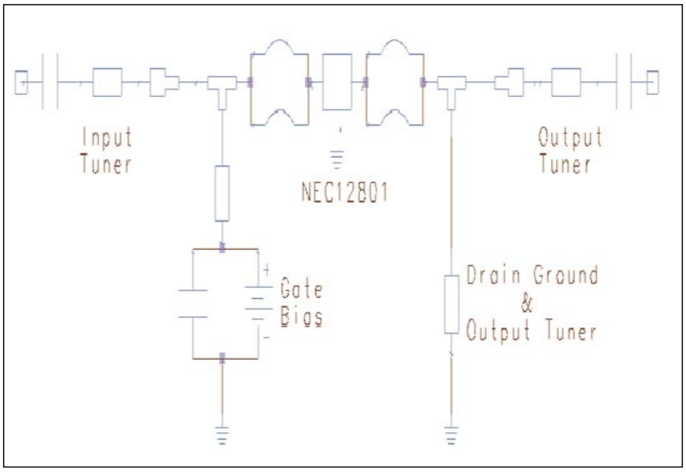


■ **Figure 1. I-V curves of the NEC12801 PHEMT used as the example device in this paper.**

In this paper, a Bias Dependent Large-Signal model of a PHEMT is simulated to show that it can produce tunable amplitude and phase transfer characteristics of a linearizer.

Pre-analysis

In order to use a bias dependent model [1], it is necessary to make sure that the model is accurate within a measured bias range (Figure 1). As



■ **Figure 2. Schematic diagram of the linearizer.**

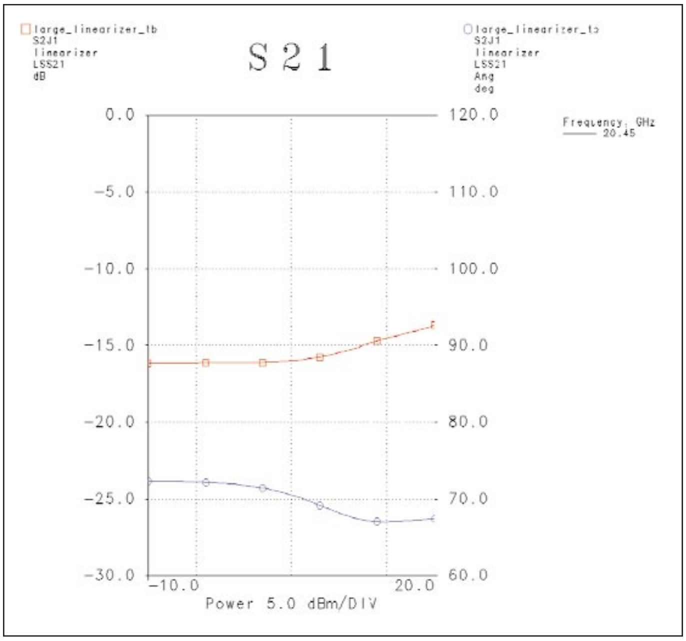
long as the model is operated within this region it is safe to say that the model will accurately predict non-linear characteristics. The device used is an NEC12801 PHEMT.

Design procedure

The Bias Dependent Large-Signal PHEMT model affords the designer the luxury of predetermining the bias and frequency dependence of any simulated circuit.

The schematic of the linearizer is shown in Figure 2. The source is directly grounded, while the drain is grounded through a tunable microstrip line. The linearizer, consistent with previously reported work [3], has only a PHEMT and matching circuits for tuning.

At a frequency of 20.45GHz, with a gate bias of –1.6V, the linearizer exhibited a gain expansion of approximately 2.5 dB (S_{21}dB) and a phase shift of approximately –5 degrees (S_{21}ang) (Figure 3). As a benchmark, the tuners were chosen to be quarter-wavelength impedance transformers.

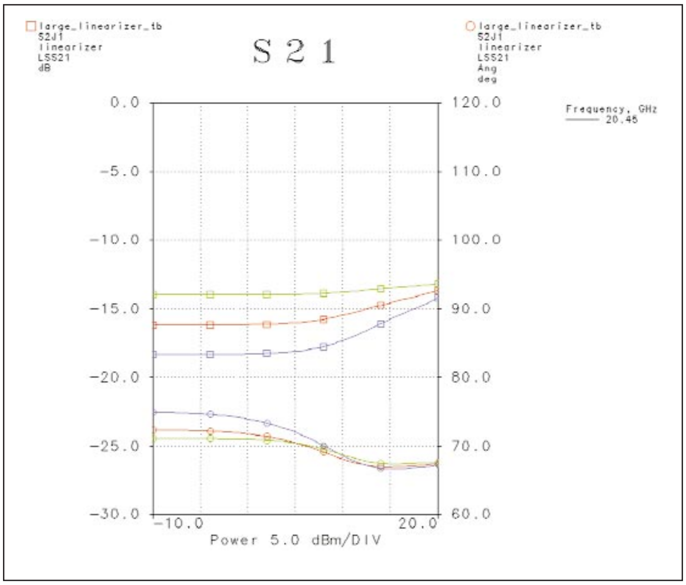


■ **Figure 3. 20.45 GHz gain expansion and phase shift.**

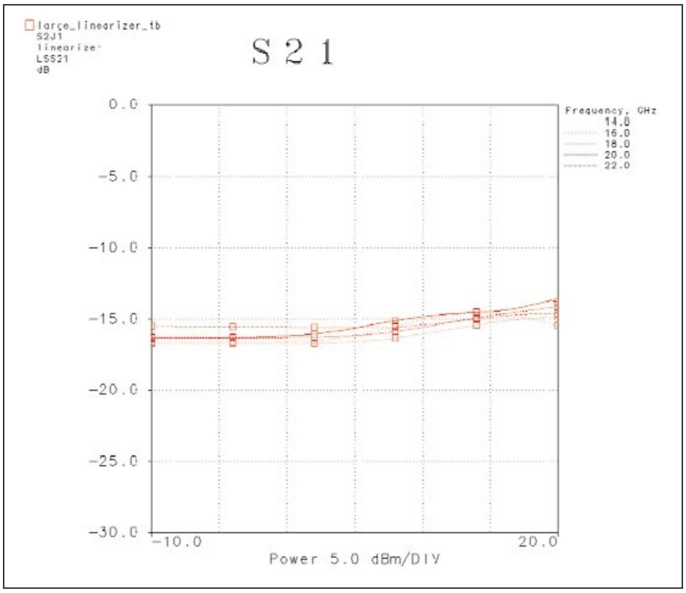
Optimization technique

To effectively optimize the linearizer's transfer characteristics, it is necessary to always find and utilize an optimum operating point. The chosen operating point should not only exhibit the necessary gain expansion, but also be within a reasonable range of gain for a typical amplifier used as an input stage for the linearizer.

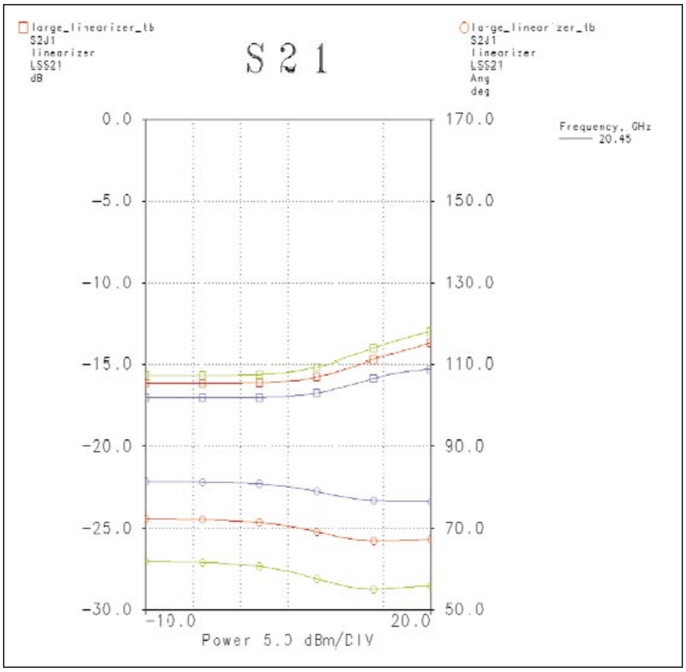
The bias on the gate is varied from –1.7 V (green) to –1.5 V (blue) (Figure 4). At the input stage of the linearizer, an amplifier with a gain of 14 dB, 16 dB or 18 dB would be needed to use the gain expansion characteristics exhibited by the linearizer, which is 1.1 dB (green), 2.5 dB (red) or 4.1 dB (blue).



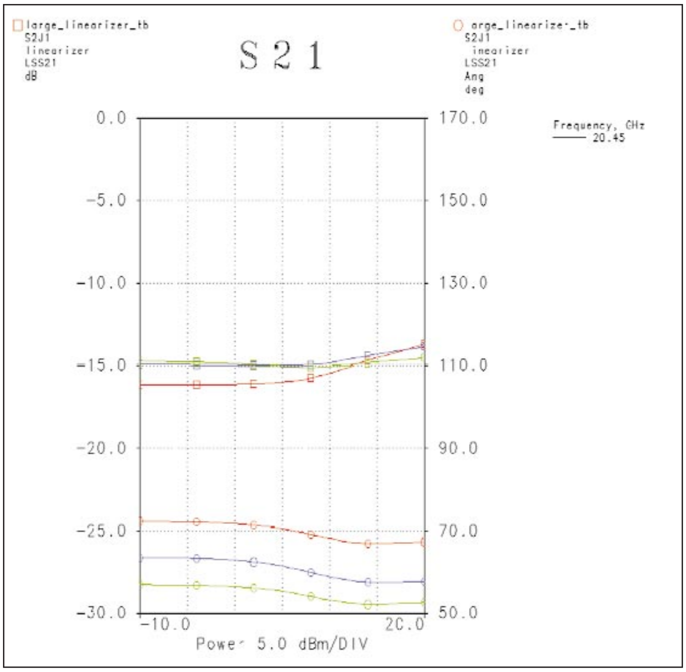
■ **Figure 4. Linearizer transfer characteristics at bias levels of –1.7 V (green), –1.6 V (red) and –1.5 V (blue).**



■ **Figure 5. Linearizer performance at frequencies from 14 to 22 GHz.**



■ **Figure 6. Performance variation with input tuner line width: 30 mils (blue), 40 mils (red) and 50 mils (green).**



■ **Figure 7. Performance variation with output tuner line width: 6 mils (red), 16 mils (blue), and 26 mils (green).**

At a gate bias of –1.6V, the linearizer can be operated over a broadband frequency range of roughly 8 GHz, as shown in Figure 5.

With the bias and frequency dependence known, a designer can also use the input and output tuners' dimensions to aid in the gain expansion curve shaping.

Varying the input tuner's line width (Figure 6) can optimize the linearizer's amplitude and phase transfer characteristics. Line widths used are 30 mils (blue), 40 mils (red) and 50 mils (green).

As shown in Figure 7, a variation in the series output tuner's width also varies the amplitude and phase transfer characteristics. Output line widths used are 6 mils (red), 16 mils (blue) and 26 mils (green).

Conclusion

A Bias Dependent Large-Signal model of a PHEMT was simulated to examine its amplitude and phase transfer characteristics as a result of variations in gate bias, frequency and tuner dimensions. The transfer characteristics agreed well with previously reported calculations and measurements [3]. A design and optimization procedure for tunable results was given. The linearizer shows great promise in that computational time is now only limited to the optimizer's convergence ability as opposed to multiple complex off-line computational techniques.

A future application would be to design a highly linear power amplifier using this linearizer design. ■

Acknowledgement

The author would like to thank Adrian Gilbert for tutelage in device modeling and circuit designs.

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