A Low-Power, CMOS Subharmonic Sampler for a Direct Digitization GPS Receiver

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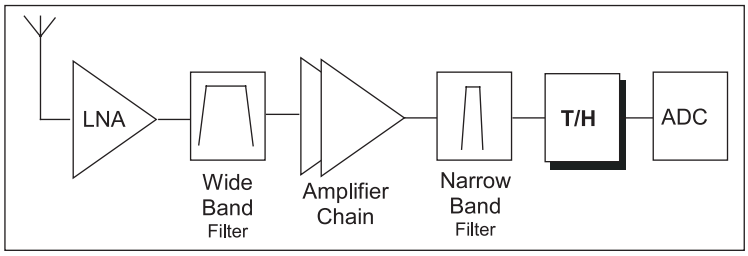
This article describes a low-power complementary metal-oxide semiconductor (CMOS) subharmonic sampler that is intended to work as a track-and-hold circuit in a direct digitization global positioning system (GPS) receiver front-end. The circuit has been implemented in a standard 0.6 μm CMOS process, with two poly-silicon layers, one high resistance poly-silicon layer and three metal layers.

The circuit meets the design objective of a 1.6 GHz input bandwidth and can operate at sampling frequencies from 5 to 40 MHz. For a single-tone input, the measured third-order intercept lies at +21 dBm of input power and –1 dB compression point at +6 dBm. The corrected downconversion loss is 2.52 dB. The circuit topology has been optimized to achieve very low power consumption. The prototype dissipates only 1 mW using a 3-volt supply, an order of magnitude lower than the best published results, to the authors' knowledge.



▲ **Figure 1. Direct digitization GPS front-end receiver.**

Introduction

In recent years, the increased use of mobile communication systems has encouraged research activities for low-cost, highly integrated circuits for receiver handsets. As CMOS went into deep submicron technology, high frequency designs previously made only in GaAs or bipolar technology become possible in CMOS.

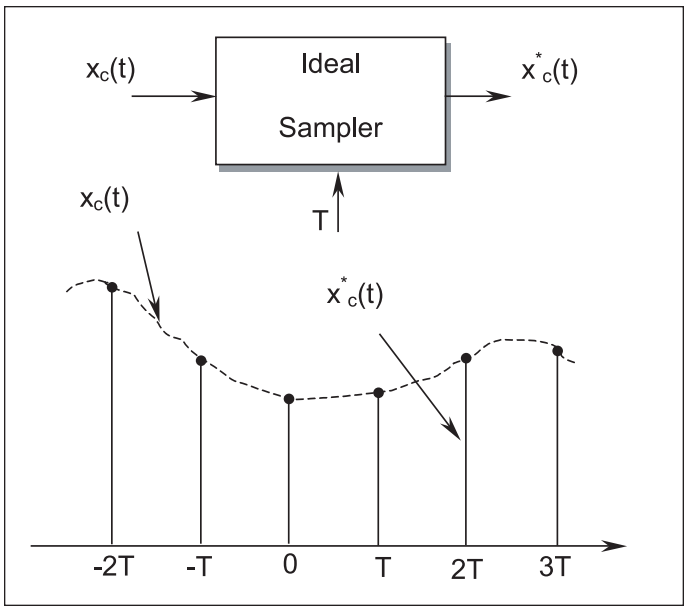
The consumer demand for GPS lead many manufacturers of cellular telephones, portable computers and other mobile devices to look for ways to incorporate GPS into their products. For many of these hand-held devices, one of the primary concerns is battery life. Thus, there is a strong motivation to provide good performance at very low power.

Initially, research concentrated on separate building blocks [1–3], but recently a whole receiver design was presented [4] and new architectures based on direct digitization were proposed [5, 6]. The work on improving these building blocks and developing new ones for these architectures is still intense.

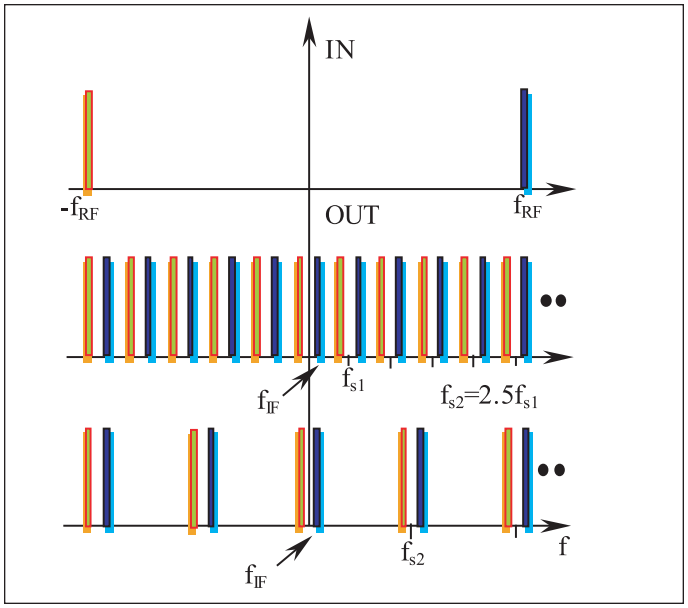
This article describes a differential CMOS subharmonic sampler for 1.6 GHz input bandwidth with offset compensated output. The goal of the design is to work as a low power track and hold circuit, which subsamples the RF input signal in a direct digitization GPS front-end receiver (Figure 1). This gives a signal which is downconverted to a low intermediate frequency. This analog signal is then digitized for further digital signal processing by means of an A/D converter.

Considerations about subsampling

Figure 2 shows the transient response of an ideal sampler, where $x_c(t)$ is the input signal, $x^*_c(t)$ the sampled output signal and T the sampling period.



▲ **Figure 2. Transient response of an ideal sampler.**



▲ **Figure 3. Spectral behavior of a subharmonic sampler for two different sampling frequencies.**

To derive the frequency-domain relation between the input and output of an ideal sampler, we convert $x_c(t)$ to $x^*_c(t)$ through impulse train modulation. The modulating signal $s(t)$ is a periodic impulse train

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{1}$$

where $\delta(t)$ is the unit impulse function or Dirac delta function. Consequently,

$$x^*_c(t) = x_c(t)s(t) = x_c(t) \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{2}$$

Through the "shifting property" of the impulse function, $x^*_c(t)$ can be written as

$$x^*_c(t) = \sum_{n=-\infty}^{\infty} x_c(nT)\delta(t - nT) \tag{3}$$

Consider now the Fourier transform of $x^*_c(t)$. Since $x^*_c(t)$ is the product of $x_c(t)$ and $s(t)$, the Fourier transform of $x^*_c(t)$ is the convolution of the Fourier transforms $X_c(j\Omega)$ and $S(j\Omega)$. Because the Fourier transform of a periodic impulse train is a peridiodic impulse train [7] and $S(j\Omega)$ is

$$S(j\Omega) = \frac{2\pi}{T} \sum_{k=-\infty}^{\infty} \delta(\Omega - k\Omega_S) \tag{4}$$

where $\Omega_s = 2\pi/T$ is the sampling frequency in radians/s, the Fourier transform of $x^*_c(t)$ is

$$\begin{aligned} X^*_c(j\Omega) &= \frac{1}{2\pi} X_C(j\Omega) S(j\Omega) \\ &= \frac{1}{T} \sum_{k=-\infty}^{\infty} X_C(j\Omega - kj\Omega_S) \end{aligned} \tag{5}$$

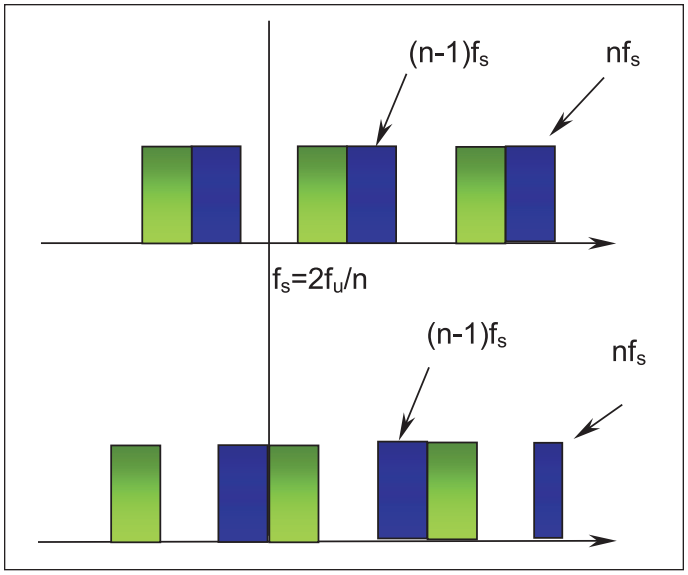
where * denotes the operation of convolution.

Equation (5) provides the relationship between the Fourier transforms of the input and output of the ideal sampler in Figure 2. The Fourier transform of $x^*_c(t)$ consists of periodically repeated copies of the Fourier transform of $x_c(t)$ (see Equation (5)). The copies of $X_c(j\Omega)$ are shifted by integer multiples of the sampling frequency and then superimposed to produce the periodic Fourier transform.

In the sub-sampling case, the copy located at or near baseband can be used as the downconverted signal at the IF. By choosing the appropriate sampling frequency a desired IF frequency is achieved. To produce the desired IF frequency, we choose from the set of sampling frequencies given by the equations

$$\begin{aligned} &\text{if } \operatorname{int}\left(\frac{f_c}{f_s/2}\right) \text{is even}, f_{IF} = f_c - \left(\operatorname{int}(f_c/f_s)f_s\right) \\ &\text{odd}, f_{IF} = f_s - \left(f_c - \left(\operatorname{int}(f_c/f_s)f_s\right)\right) \end{aligned} \tag{6}$$

where int(a) is the truncated integer portion of argument a, f_c is the carrier frequency and f_s is the sampling frequency.



▲ **Figure 4. Two situations corresponding to the upper and lower limits of Equation (7).**

When the sampling frequency f_s is at least twice the bandwidth of the modulated RF input signal, this signal can be downconverted without aliasing (see Equation (3)). However, not all frequencies above the theoretical minimum (twice the bandwidth of the modulated RF input signal) are good choices. In some bands, aliasing will occur. To avoid aliasing, the sampling frequency must be at least twice the bandwidth of the modulated RF input signal, as we have said previously, and the following condition [8] must be verified:

$$\frac{2f_U}{n} < f_s < \frac{2f_L}{n-1} \tag{7}$$

where n is an integer given by

$$l \le n < \text{int}\left(\frac{f_U}{B}\right) \tag{8}$$

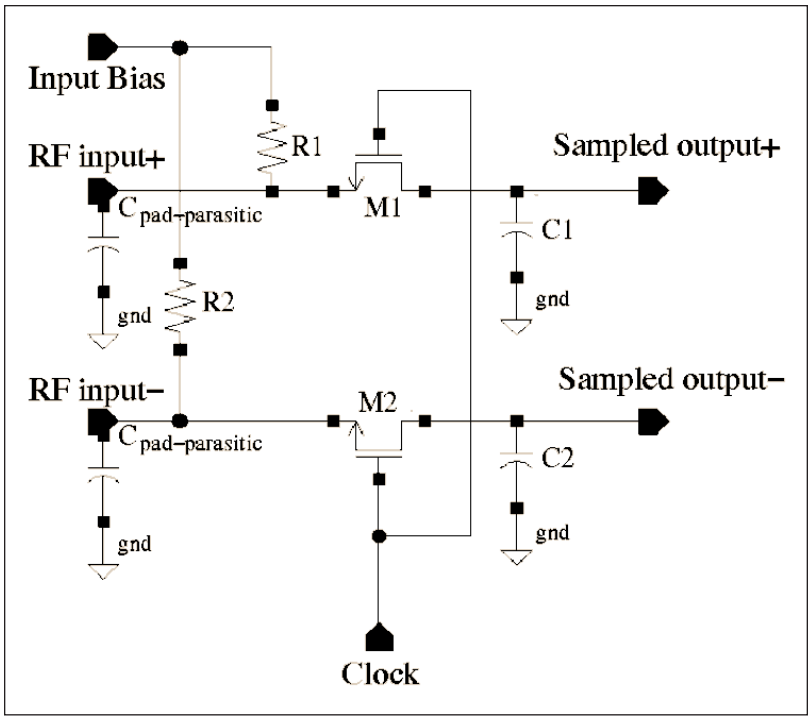
where B is the RF input signal bandwidth, f_U is the higher RF input signal frequency and f_L is the lower RF input signal frequency. The upper and lower limits of Equation (7) for a generic n correspond to the situations shown in Figure 4.

It is important to note that in the sampling process, the signal becomes degraded due to the aliasing of the noise (introduced after any band-pass antialiasing filter) between dc and at least the original band-pass spectral position. This degradation is unavoidable (and could represent a serious problem). However, for the direct digitization GPS receiver architecture, this signal degradation is reduced by the high amplification of the amplifier chain and the previous bandpass filter, which must be as narrow as possible [6].

In our case, an RF input signal of 1.577 GHz has been sampled at 20 MHz. The obtained IF signal obtained from Equation (6) is 3 MHz.

Circuit design issues

This subharmonic sampler chip consists of three stages: a sampling network, an offset compensated differential amplifier and an output buffer necessary to drive the 50-ohm load of the probe head.

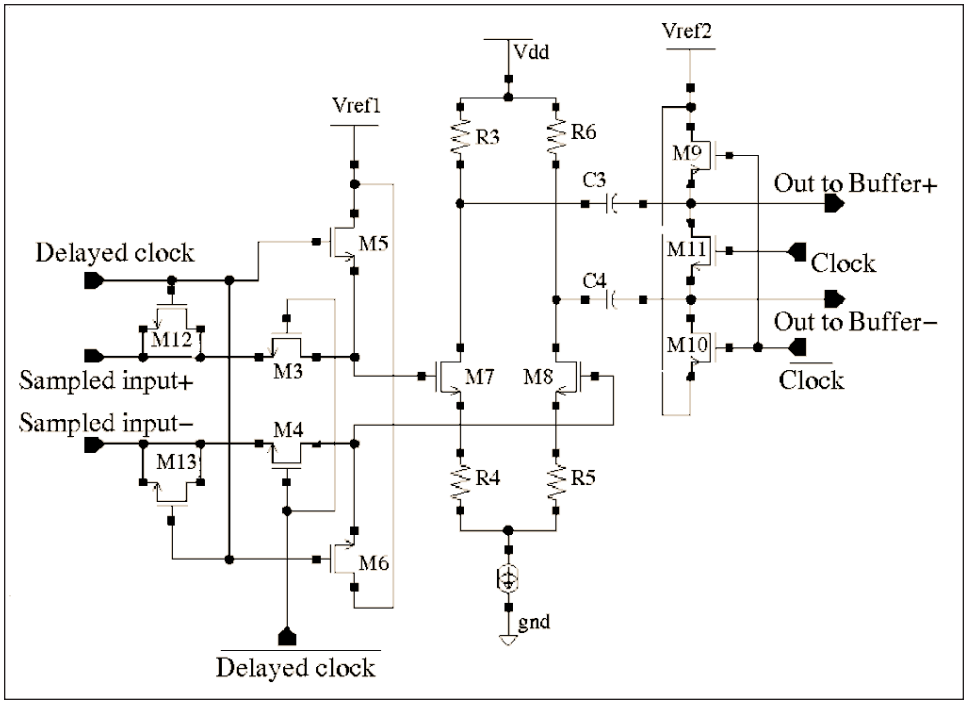


▲ **Figure 5. Input sampling network.**

Sampling network

Sampling circuits can be roughly divided into two categories depending on the switch type. Diode switches are often used when high-speed switching is needed, but at lower sampling frequencies, transistor switches are the dominant choice because they offer higher performance.

The sampling network, shown in Figure 5, presents a differential structure that cancels the signal independent charge injection and the clock feedthrough errors. These errors can be cancelled by taking the input differentially as long as they appear equally on both signal inputs. This structure retains the signal dependent charge injection error. This error, and consequently the distortion introduced by it, is relatively small due to the small input signal, the small input transistors and the small value of the ratio $C_1/C_{\text{pad-parasitic}}$ [9].



▲ **Figure 6. Offset cancelled differential amplifier.**

The sampling distortion due to the increasing MOS ON resistance as it leaves the triode region and due to the sampling time uncertainty is minimized by using a clock waveform with a sharp cut-off. The sampling architecture used and the bottom-plate architecture present similar performances in the presence of a clock waveform with small fall-time [10].

The input transistors M1 and M2 work as switches. In the track-phase, these switches are closed; therefore, the RF path is a low pass type and must have a pole above the maximum tracking frequency. The ON resistance of these transistors (R_{on}) and the capacitors in the RF path (C_s) set the pole of the RF path.

$$f_{pole} = \frac{1}{2\pi C_s R_{on}} > f_{track} \tag{9}$$

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{gs} - V_t\right)} \tag{10}$$

Thus, the values of the sampling capacitors and the dimensioning of the transistors M1 and M2 are critical. A value of 375 fF was chosen for the sampling capacitor.

Two 50-ohm resistors were added between the input and AC ground. This matches the input impedance to 50 ohms and provides a stable load to the preceding stage.

Offset compensated differential amplifier

To improve the common-mode rejection ratio (CMRR) of the circuit and provide buffering, a differential amplifier was used. The analog signal from the sampling network must be digitized for further digital signal processing by means of an A/D converter. Therefore, it is important to minimize the differential amplifier offset to reduce the overall input offset. The configuration chosen is an output offset storage (OOS) structure [11] (see Figure 6).

During the track phase, transistors M3 and M4 are off, and M5 and M6 are on. Thus, at both inputs of the differential amplifier, the same reference voltage ($V_{ref}1$) is applied. During this clock phase, the differential amplifier offset is stored in the output capacitors C3 and C4, which are connected to AC ground through transistors M9 and M10.

During the hold phase, transistors M3 and M4 are on, and M5 and M6 are off, so the sampled value is amplified. During this phase, the stored offset in capacitors C3 and C4 is subtracted from the output and the offset is cancelled.

Transistor M11 minimizes the charge injection from transistors M9 and M10 in the offset storage capacitors. In addition, two dummy transistors M12 and M13 minimize the charge injection from transistors M5 and M6 in the sampling capacitors. The output DC level is $V_{ref}2$. Therefore, no common-mode feedback bias (CMFB) is needed.

Output buffer

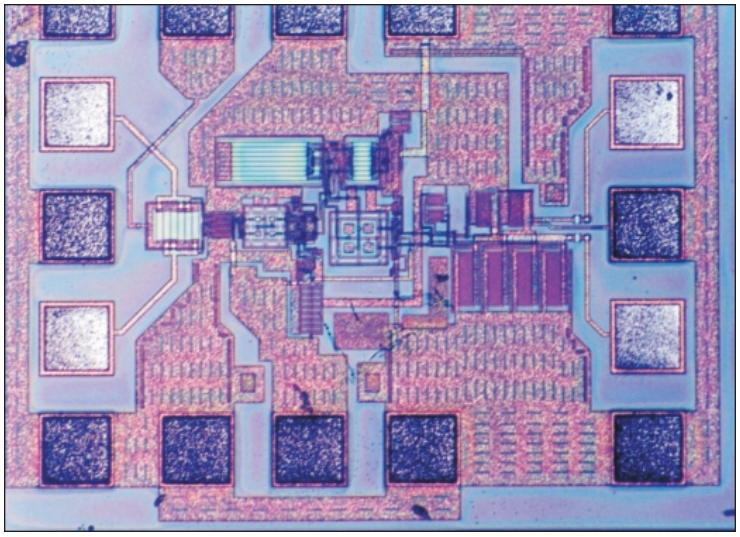
An output buffer is necessary to drive the 50-ohm load of the probe head. This buffer is not necessary in the final design when both track and hold and ADC are allocated at the same chip.

A source follower configuration was adopted and two resistors are introduced to match the output to 50 ohms.

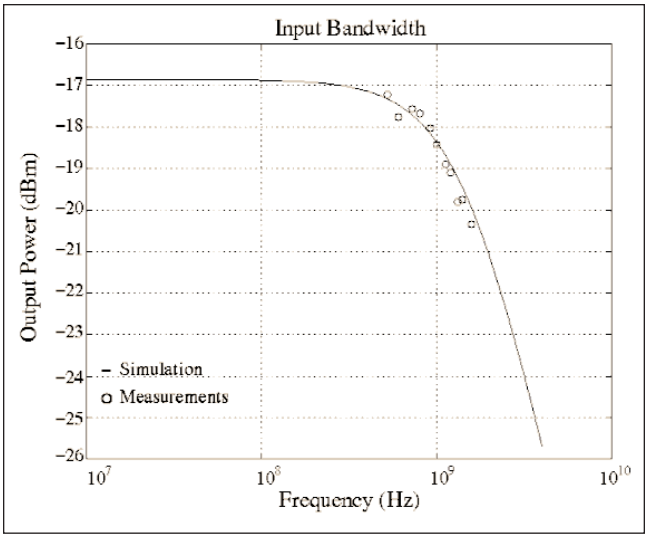
Measurements results

The subharmonic sampler occupies an active area of 0.61 × 0.33 mm (Figure 7), and is designed in a triple metal, double poly, single high-resistance poly CMOS process with a 0.6 µm gate feature size.

The dimensions of the sampling transistors, the values of the sampling capacitors and input resistors are crucial. These conditions provide a stable 50-ohm load to the preceding stage. The measured circuit input impedance for a 20 MHz band centered at 1.575 GHz was (72



▲ **Figure 7. Microphotograph of the subharmonic sampler chip.**

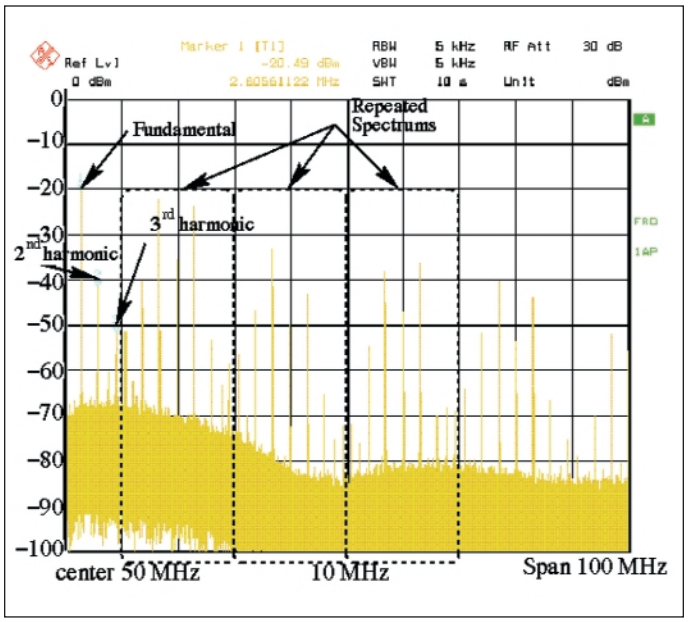


▲ **Figure 8. Input response of the subharmonic sampler.**

$-j7$) ohms. The simulated input impedance for the same band was $(48 - j8)$ ohms.

Spectral measurements were used to evaluate the circuit performance. A coupler was connected between the circuit and the RF synthesizer to produce the differential input. The output was taken single-ended through a DC-block. Most of measurements were done choosing a clock frequency that fixed the IF output frequency at 3 MHz. A clock generator using the crystal reference from the RF source generated the clock waveform.

The design objectives of 1.6 GHz input bandwidth and low power consumption were met and measurements matched well with the simulations. The input frequency is varied to produce a fixed IF of 3 MHz at a 20 MHz sampling frequency (Figure 8).



▲ **Figure 9. Output spectrum.**

Figure 9 shows the output spectrum of an RF signal of 1.577 GHz, subsampled at 20 MHz. As predicted by Equation (6), the output IF frequency is 3 MHz, and periodically repeated copies of the signal spectrum are located at every 20 MHz.

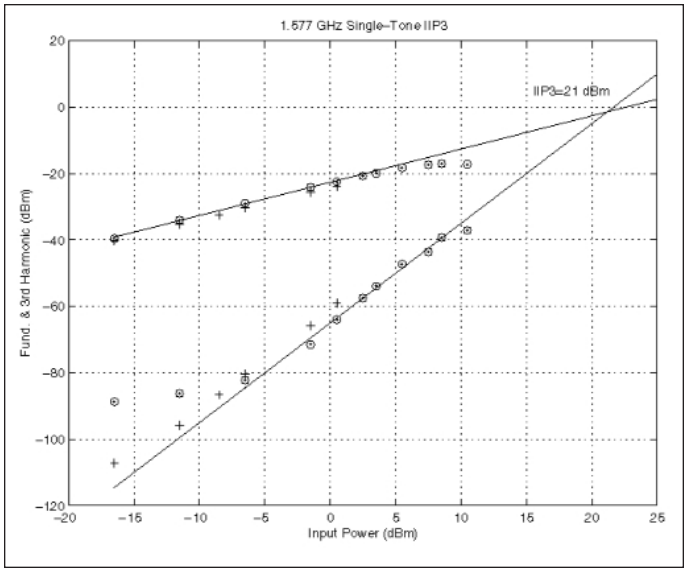
There is a second harmonic spectral component 23 dB below the desired signal and a third harmonic component 34 dB below. The larger second harmonic component is due to the single-ended measurements and differences in the input sampling transistors. Thus, the second harmonic components of the differential path are neither equal nor in phase, so the differential amplifier amplifies them.

The linearity was measured with one tone. Simulated and measured values are presented in Figure 10. The single-tone IIP_3 is +21 dBm. The measured conversion loss is 22.52 dB; of this, 11 dB is due to the output buffer, 3 dB is due to the single-ended measurement and 6 dB is due to the 50 percent clock duty cycle [12]. The corrected conversion loss is 2.52 dB [13].

The post-layout simulated noise figure (NF) is 43 dB. This large value is a consequence of the aliasing of the noise between at least the original band-pass spectral position and DC frequency. This value does not limit the noise figure performance of the whole GPS direct digitization front-end because of the high amplification of the preceding amplifier chain (typically 94 dB) [4, 6].

The total power consumption is 28 mW, with 1 mW consumed by the subharmonic sampler and 27 mW by the output buffer, which is not necessary in the final design, when track and hold and ADC will on-chip.

A summary of the results is presented in Table 1. The circuit conversion loss of 2.52 dB and the IIP3 of +21 dBm are comparable with high-power subharmonic samplers [12–15]. This low power consumption is due to the simple topology.



▲ **Figure 10. Measured single-tone IIP_3.**

Conclusion

A track and hold circuit has been designed using a simple configuration. It can work as a subharmonic sampler in a direct digitization GPS receiver front-end. The tracking part handles input signals up to 1.6 GHz, and the holding part converts the signal to a low intermediate frequency using sampling frequencies up to 40 MHz.

Good linearity was obtained with a single 3-volt supply. The prototype power dissipation is only 1 mW, 12 times lower than the best reported results for IC subharmonic sampler operating in this RF band [12–15]. ■

References

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Bandwidth (GHz)	1.6
Sampling Frequency (MHz)	£ 40
Noise Figure (dB)	43[1]
IIP_3 (dB)	+21
Gain (dB)	–2.52
V^{dd} (V)	3
Power (mW)	1
Technology	0.6-mm CMOS
[1]Post-layout simulated value	

▲ **Table 1. Summary of simulated results.**

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