A Comparison of Various Bipolar Transistor Biasing Circuits

An up-to-date review of bias techniques

By Al Ward and Bryan Ward
Agilent Technologies

The bipolar junction transistor (BJT) is often used as a low noise amplifier in cellular, PCS and pager applications because of its low cost. With a minimal number of external matching networks, the BJT can produce an LNA with RF performance considerably better than an MMIC. Of equal importance is the DC performance. Although the device's RF performance may be quite closely controlled, the variation in device DC parameters can be quite significant because of normal process variations.

It is not unusual to find a 2 or 3 to 1 ratio in device h_{FE}. Variation in h_{FE} from device to device will generally not appear as a difference in RF performance. In other words, two devices with widely different h_{FE} can have similar RF performance, as long as the devices are biased at the same V_{CE} and I_C. The primary purpose of the bias network is to keep V_{CE} and I_C constant as DC parameters vary from device to device.

The bias circuitry is often overlooked because of its apparent simplicity. With a poorly designed fixed bias circuit, the variation in I_C from lot to lot can have the same maximum to minimum ratio as the h_{FE} variation from lot to lot. If there is no compensation I_C will double when h_{FE} is doubled. It is the task of the DC bias circuit to maximize the circuit's tolerance to h_{FE} variations. In addition, transistor parameters can vary over temperature causing a drift in I_C at temperature. The low power supply voltages typically available for handheld applications also make it more difficult to design a temperature stable bias circuit.

One solution to the biasing dilemma is the use of active biasing. Active biasing often makes use of an IC or a PNP transistor and a variety of resistors, effectively setting V_{CE} and I_C regardless of variations in device h_{FE}. Although the technique of active biasing would be the best choice for control of device to device variability and over temperature variations, associated costs are usually high.

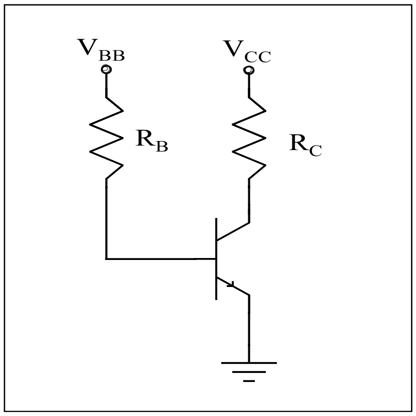
Other biasing options include various forms of passive biasing. This article discusses various passive biasing circuits, including their advantages and disadvantages.

Various BJT passive bias circuits

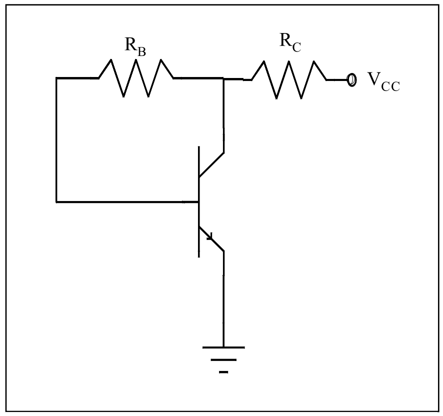
Passive biasing schemes usually consist of two to five resistors properly arranged about the transistor. Various passive biasing schemes are shown in Figure 1. The simplest form of passive biasing is shown as Circuit #1 in Figure 1. The collector current I_C is simply h_{FE} times the base current I_B. The base current is determined by the value of R_B. The collector voltage V_{CE} is determined by subtracting the voltage drop across resistor R_C from the power supply voltage V_{CC}. As the collector current is varied, the V_{CE} will change based on the voltage drop across R_C. Varying h_{FE} will cause I_C to vary in a fairly direct manner. For constant V_{CC} and constant V_{BE}, I_C will vary in direct proportion to h_{FE}. For example, as h_{FE} is doubled, collector current, I_C, will also double. Bias circuit #1 provides no compensation for variation in device h_{FE}.

Bias circuit #2 provides voltage feedback to the base current source resistor R_B. The base current source is fed from the voltage V_{CE}, as opposed to the supply voltage V_{CC}. The value of the base bias resistor R_B is calculated based upon nominal device V_{BE} and the desired V_{CE}. Collector resistor R_C has both I_C and I_B flowing through it.

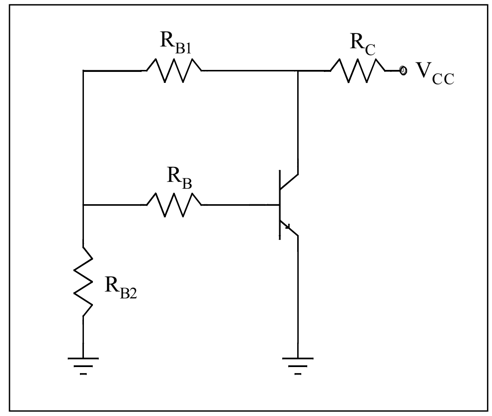
The operation of this circuit is best explained



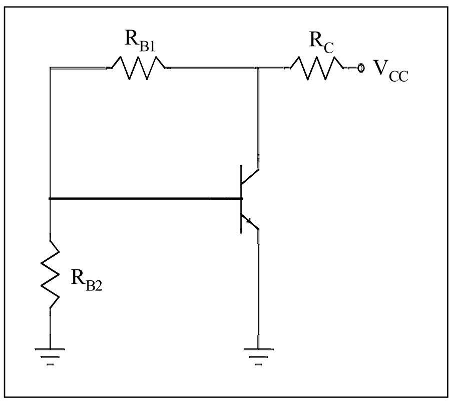
▲ **Figure 1(a). Circuit #1: nonstabilized BJT bias network.**



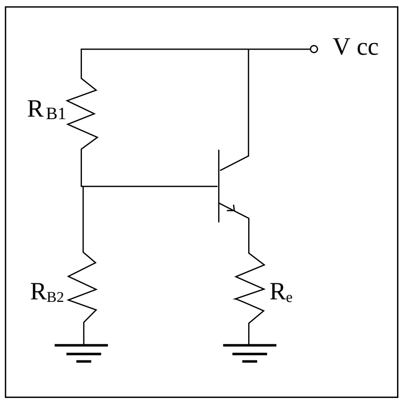
▲ **Figure 1(b). Circuit #2: voltage feedback BJT bias network.**



▲ **Figure 1(c). Circuit #3: voltage feedback with current source BJT bias network.**



▲ **Figure 1(d). Circuit #4: voltage feedback with voltage source BJT bias network.**



▲ **Figure 1(e). Circuit #5: emitter feedback BJT bias network.**

as follows. An increase in h_{FE} will tend to cause I_C to increase. An increase in I_C causes the voltage drop across resistor R_C to increase. The increase in voltage across R_C causes V_{CE} to decrease. The decrease in V_{CE} causes I_B to decrease because the potential difference across base bias resistor R_B has decreased. This topology provides a basic form of negative feedback which tends to reduce the amount that the collector current increases as h_{FE} is increased.

Bias circuit #3 has been discussed in past literature but predominately when very high V_{CC} (> 15 volts) and V_{CE} (> 12 volts) were used [1]. The voltage divider network consisting of R_{B1} and R_{B2} provide a voltage divider from which resistor R_B is connected. Resistor R_B then determines the base current. I_B times h_{FE} provides I_C. The voltage drop across R_C is determined by the collector current I_C, the base current I_B and the current consumed by the voltage divider, consisting of R_{B1} and R_{B2}. This circuit provides similar voltage feedback to that of bias circuit #2.

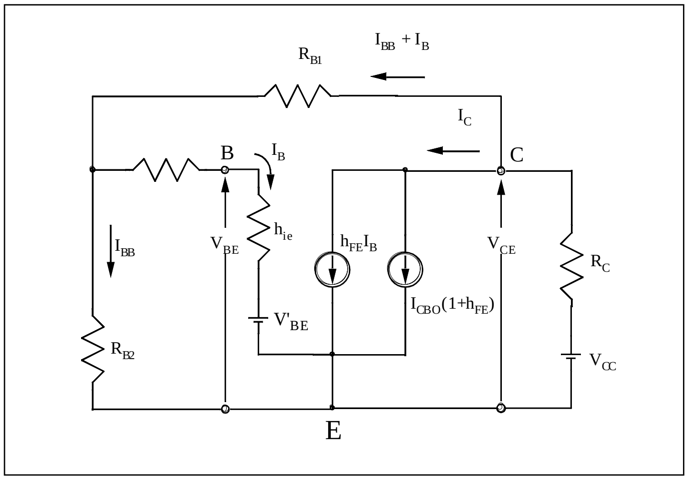
Bias circuit #4 is similar to bias circuit #3 with the exception that the series current source resistor R_B is omitted. This circuit is seen in bipolar power amplifier design with resistor R_{B2} replaced by a series silicon power diode providing temperature compensation for the bipolar device. The current flowing through resistor R_{B1} is shared by both resistor R_{B2} and the base emitter junction V_{BE}. The greater the current through resistor R_{B2}, the greater the regulation of the base emitter voltage V_{BE}.

Bias circuit #5 is the customary textbook circuit for biasing BJTs. A resistor is used in series with the device emitter lead to provide voltage feedback. This circuit ultimately provides the best control of h_{FE} variations from device to device and over temperature. The disadvantage of this circuit is that the emitter resistor must be properly bypassed for RF. The typical bypass capacitor often has internal lead inductance which can create unwanted regenerative feedback. The feedback can create device instability. Despite the problems associated with using the emitter resistor technique, this biasing scheme generally provides the best control on h_{FE} and over temperature variations.

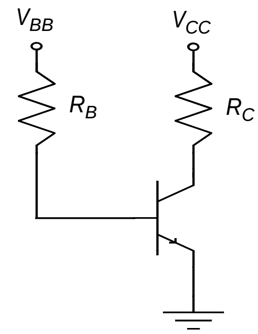
The sections that follow begin with a discussion of the BJT model and its temperature dependent variables. From the basic model, various equations are developed to predict the device's behavior over h_{FE} and temperature variations. This article is an update to the original article written by Kenneth Richter of Hewlett-Packard [2] and Hewlett-Packard Application Note 944-1 [3].

BJT modeling

The BJT is modeled as two current sources, as shown in Figure 2. The primary current source is $h_{FE}I_B$. In parallel is a secondary current source I_{CBO} $(1+\ h_{FE})$ that



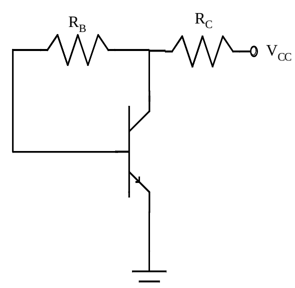
▲ **Figure 2. Gummel-Poon model of BJT with voltage feedback and constant base current source network.**



$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$I_C = \frac{h_{FE} .(V_{CC} - V'_{BE})}{h_{ie} + R_B} + I_{CBO} \cdot (1 + h_{FE})$$

▲ **Figure 3. Equations for nonstabilized bias network.**



$$R_B = \frac{V_{CE} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B}$$

$$I_C = \frac{h_{FE} \cdot (V_{CC} - V'_{BE}) + I_{CBO} \cdot (1 + h_{FE}).(h_{ie} + R_B + R_C)}{h_{ie} + R_B + R_C \cdot (1 + h_{FE})}$$

▲ **Figure 4. Equations for voltage feedback bias network.**

describes the leakage current flowing through a reverse biased PN junction. I_{CBO} is typically 1×10^{-7} A at 25 degrees C for an Agilent Technologies HBFP-0405 transistor. V'_{BE} is the internal base emitter voltage with h_{ie} representing the equivalent Hybrid PI input impedance of the transistor. h_{ie} is also equal to $h_{FE} / \lambda I_C$ where λ = 40 at +25 degrees C. V_{BE} will be defined as measured between the base and emitter leads of the transistor. It is equivalent to $V'_{BE} + I_B h_{ie}$. V_{BE} is approximately 0.78 volts at 25 degrees C for the HBFP-0405 transistor.

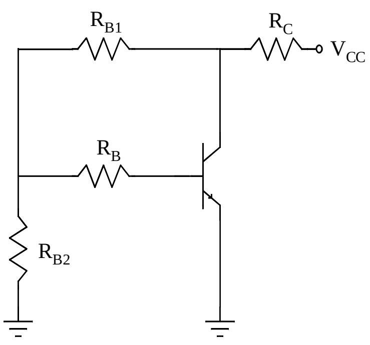
The device parameters that exhibit the greatest change as temperature is varied are h_{FE}, V'_{BE}, and I_{CBO}. These temperature dependent variables have characteristics which are process dependent and fairly well understood. h_{FE} typically increases with temperature at the rate of 0.5 percent/degrees C. V'_{BE} has a typical negative temperature coefficient of –2 mV/degrees C. This indicates that V_{BE} decreases 2 mV for every degree increase in temperature. I_{CBO} typically doubles for every 10 degree C rise in temperature. Each one of these parameters contributes to the net resultant change in collector current as temperature is varied.

For each bias network shown in Figure 1, several sets of simplified circuit equations have been generated to allow calculation of the various bias resistors. These are shown in Figures 3, 4, 5, 6 and 7. Each of the bias resistor values are calculated based on various design parameters such as desired I_C, V_{CE}, power supply voltage V_{CC} and nominal h_{FE}. I_{CBO} and h_{ie} are assumed to be zero for the basic calculation of resistor values.

Additional information, usually provided by the designer, is required for the three circuits that use the voltage divider consisting of R_{B1} and R_{B2}. For the bias network that uses voltage feedback with current source, the designer must choose the voltage across R_{B2} (V_{RB2}) and the bias current through resistor R_{B2}, which will be termed I_{RB2}. If $V_{CE} > V_{RB2} > V_{BE}$, then a suggested V_{RB2} would be 1.5 volts and a suggested I_{RB2} would be 10 percent of I_C, or 0.5 mA.

The voltage feedback with a voltage source network and the emitter feedback network also require that the designer choose I_{RB2}. The ratio of I_C to I_{RB2} can play a major role in bias stability.

An equation was then developed for each circuit that calculates collector current, I_C, based on nominal bias resistor values and typical device parameters, including h_{FE}, I_{CBO}, and V'_{BE}. MATHCAD 7 was used to help develop the I_C equation. Although the I_C equation begins simply, it develops into a rather lengthy equation



$$R_B = \frac{V_{RB2} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C + I_{B2} + I_B}$$

$$R_{B1} = \frac{V_{CE} - V_{RB2}}{I_{B2} + I_B} \qquad R_{B2} = \frac{V_{RB2}}{I_{B2}}$$

Designer must choose I_{B2} and V_{RB2} such that $V_{CE} > V_{RB2} > V_{BE}$

$$I_C = \left[\frac{-V'_{BE}\cdot(R_{B1}+R_{B2}+R_C) - R_{B2}\cdot[R_C\cdot I_{CBO}\cdot(1+h_{FE}) - V_{CC}]}{(R_B+h_{ie})\cdot(R_{B1}+R_{B2}+R_C) + R_{B2}\cdot(h_{FE}\cdot R_C + R_C + R_{B1})}\right]\cdot h_{FE} + I_{CBO}\cdot(1+h_{FE})$$

▲ **Figure 5. Equations for voltage feedback with current source bias network.**

for some of the more complicated circuits. MATHCAD helped to simplify this task.

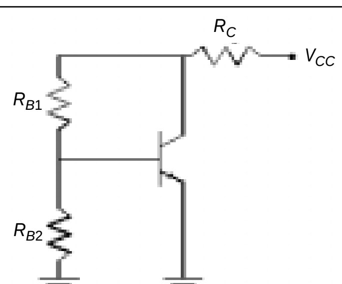
Design example using the Agilent HBFP-0405 BJT

The HBFP-0405 transistor is used as a test example for each of the bias circuits. The HBFP-0405 is described in [4] as a low noise amplifier for 1800 to 1900 MHz applications. The HBFP-0405 will be biased at a V_{CE} of 2.7 volts and a drain current I_C of 5 mA. A power supply voltage of 3 volts will be assumed. The nominal h_{FE} of the HBFP-0405 is 80. The minimum is 50 while the maximum is 150. The calculated bias resistor values for each bias circuit are described in Table 1.

With the established resistor values, I_C is calculated based on minimum and maximum h_{FE}. The performance of each bias circuit with respect to h_{FE} variation is shown in Table 2. Bias circuit #1 clearly has no compensation for varying h_{FE}, allowing I_C to increase 85 percent as h_{FE} is taken to its maximum. Circuit #2 with very simple collector feedback offers considerable compensation due to h_{FE} variations allowing an increase of only 42 percent. Circuit #3 offers very little improvement over circuit #2. Circuit #4 provides considerable improvement in h_{FE} control by only allowing a 9 percent increase in I_C. Circuit #4 offers an improvement over the previous circuits by providing a stiffer voltage source across the base emitter junction. As we will see later, this circuit has worse performance over temperature as compared to circuits #2 and #3. However, when both h_{FE} and temperature are considered, circuit #4 will appear to be the best performer for a grounded emitter configuration. As expected, circuit #5 provides the best control on I_C with varying h_{FE} allowing only a 5.4 percent increase in I_C. Results are power supply dependent, and with higher V_{CC}, results may vary significantly.

BJT performance over temperature

Since all three temperature dependent variables (I_{CBO}, h_{FE} and V'_{BE}) exist in the I_C equation, differentiating the I_C equation with respect to each of the parameters provides insight into their effect on I_C. The partial derivative of each of the three parameters represents a stability factor. The various stability factors and their calculation are shown in Table 3. Each circuit has three distinctly different stability factors which are then multiplied times a corresponding change in either V'_{BE}, h_{FE}, or I_{CBO} and finally summed. These changes or deltas in V'_{BE}, h_{FE}, and I_{CBO} are calculated based on



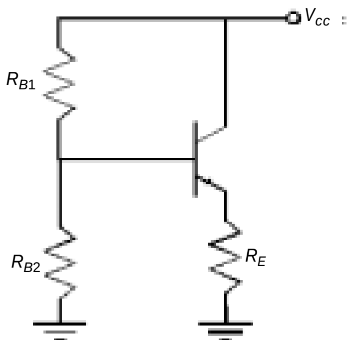
$$R_{B2} := \frac{V_{BE}}{I_{B2}} \qquad R_C := \frac{V_{CC} - V_{CE}}{I_C + I_B + I_{B2}}$$

$$R_{B1} := \frac{V_{CE} - (I_{B2}\cdot R_{B2})}{I_B + I_{B2}}$$

Designer must choose I_{B2}

$$I_C := \frac{-\left[\frac{-R_C}{h_{FE}}\cdot I_{CBO} - R_C\cdot I_{CBO} + \frac{R_C}{R_{B2}}\cdot V'_{BE} - \frac{R_C}{(R_{B2}\cdot h_{FE})}\cdot h_{ie}\cdot I_{CBO} - \frac{R_C}{R_{B2}}\cdot h_{ie}\cdot I_{CBO} - \frac{R_{B1}}{h_{FE}}\cdot I_{CBO} - R_{B1}\cdot I_{CBO} + \frac{R_{B1}}{R_{B2}}\cdot V'_{BE} - \frac{R_{B1}}{(R_{B2}\cdot h_{FE})}\cdot h_{ie}\cdot I_{CBO} - \frac{R_{B1}}{R_{B2}}\cdot h_{ie}\cdot I_{CBO} + V'_{BE} - \frac{1}{h_{FE}}\cdot h_{ie}\cdot I_{CBO} - h_{ie}\cdot I_{CBO} - V_{CC}\right]}{\left[R_C + \frac{R_C}{h_{FE}} + \frac{R_C}{(R_{B2}\cdot h_{FE})}\cdot h_{ie} + \frac{R_{B1}}{h_{FE}} + \frac{R_{B1}}{(R_{B2}\cdot h_{FE})}\cdot h_{ie} + \frac{1}{h_{FE}}\cdot h_{ie}\right]}$$

▲ **Figure 6. Equations for voltage feedback with voltage source bias network.**



$$R_E = \frac{V_{CC} - V_{CE}}{I_C\left(1 + \frac{1}{h_{FE}}\right)} \qquad R1 = \frac{V_{CC} - I_{B2} \cdot R_2}{I_{B2} + I_B}$$

Pick I_{B2} to be 10 percent of I_C, which is equal to .0005 A

$$R_2 = \frac{V_{RB2}}{I_{B2}} \qquad V_{RB2} = V_{BE} + (I_B + I_C) \cdot R_E$$

$$I_C := \frac{-\left[V_{BE} - \frac{1}{h_{FE}} \cdot h_{ie} \cdot I_{CBO} - h_{ie} \cdot I_{CBO} - \frac{R_E}{h_{FE}} \cdot I_{CBO} - R_E \cdot I_{CBO} + \frac{R_1}{R_2} \cdot V_{BE} - \frac{R_1}{(R_2 \cdot h_{FE})} \cdot h_{ie} \cdot I_{CBO} - \frac{R_1}{R_2} \cdot h_{ie} \cdot I_{CBO} - \frac{R_1}{R_2} \cdot \frac{R_E}{h_{FE}} \cdot I_{CBO} - \frac{R_1}{R_2} \cdot R_E \cdot I_{CBO} - \frac{R_1}{h_{FE}} \cdot I_{CBO} - R_1 \cdot I_{CBO} - V_{CC}\right]}{\left[\frac{1}{h_{FE}} \cdot h_{ie} + \frac{R_E}{h_{FE}} + R_E + \frac{R_1}{(R_2 \cdot h_{FE})} \cdot h_{ie} + \frac{R_1}{R_2} \cdot \frac{R_E}{h_{FE}} + \frac{R_1}{R_2} \cdot R_E + \frac{R_1}{h_{FE}}\right]}$$

▲ **Figure 7. Equations for emitter feedback bias network.**

variations in these parameters based on the manufacturing processes.

A comparison of each circuit's stability factors will certainly provide insight as to which circuit compensates best for each parameter. MATHCAD was again used to calculate the partial derivatives for each desired stability factor. The stability factors for bias circuit #1 are shown in Table 4. The stability factors for the remaining circuits are shown in the Appendix.

The change in collector current from the nominal design value at 25 degrees C is then calculated by taking each stability factor and multiplying it times the corresponding change in each parameter. Each product is then summed to determine the absolute change in collector current.

As an example, the collector current of the HBFP-0405 will be analyzed as temperature is increased from +25 degrees C to +65 degrees C. For the HBFP-0405, I_{CBO} is typically 100 nA at +25 degrees C and typically doubles for every 10 degrees C temperature rise. Therefore, I_{CBO} will increase from 100 nA to 1600 nA at +65 degrees C. The difference or ΔI_{CBO} will be 1600 – 100 = 1500 nA. The 1500 nA will then be multiplied times its corresponding I_{CBO} stability factor.

V'_{BE} at 25 degrees C was measured at 0.755 volts for the HBFP-0405. Since V'_{BE} has a typical negative temperature coefficient of –2 mV per degree C, V'_{BE} will be 0.675 volts at +65 degrees C. The difference in V'_{BE} will then be 0.675 – 0.755 = –0.08 volts. The –0.08 volts will then be multiplied by its corresponding V'_{BE} stability factor.

Resistor	Non-Stabilized Bias Network	Voltage Feedback Bias Network	Voltage Feedback with Current Source Bias Network	Voltage Feedback with Voltage Source Bias Network	Emitter Feedback Bias Network
R_C	140 Ω	138 Ω	126 Ω	126 Ω	
R_B	30770 Ω	19552 Ω	11539 Ω		
R_{B1}			889 Ω	2169 Ω	2169 Ω
R_{B2}			3000 Ω	1560 Ω	2960 Ω
R_E					138 Ω

▲ **Table 1. Bias resistor values for HBFP-0405 biased at V_{CE} = 2 volts, V_{CC} = 2.7 volts, I_C = 5 mA, h_{FE} = 80 for the various bias networks.**

Bias Circuit	Non-Stabilized Bias Network	Voltage Feedback Bias Network	Voltage Feedback with Current Source Bias Network	Voltage Feedback with Voltage Source Bias Network	Emitter Feedback Bias Network
I_c(mA)@ minimum h_{FE}	3.14	3.63	3.66	4.53	4.70
I_c(mA)@ typical h_{FE}	5.0	5.0	5.0	5.0	5.0
I_c(mA)@ maximum h_{FE}	9.27	7.09	6.98	5.44	5.27
Percentage change in I_c from nominal I_c	+85% –37%	+42% –27%	+40% –27%	+9% –9%	+5.4% –6%

▲ **Table 2. Summary of I_C variation versus h_{FE} for various bias networks for the HBFP-0405, V_{CC} = 2.7 volts, V_{CE} = 2 volts, I_C = 5 mA, T_j = +25 degrees C.**

$$I_{CBO} = \frac{\partial I_C}{\partial I_{CBO}} \quad h_{FE}, V'_{BE} = \text{constant}$$

$$V'_{BE} = \frac{\partial I_C}{\partial V'_{BE}} \quad I_{CBO}, h_{FE} = \text{constant}$$

$$h_{FE} = \frac{\partial I_C}{\partial h_{FE}} \quad I_{CBO}, V'_{BE} = \text{constant}$$

First calculate the stability factors for V'_{BE}, I_{CBO} and h_{FE}. Then, to find the change in collector current at any temperature, multiply the change from 25 degrees C of each temperature dependent variable with its corresponding stability factor and sum.

$$\Delta I_C = SI_{CBO} \times \Delta I_{CBO} + SV'_{BE} \times \Delta V'_{BE} + Sh_{FE} \times \Delta h_{FE}$$

▲ **Table 3. Calculation of the stability factors and their combined effect on I_C.**

Collector Current at any Temperature (I_C)	$\frac{h_{FE} \cdot (V_{CC} - V'_{BE})}{(h_{ie} + R_B)} + I_{CBO} \cdot (1 + h_{FE})$
I_{CBO} Stability Factor $I_{CBO} = \frac{\partial I_C}{\partial I_{CBO}} \Big\vert h_{FE}, V'_{BE} = \text{constant}$	$1 + h_{FE}$
V'_{BE} Stability Factor $V'_{BE} = \frac{\partial I_C}{\partial V'_{BE}} \Big\vert I_{CBO}, h_{FE} = \text{constant}$	$\frac{-h_{FE}}{h_{ie} + R_B}$
h_{FE} Stability Factor $h_{FE} = \frac{\partial I_C}{\partial h_{FE}} \Big\vert I_{CBO}, V'_{BE} = \text{constant}$	$\frac{V_{CC} - V'_{BE}}{h_{ie} + R_B} + I_{CBO}$

▲ **Table 4. Stability factors for non-stabilized bias network #1.**

h_{FE} is typically 80 at +25 degrees C and typically increases at a rate of 0.5 percent per degree C. Therefore, h_{FE} will increase from 80 to 96 at +65 degrees C, making Δh_{FE} equal to 96 – 80 = 16. Again the Δ is multiplied by its corresponding stability factor.

Once all stability terms are known, they can be summed to give the resultant change in collector current from the nominal value at +25 degrees C. The results of the stability analysis are shown in Table 5. The nonstabilized circuit #1 allows I_C to increase about 27 percent, while circuits 2 and 3 show a 19 to 20 percent increase in I_C. Somewhat surprising is that circuit #4 shows a nearly 30 percent increase in I_C with temperature because V'_{BE} is the major contributor to stability. This is probably due to the impedance of the R_{B1} and R_{B2} voltage divider working against V'_{BE}. Both circuits #2 and #3 have very similar performance over temperature. Both offer a significant improvement over circuit #1 and #4. Predictably, circuit #5 offers the best performance over temperature by nature of the emitter feedback. Emitter feedback can be used effectively if the resistor can be adequately RF bypassed without producing stability problems.

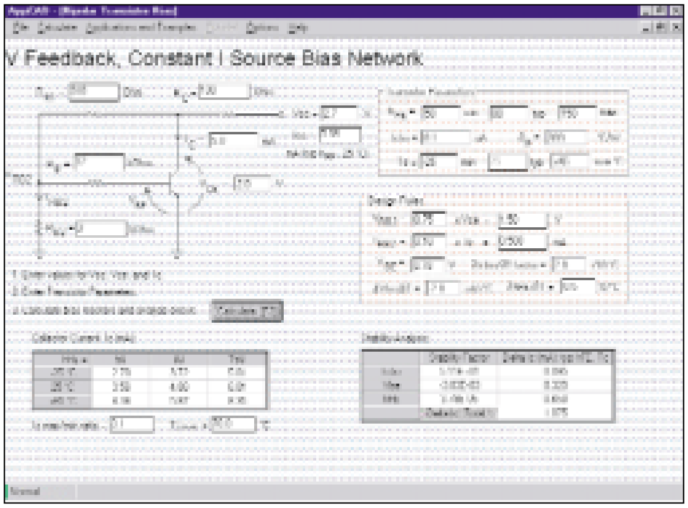
The degree of control that each bias circuit has on controlling I_C due to h_{FE} variations and the intrinsic temperature dependent parameters is defined by the design of the bias circuit. Increasing the voltage differential between V_{CE} and V_{CC} can enhance the circuit's ability to control I_C. In handset applications, this becomes difficult with 3-volt batteries as power sources. The current that is allowed to flow through the various bias resistors can also have a major effect on I_C control.

In order to analyze the various configurations, an AppCAD [5] module was generated. AppCAD consists of various modules developed to help RF designers with microstrip, stripline, detector, pin diode, MMIC biasing, RF amplifier, transistor biasing and system level calculations, as well as other design modules. The AppCAD BJT biasing module allows the designer to fine-tune each bias circuit design for optimum performance. AppCAD also allows the designer to input device variation parameters peculiar to a certain manufacturer's semiconductor process. A sample screen showing a typical bias circuit is shown in Figure 8. The data from AppCAD is used to create the graphs in the following sections.

The first exercise is to graphically illustrate the percentage

Bias Circuit	Non-stabilized	#2 Voltage Feedback	#3 Voltage Feedback w/Current Source	#4 Voltage Feedback	#5 Emitter Feedback
I_{CBO} stability factor	81	52.238	50.865	19.929	11.286
V'_{BE} stability factor	-2.56653×10^{-3}	-2.568011×10^{-3}	-3.956×10^{-3}	–0.015	-6.224378×10^{-3}
h_{FE} stability factor	6.249877×10^{-5}	4.031×10^{-5}	3.924702×10^{-5}	1.537669×10^{-5}	8.707988×10^{-6}
ΔI_C due to I_{CBO}(mA)	0.120	0.078	0.076	0.030	0.017
ΔI_C due to V'_{BE}(mA)	0.210	0.205	0.316	1.200	0.497
ΔI_C due to h_{FE}(mA)	0.999	0.645	0.628	0.246	0.140
Total I_C(mA)	1.329	0.928	1.020	1.476	0.654
Percentage change in I_C from nominal I_C	26.6%	18.6%	20.4%	29.5%	13.1%

▲ **Table 5. Bias stability analysis at +65 degrees C using the HBFP-0405, where V_{cc} = 2.7 volts, V_{CE} = 2 volts and I_c = 5 mA.**



▲ **Figure 8. Agilent Technologies AppCAD module for BJT biasing.**

change in I_C versus h_{FE}. AppCAD is used to calculate the resistor values for each of the five bias networks. The HBFP-0405 transistor is biased at a V_{CE} of 2 volts, I_C of 5 mA, and V_{CC} of 2.7 volts. Various values of h_{FE} are substituted into AppCAD; results are presented in Figure 9. The data clearly shows that the emitter feedback and voltage feedback with voltage source networks are superior to the remaining circuits with regards to controlling h_{FE} at room temperature. These networks provide a 4:1 improvement over the other two voltage feedback networks.

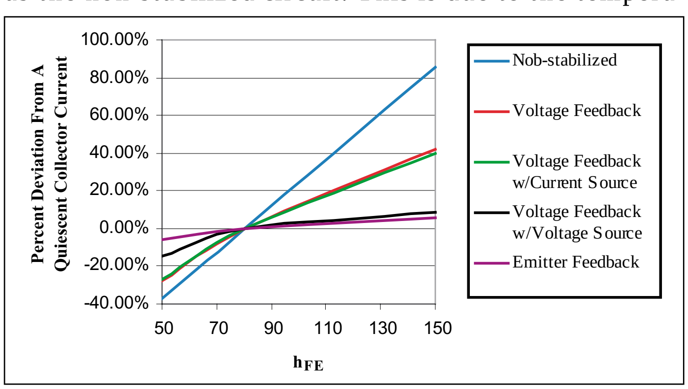
AppCAD is then used to simulate a temperature change from T_j = –25 de-grees C to +65 de-grees C with h_{FE} held constant. Whereas the original Matchcad analysis assumed that $T_c = T_j$, AppCAD takes into account that T_j is greater than T_c. AppCAD calculates the thermal rise based on DC power dissipated and the thermal impedance of the device. The results of the analysis are shown in Figure 10. The voltage feedback with voltage source network performed nearly as poorly as the non-stabilized circuit. This is due to the temperature induced V_{BE} decrease and the bias circuit trying to keep V_{BE} constant. Power bipolar designers will often utilize a silicon diode in place of R_{B2} so that the bias voltage will track the V_{BE} of the transistor. Depending on the impedance of the voltage divider network, V_{BE} could rise, causing I_C to increase. The emitter feedback network performed very well as expected. The simple voltage feedback network appeared to be optimum when considering the simplicity of the circuit.

Bias networks 3 through 5 make use of an additional resistor that shunts some of the total power supply current to ground. Properly chosen, this additional bias current can be used to assist in controlling I_C over temperature and h_{FE} variations from device to device. AppCAD is set up such that the designer has various choices regarding the amount of bias resistor current that is allowed to flow from the power supply. AppCAD is used to analyze each bias circuit.

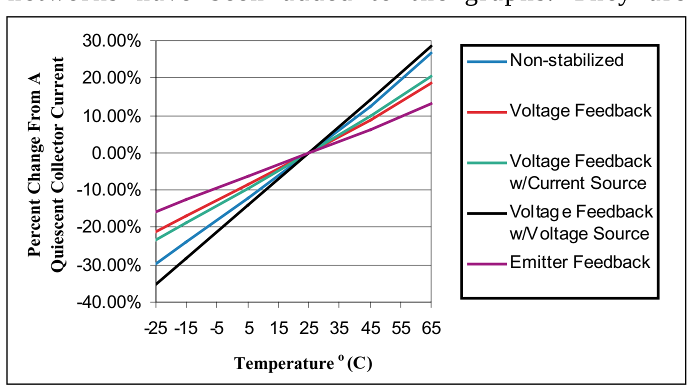
The graphs in Figures 11 and 12 plot the percentage change in I_C versus the ratio of I_C to I_{RB1}. I_{RB1} is the current flowing through resistor R_{B1}, which is the summation of base current I_B and current flowing through resistor R_{B2}. The maximum permissible ratio of I_C to I_{RB1} is limited by the h_{FE} of the transistor. Figure 11 represents the worst case condition, where I_C increases at maximum h_{FE} and highest temperature. Figure 12 shows the opposite scenario, in which the lowest I_C results from lowest h_{FE} and lowest temperature. The percentage change is certainly more pronounced at high h_{FE} and high temperature.

Although some of the predicted results are somewhat surprising, the bias network with emitter resistor feedback, as expected, offers the best performance overall. For a ratio of I_C to I_{RB1} of 10 to 1 or less, the resultant change in collector current is less than 20 percent. The voltage feedback with voltage source network performs best with an I_C to I_{RB1} ratio between 6 and 10 with a worst case change of 41 percent in collector current.

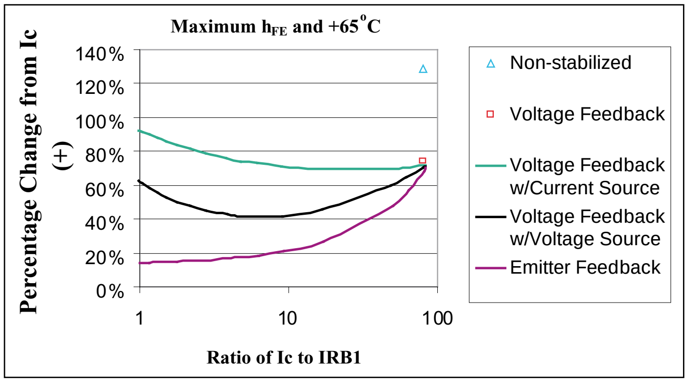
To complete the comparison, two additional points representing the nonstabilized and the voltage feedback networks have been added to the graphs. They are



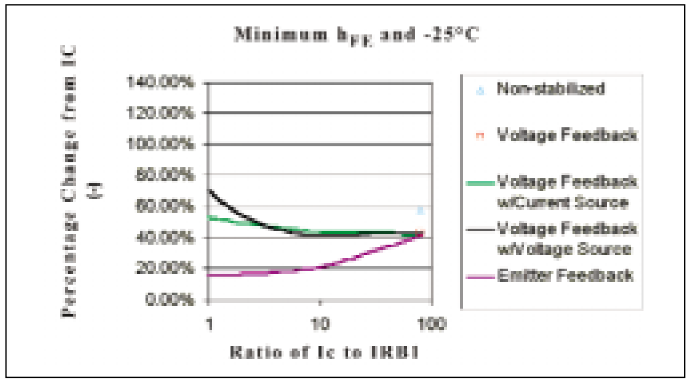
▲ **Figure 9. Percent change in quiescent collector current versus h_{FE} for the HBFP-0405 where V_{CC} = 2.7 volts, V_{CE} = 2 volts, I_C = 5 mA and T_j = +25 degrees C.**



▲ **Figure 10. Percent change in quiescent collector current versus temperature for the HBFP-0405 where V_{CC} = 2.7 volts, V_{CE} = 2 volts, I_C = 5 mA and T_j = +25 degrees C.**



▲ **Figure 11. Percent change in quiescent collector current versus ratio of I_C to I_{RB1} for maximum h_{FE} and T_j = +65 degrees C for the HBFP-0405, where V_C = 2.7 volts, V_{CE} = 2 volts and I_C = 5 mA.**



▲ **Figure 12. Percent change in quiescent collector current versus ratio of I_C to I_{RB1} for minimum h_{FE} and T_j = –25 degrees C for the HBFP-0405, where V_{CC} = 2.7 volts, V_{CE} = 2 volts and I_C = 5 mA.**

shown as single points because only the base current is in addition to the collector current. The nonstabilized network has an increase of 129 percent, while the voltage feedback network has an increase of 74.5 percent. The voltage feedback with current source network offers no benefit over the simpler voltage feedback network.

Conclusion

This article discussed the circuit analysis of four commonly used stabilized bias networks and one nonstabilized bias network for the bipolar junction transistor. In addition to the presentation of the basic design equations for the bias resistors for each network, an equation was presented for collector current in terms of bias resistors and device parameters. The collector current equation was then differentiated with respect to the three primary temperature dependent variables resulting in three stability factors for each network. These stability factors plus the basic collector current equation give the designer insight as to how best bias transistors for best performance over h_{FE} and temperature variations. The basic equations were then integrated into an AppCAD module, providing the circuit designer with an easy and effective way to analyze bias networks for bipolar transistors. ■

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Author information

Al Ward is an applications engineer with Agilent Technologies Wireless Semiconductor Division, 1410 E. Renner Road, Suite 100, Richardson, TX, 75082. He may be reached at 972-699-4369, or via e-mail at al_ward@agilent.com. Bryan Ward was a summer “SEED” student with Agilent Technologies.

Appendix

Collector Current at any Temperature (I_C)	$\dfrac{h_{FE}\cdot(V_{CC}-V'_{BE})+I_{CBO}\cdot(1+h_{FE})\cdot A}{h_{ie}+R_B+R_C\cdot(1+h_{FE})}$
I_{CBO} Stability Factor $I_{CBO}=\dfrac{\partial I_C}{\partial I_{CBO}}\Big\vert h_{FE}, V'_{BE}=\text{constant}$	$\dfrac{(1+h_{FE})\cdot A}{h_{ie}+R_B+R_C\cdot(1+h_{FE})}$
V'_{BE} Stability Factor $V'_{BE}=\dfrac{\partial I_C}{\partial V'_{BE}}\Big\vert I_{CBO}, h_{FE}=\text{constant}$	$\dfrac{-h_{FE}}{h_{ie}+R_B+R_C\cdot(1+h_{FE})}$
h_{FE} Stability Factor $h_{FE}=\dfrac{\partial I_C}{\partial h_{FE}}\Big\vert I_{CBO}, V'_{BE}=\text{constant}$	$\dfrac{V_{CC}-V'_{BE}+A\cdot I_{CBO}}{h_{FE}\cdot R_C+R_B+h_{ie}+R_C}-$ $\dfrac{R_C\cdot h_{FE}\cdot(V_{CC}-V'_{BE}+A\cdot I_{CBO})+A\cdot I_{CBO}}{(h_{FE}\cdot R_C+R_B+h_{ie}+R_C)^2}$ where $A=h_{ie}+R_B+R_C$

▲ **Stability factors for voltage feedback bias network #2.**

Collector Current at any Temperature (I_C)	$h_{FE}\left[\dfrac{-V'_{BE}\cdot A-R_{B2}\cdot\left[R_C\cdot I_{CBO}\cdot(1+h_{FE})-V_{CC}\right]}{(R_B+h_{ie})\cdot A+R_{B2}\cdot(h_{FE}\cdot R_C+R_C+R_{B1})}\right]+I_{CBO}\cdot(1+h_{FE})$
I_{CBO} Stability Factor $I_{CBO}=\dfrac{\partial I_C}{\partial I_{CBO}}\Big\vert h_{FE}, V'_{BE}=\text{constant}$	$(1+h_{FE})-\dfrac{R_{B2}\cdot h_{FE}\cdot R_C\cdot(1+h_{FE})}{A\cdot(R_B+h_{ie})+R_{B2}\cdot(h_{FE}\cdot R_C+R_C+R_{B1})}$
V'_{BE} Stability Factor $V'_{BE}=\dfrac{\partial I_C}{\partial V'_{BE}}\Big\vert I_{CBO}, h_{FE}=\text{constant}$	$\dfrac{-h_{FE}\cdot A}{(R_B+h_{ie})\cdot A+R_{B2}\cdot(h_{FE}\cdot R_C+R_C+R_{B1})}$
h_{FE} Stability Factor $h_{FE}=\dfrac{\partial I_C}{\partial h_{FE}}\Big\vert I_{CBO}, V'_{BE}=\text{constant}$	$\dfrac{h_{FE}\cdot\{R_{B2}\cdot R_C\cdot[(-R_{B2}\cdot V_{CC}+B)+R_{B2}\cdot R_C\cdot I_{CBO}\cdot(1+h_{FE})]\}}{D^2}-$ $\left[\dfrac{B+R_{B2}\cdot[R_C\cdot I_{CBO}\cdot(1+h_{FE})-V_{CC}+h_{FE}\cdot R_C\cdot I_{CBO}]}{D}\right]+I_{CBO}$ where $A=R_{B1}+R_{B2}+R_C$ $B=V'_{BE}\cdot(R_{B1}+R_{B2}+R_C)$ $C=(R_B+h_{ie})\cdot(R_{B1}+R_{B2}+R_C)$ $D=(R_B+h_{ie})\cdot(R_{B1}+R_{B2}+R_C)$ $+R_{B2}\cdot(h_{FE}\cdot R_C+R_C+R_{B1})$

▲ **Stability factors for voltage feedback with current source bias network #3.**

Collector Current at any Temperature (I_C)	$\frac{I_{CBO}\cdot(-A)+I_{CBO}\cdot h_{ie}\cdot(-B)+D-V_{CC}}{C}$
I_{CBO} Stability Factor $I_{CBO}=\frac{\partial I_C}{\partial I_{CBO}}\Big\vert h_{FE},V'_{BE}=\text{constant}$	$\frac{h_{ie}\cdot B+A}{C}$
V'_{BE} Stability Factor $V'_{BE}=\frac{\partial I_C}{\partial V'_{BE}}\Big\vert I_{CBO},h_{FE}=\text{constant}$	$\frac{\frac{-R_C}{R_{B2}}-\frac{R_{B1}}{R_{B2}}-1}{C}$
h_{FE} Stability Factor $h_{FE}=\frac{\partial I_C}{\partial h_{FE}}\Big\vert I_{CBO},V'_{BE}=\text{constant}$	$\frac{I_{CBO}\cdot\left[\frac{-R_C}{h_{FE}^2}-\frac{R_{B1}}{h_{FE}^2}\right]+I_{CBO}\cdot h_{ie}\cdot E}{C}-$ $\frac{I_{CBO}\cdot A+I_{CBO}\cdot h_{ie}\cdot B-D+V_{CC}}{C^2}\cdot\left[\frac{-R_C}{h_{FE}^2}-\frac{R_{B1}}{h_{FE}^2}+h_{ie}\cdot E\right]$ where: $A=\frac{R_C}{h_{FE}}+R_C+\frac{R_{B1}}{h_{FE}}+R_{B1}$ $B=\frac{R_C}{R_{B2}\cdot h_{FE}}+\frac{R_C}{R_{B2}}+\frac{R_{B1}}{R_{B2}\cdot h_{FE}}+\frac{R_{B1}}{R_{B2}}+\frac{1}{h_{FE}}+1$ $C=R_C+\frac{R_C}{h_{FE}}+\frac{R_{B1}}{h_{FE}}+h_{ie}\cdot\left[\frac{R_C}{R_{B2}\cdot h_{FE}}+\frac{R_{B1}}{R_{B2}\cdot h_{FE}}+\frac{1}{h_{FE}}\right]$ $D=\frac{R_C}{R_{B2}}\cdot V'_{BE}+\frac{R_{B1}}{R_{B2}}\cdot V'_{BE}+V'_{BE}$ $E=\frac{-R_C}{R_{B2}\cdot h_{FE}^2}-\frac{R_{B1}}{R_{B2}\cdot h_{FE}^2}-\frac{1}{h_{FE}^2}$

▲ **Stability factors for voltage feedback with voltage source bias network #4.**

Collector Current at any Temperature (I_C)	$$\frac{h_{ie}\cdot I_{CBO}\cdot(-A)+I_{CBO}\cdot(-B)+D}{C}$$
I_{CBO} Stability Factor $$I_{CBO}=\frac{\partial I_C}{\partial I_{CBO}}\Big\vert h_{FE},V'_{BE}=\text{constant}$$	$$\frac{h_{ie}\cdot A+B}{C}$$
V'_{BE} Stability Factor $$V'_{BE}=\frac{\partial I_C}{\partial V'_{BE}}\Big\vert I_{CBO},h_{FE}=\text{constant}$$	$$\frac{-1-\frac{R_1}{R_2}}{C}$$
h_{FE} Stability Factor $$h_{FE}=\frac{\partial I_C}{\partial h_{FE}}\Big\vert I_{CBO},V'_{BE}=\text{constant}$$	$$\frac{I_{CBO}\cdot E+h_{ie}\cdot I_{CBO}\cdot\left[\frac{-1}{{h_{FE}}^2}-\frac{R_1}{R_2\cdot {h_{FE}}^2}\right]}{C}-\frac{I_{CBO}\cdot B+h_{ie}\cdot I_{CBO}\cdot A-D}{C^2}\cdot\left[h_{ie}\cdot\left(\frac{-1}{{h_{FE}}^2}-\frac{R_1}{R_2\cdot {h_{FE}}^2}\right)+E\right]$$ where $$A=\frac{R_1}{R_2\cdot h_{FE}}+\frac{R_1}{R_2}+\frac{1}{h_{FE}}+1$$ $$B=\frac{R_1}{R_2}\cdot\frac{R_E}{h_{FE}}+\frac{R_1}{R_2}\cdot R_E+\frac{R_E}{h_{FE}}+R_E+\frac{R_1}{h_{FE}}+R_1$$ $$C=h_{ie}\cdot\left(\frac{1}{h_{FE}}+\frac{R_1}{R_2\cdot h_{FE}}\right)+\frac{R_E}{h_{FE}}+R_E+\frac{R_1}{R_2}\cdot\frac{R_E}{h_{FE}}+\frac{R_1}{R_2}\cdot R_E+\frac{R_1}{h_{FE}}$$ $$D=V'_{BE}+\frac{R_1}{R_2}\cdot V'_{BE}-V_{CC}$$ $$E=\frac{-R_E}{{h_{FE}}^2}-\frac{R_1}{R_2}\cdot\frac{R_E}{{h_{FE}}^2}-\frac{R_1}{{h_{FE}}^2}$$

▲ **Stability factors for emitter feedback bias network #5.**