A Low-Noise Amplifier for 2 GHz Applications Using the NE334S01 Transistor

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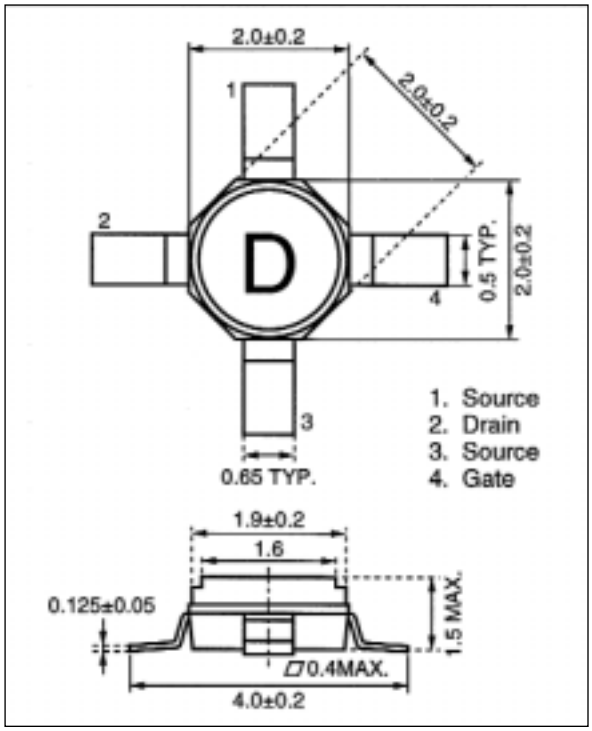
This article describes the design of a multiband, low-noise amplifier (LNA) using the NE334S01 from NEC. This device, originally intended for X-band use, was applied in this note for 2 GHz operation. It comes in an NEC S01 package and uses gallium arsenide (GaAs) heterojunction field effect transistor (HJ-FET) technology, which provides high gain and very low noise characteristics. This behavior makes it suitable for future communication standards such as W-CDMA (UMTS).

The design described here uses a bias voltage on either side of the transistor, i.e., gate and drain are each biased with its own voltage. Despite the need for a negative gate voltage, there are several advantages to biasing the device in the way shown, including good stability. The main goal of this design is to achieve unconditional stability over the entire frequency range. Therefore, no active (self-) bias circuitry is used.

Design overview

This design is an LNA input stage for the 2100 MHz frequency range. Goals of the design are gain (S_{21}) of higher than 15 dB, noise figure of about 1 dB, unconditional stability in the entire frequency range, current consumption of approximately 15 mA, low parts count and a small PCB area.

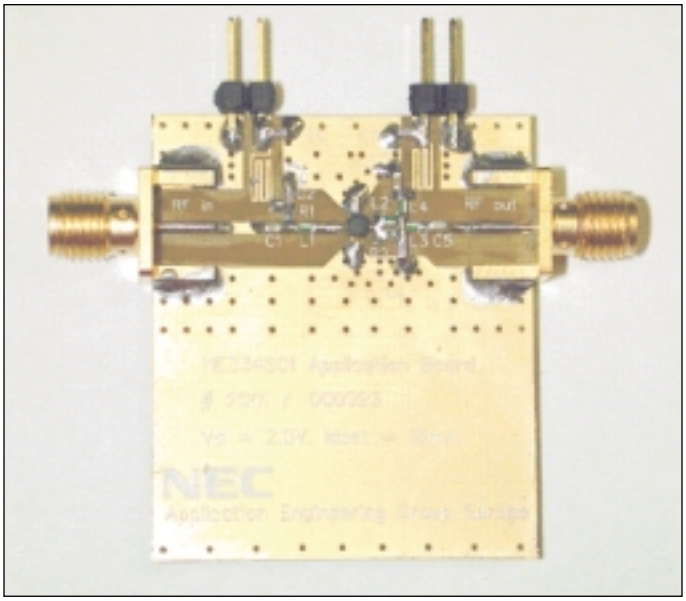
The goal of reaching unconditional stability over the entire frequency range makes this design especially challenging. According to the data sheet, when the NE334S01 is biased with 2 volts, 15 mA (the only bias condition given in the data sheet), the circuit is only unconditionally stable between 9 and 16 GHz. At 2 GHz, the stability factor (k) is 0.1.



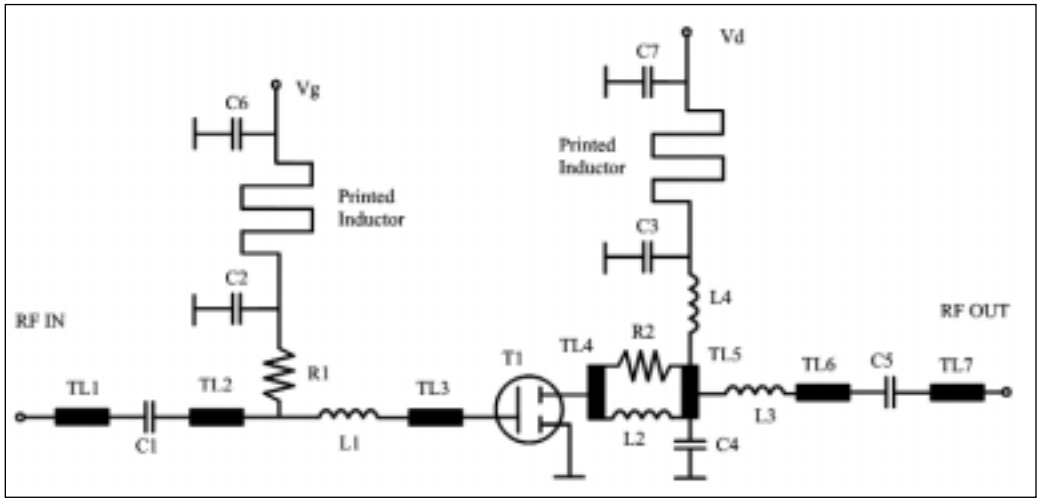
▲ **Figure 1. Package style, outline and pin configuration of NE334S01.**

Circuit description

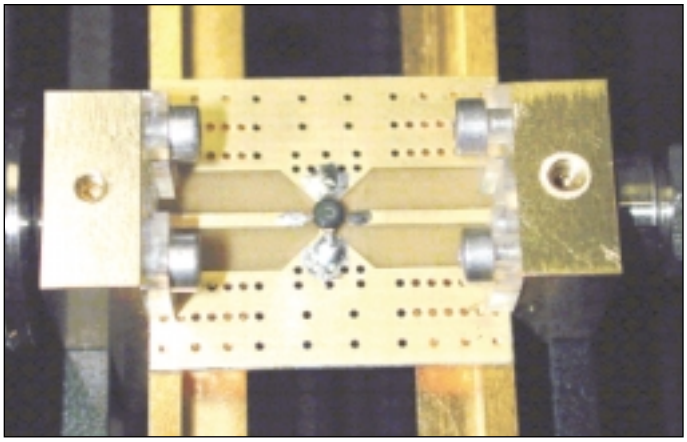
Figure 2 shows the LNA. The circuit is small in size (the area used for the LNA without SMA connectors is about 20 × 10 mm = 200 square mm). The schematic, shown in Figure 3, consists of input noise match, bias circuitry and output gain match. The transistor is directly soldered to ground without any inductive source loading. (In a prior design, inductive source loading was used, which also allows use of a self-bias topology. Oscillations were found at about 9



▲ **Figure 2. Application board of the low-noise amplifier.**



▲ **Figure 3. Schematic of the low-noise amplifier.**



▲ **Figure 4. Test board.**

to 10 GHz, due to the inductive source loading.)

The topology described here was chosen to obtain an unconditionally stable LNA at all frequencies. This circuit does not use a self-bias topology, and its gate must have proper voltage applied. The meander lines in the gate and drain bias branches are quarter-wave, 100-ohm microstrip lines at 2 GHz. They are grounded by capacitors, which leads to a better decoupling property of the DC supply.

C1 is needed for DC blocking; C2 and R1 apply negative input bias to the transistor. R1 is set to a high value (1 kohm) so that the overall noise figure is not increased significantly.

The noise match is formed with L1 and TL3. The datasheet gives the optimum source match at 2 GHz with Γ_{opt} = 0.77 ∠ 15 degrees. The match used here has a value of approximately 0.45 ∠ 41 degrees. In this application, a tradeoff is made between optimum noise figure and maximum gain.

Simulation shows that higher overall gain is achieved at 2 GHz when transistor input is matched to this point. The noise figure is only slightly increased. Also, the S_{21max} is shifted from almost 1.5 GHz (when matched with Γ_{opt}) to 2 GHz.

To keep the stability factor higher than 1 at in-band frequencies, it is necessary to slightly reduce the gain again. Thus, R2 was inserted.

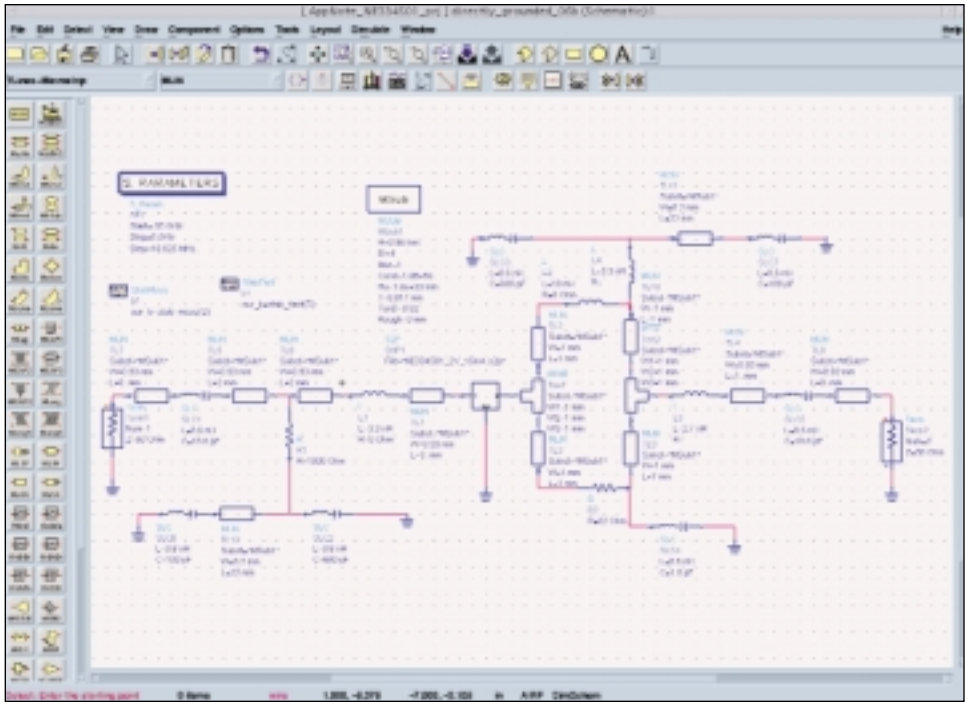
By choosing an appropriate value, k can be kept above 1. In this case, 68 ohms is sufficient. L2 bypasses DC and makes V_d independent of R2, in cases where a fixed I_d is required. L4 and C3 are part of the output bias circuitry. C4 and L3 are matching elements that allow a proper transformation to the final 50 ohms. Finally, C5 is a DC blocking cap.

Design flow

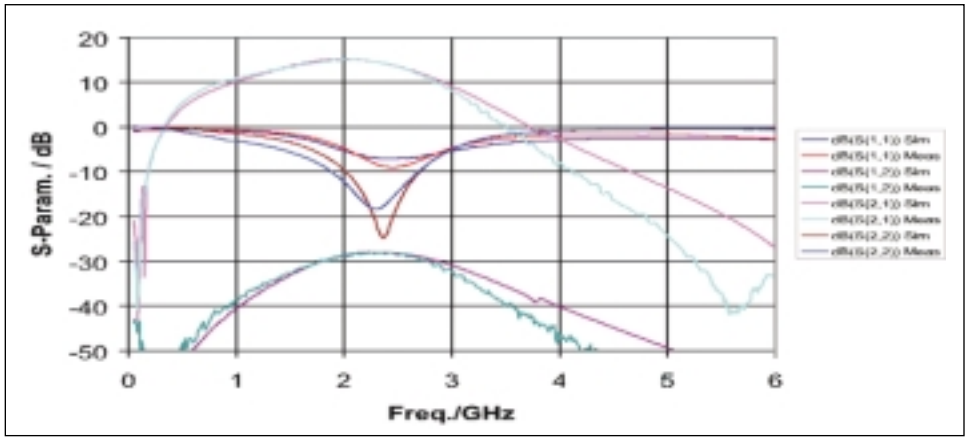
The design flow for this LNA is as follows:

- measure transistor and deembedding
- simulate resistive loading to ensure stability
- simulate and optimize input noise match
- simulate and optimize output gain match
- check overall performance and linearity

For this simulation, only measured *S*-parameters were used.



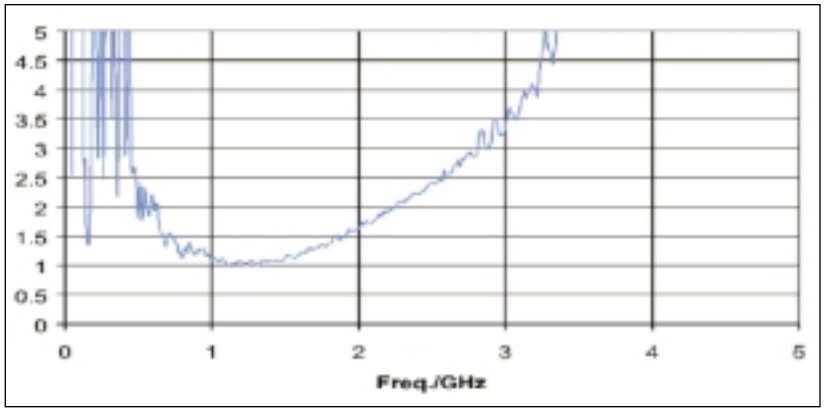
▲ **Figure 5. ADS schematic window.**



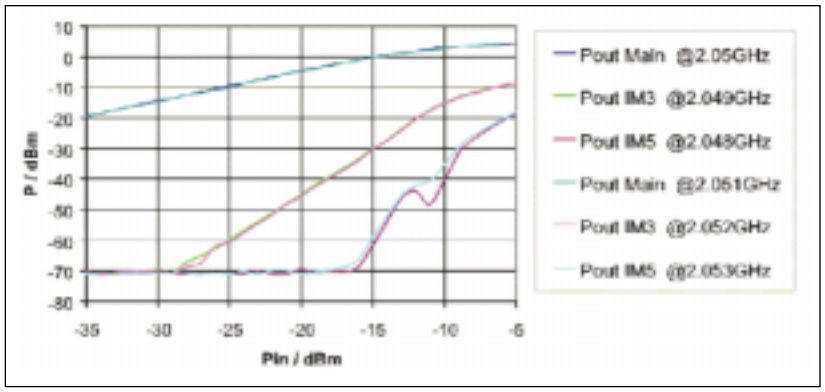
▲ **Figure 6. S-parameters (simulation versus measurement) up to 6 GHz.**

Starting point: The *S*-parameters of the device are measured on a test board specially designed for the S01 package (see Figure 4). The board substrate is FR4, with the same mechanic characteristics (thickness) as the final board. A special microwave test fixture (Model UTF by HMS) was used to connect the test board to the VNA. This test fixture provides a very low reflective transition from coaxial to microstrip and works through 10 GHz. For measurement deembedding, the VNA feature port extension was applied. Despite the use of this special microwave test fixture, some inaccuracies occur at higher frequencies. This is because board losses are not included and the dispersive behavior of the microstrip lines used is not taken into account. However, this procedure leads to valuable results. Measurement was taken at 2 volts, 15 mA, using the internal bias tees, up to 20 GHz.

Simulation of resistive loading to ensure stability: After determining the *S*-parameters of the transistor at 2-volt, 15 mA, the file can be transferred (as .s2p) to a suitable microwave simulator. In this case, Agilent's Advanced Design System is used. Resistors are placed, and the stability figures k and b_1 are calculated at the input and output. Next, the val-



▲ **Figure 7. *k*-Factor up to 6 GHz.**



▲ **Figure 8. Intermodulation characteristic.**

ues are changed until the minimum *k* is higher than 1.5 (here at approximately 1.5 GHz) to allow for a safety margin; b_1 has to be larger than 0 for the entire frequency range.

Simulation and optimization of input noise match: An inductor in series with a short transmission line (TL3) turns the 50-ohm input into the required source match. The initial value of the inductor (8.2 nH) is changed to a smaller value after the following step because of the above mentioned gain considerations.

Simulation and optimization of output gain match: The design of the output (drain) matching network depends on biasing, matching to the 50-ohm output and increased *k* factor, which improves the stability of the circuit.

Final check of overall performance and linearity: The circuit can now be built.

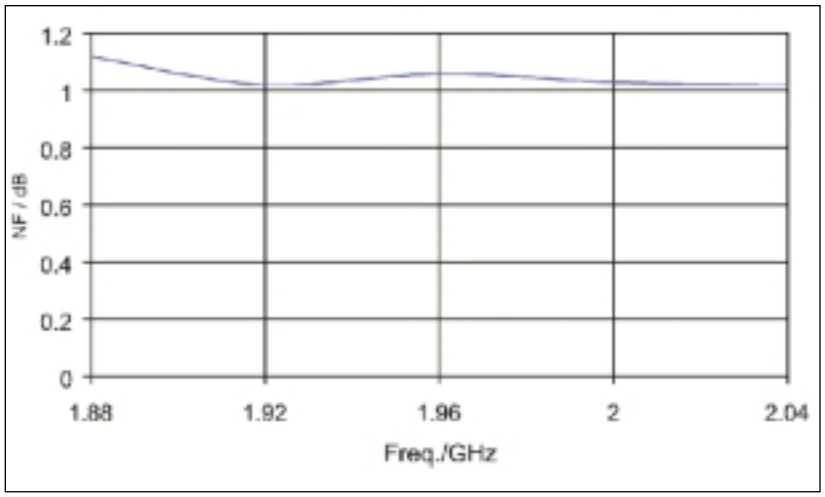
Simulation

A screenshot of the schematic is shown in Figure 5. The .s2p file is in the center of the graphic. Note that the resistors and inductors are lumped elements, but the 0603-size SMD capacitors are two elements connected together in series, consisting of a capacitor and an inductor.

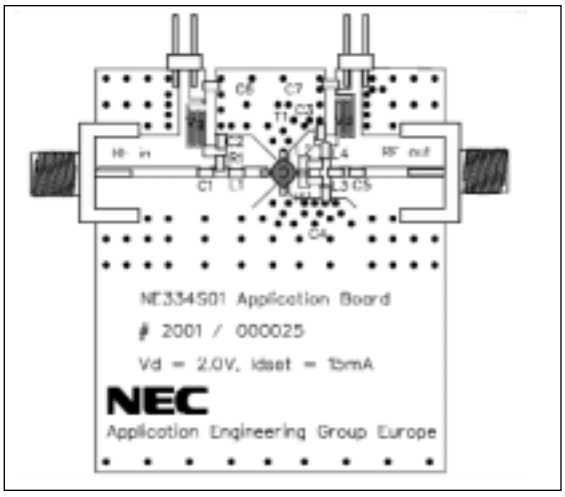
The equivalent circuit and the appropriate values are gathered from the manufacturer's datasheet. The inductor depends on the case size. In this case (using only 0603 SMD components), the value is 0.6 nH.

Measurement data

A comparison between simulation and measurements is shown in Figure 6. The simulated gain fits very well to the measurements. The correlation between simulated measurements in the frequency range of interest (1.8 to 2.4 GHz) is within 0.3 dB. The input and output reflection coefficients are showing a higher degree of deviation, but show a consistent behavior versus frequency. At higher frequencies, the deviation is also larger.



▲ **Figure 9. Measured noise figure.**



▲ **Figure 10. Layout and component placement.**

Des.	Size	Value	Manfgtr.	Part N0.
C1	0603	10 pF	Philips	NP0
C2	0603	680 pF	Philips	NP0
C3	0603	680 pF	Philips	NP0
C4	0603	1, 0 pF	Philips	NP0
C5	0603	10 pF	Philips	NP0
C6	0603	100 pF	Philips	NP0
C7	0603	100 pF	Philips	NP0
L1	0603	3, 9 nH	Susumu	
L2	0603	18 nH	Susumu	
L3	0603	2, 7 nH	Susumu	
L4	0603	3, 3 nH	Susumu	
R1	0603	1 k ohm	Rohm	
R2	0603	68 ohm	Rohm	
T1	S01	NE334S01	NEC	NEC NE334S01
J1, J2				3M
P1, 2		SMA		Johnson
PCB				#2001 000025

▲ **Table 1. Parts list.**

The overall unconditional stability is illustrated in Figure 7. The circuit shows unconditional stability over the entire frequency range. The plot only covers the range up to 6 GHz, but beyond this frequency the k-Factor does not reach 1 again. Also, b_1 is always positive, up to 20 GHz (not shown). The measured intermodulation characteristic of the circuit is given in Figure 8. From this measurement the OIP3 can be determined to 15.5 dBm. Signal spacing is set to 1 MHz, the two signals are set to 2.05 and 2.051 GHz. Noise figure is shown in Figure 9. This measurement in-cludes also the input SMA connector, so the real noise figure should be somewhat lower (approximately 0.1 dB).

Parts list and layout

The parts list is found in Table 1. The circuit layout with information on component placement, is given in Figure 10. ■

Author information

Ulrich Delpy received a diploma in electrical engineering from the University of Duisburg, Germany, in 1994. He worked at the IMST in Kamp-Lintfort, Germany, in development of planar antennas at 24 and 13 GHz and as a hybrid circuit designer. In 1999, he joined NEC Electronics (Europe) GmbH, in Duesseldorf, Germany. At NEC, he works in the Photonics and Microwave Business Unit. He can be contacted via E-mail: delpyu@ee.nec.de.