CMOS SOS for Mixed-Signal ICs

New process offers advantages for high-frequency and mixed-signal applications

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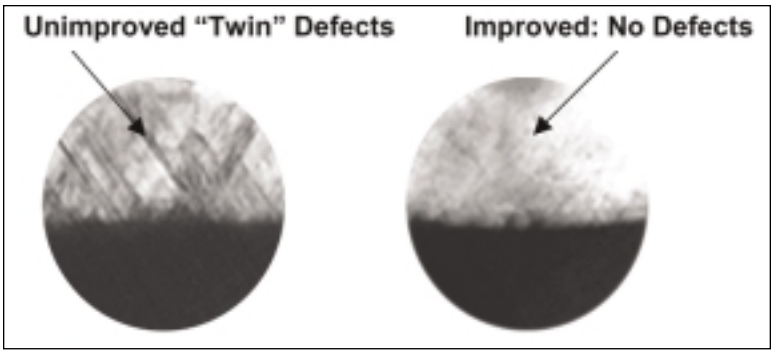
Silicon on sapphire (SOS) has long held great promise for mixed-signal applications but has never had high enough yields for commercial applications. Recent advances in growing a defect-free silicon layer on sapphire, however, have brought these yields to commercially viable levels. As a result, the advantages of fully depleted silicon-on-insulator complementary metal-oxide semiconductor (CMOS) technology for mixed-signal applications can finally be realized. These advantages include high frequency operation, excellent linearity and isolation and the ability to integrate high-quality passives directly onto integrated circuits (ICs). Less obvious advantages are the ability to integrate digital functionality, including EEPROM, to the circuits with no additional mask steps.

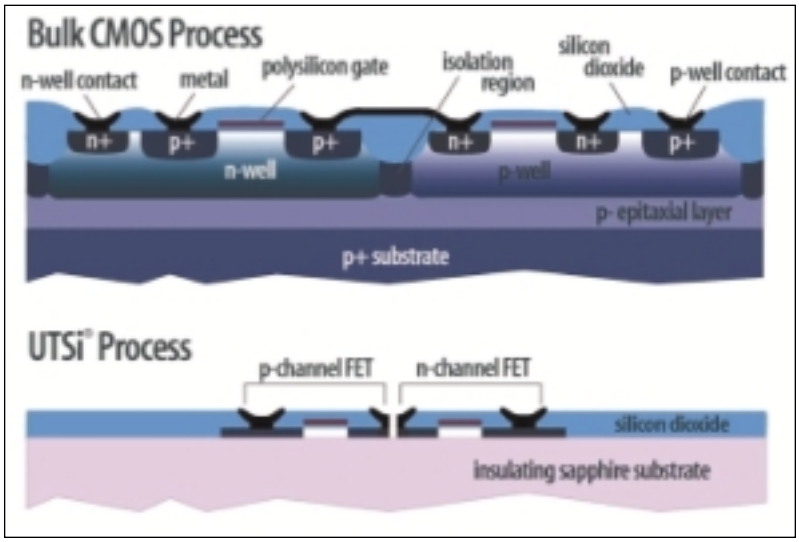


▲ **Figure 1. Photographs illustrating that annealing has removed defects in the silicon layer.**

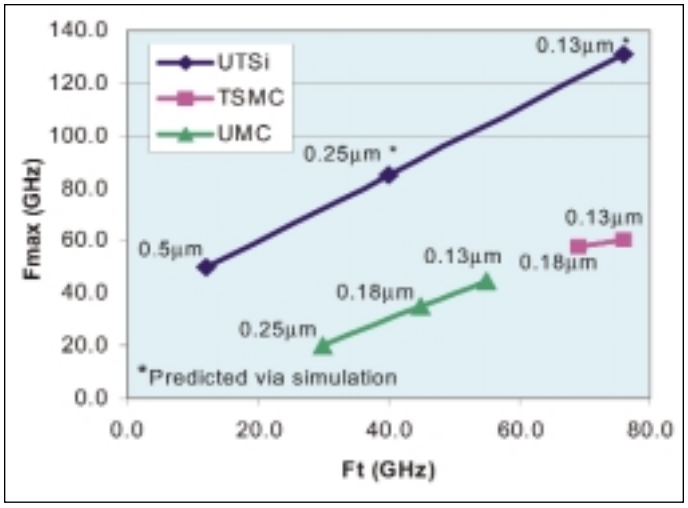
SOS has many of the transistor performance characteristics of gallium arsenide (GaAs) and silicon germanium (SiGe), but with the low power consumption and high yields of CMOS. It also has the ability to integrate greater functionality onto the circuits. This article describes the areas where CMOS SOS has advantages for mixed-signal applications and attempts to identify the niche in the competitive landscape that SOS belongs.

Technology review

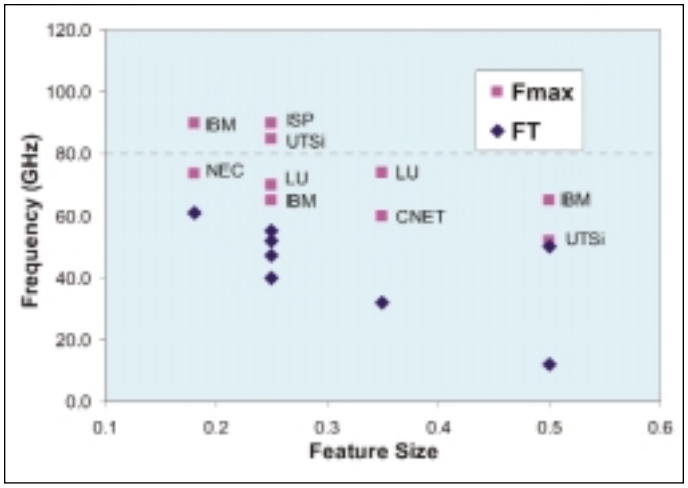
SOS, which was invented in the 1960s at Rockwell, was recognized immediately for its high speed and low power potential. In its original embodiment, poor crystalline quality resulted in very low yields and, therefore, high cost. Peregrine Semiconductor has since developed an ultra thin silicon (UTSi) process that eliminates these defects. Normal epi deposition of silicon on sapphire leaves dislocation defects in the silicon layer due to the lattice mismatch. SOS was brought to maturity by using a simple two-step improvement process that eliminates these defects. During the first step, silicon is implanted into the defective silicon layer, causing the bottom two-thirds of the silicon film to be amorphized. The second step consists of a thermal anneal and oxidation. Annealing allows silicon at the surface to regrow down into the amorphous region, producing defect-free silicon all the way to the sapphire substrate. Subsequent oxidation thins the film and an HF strip of the oxide leaves a high-quality UTSi film on a sapphire substrate. From there, CMOS circuitry is fabricated by a standard but simplified process flow, since the deep implants and guard regions are unnecessary thanks to the insulating sapphire substrate.



▲ **Figure 2. Film layer comparisons of bulk CMOS and UTSi processes.**



▲ **Figure 3. Ft versus Fmax for UTSi and Bulk CMOS.**



▲ **Figure 4. Ft versus Fmax versus feature size for SiGe processes.**

Trade space

The advantages of forming CMOS transistors in the UTSi layer over insulating sapphire include the following:

- elimination of substrate capacitance, which allows higher speed at lower power and avoids voltage dependent capacitance distortions,
- fully depleted operation, improving linearity, speed and low voltage performance and
- excellent isolation, which allows integration of multiple radio frequency (RF) functions without crosstalk.

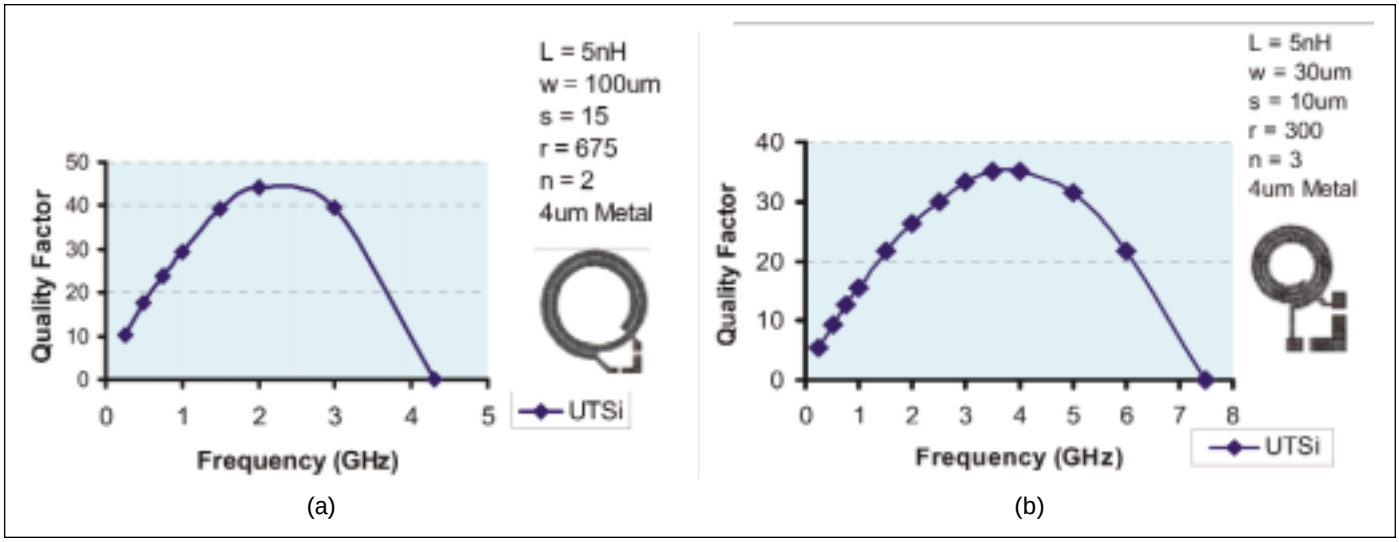
For RF and high-frequency mixed-signal applications, SOS offers a high Fmax compared to Ft. Fmax measures the ability of the technology to provide power gain, while Ft is primarily a function of gate length. Bulk processes typically have Fmax roughly equal to Ft, while the SOS process has Fmax roughly three times the amount of Ft. This allows the designer the freedom to design at higher frequencies for a given lithography or to design at a given frequency in a larger geometry technology. Comparing UTSi to bulk CMOS processes, the 0.5 µm UTSi process has an Fmax of 50 GHz, which is higher than bulk CMOS at 0.25 µm. At 0.25 µm, UTSi will have higher Fmax than bulk at 0.13 µm, which opens up design options at higher frequency (10 Gbps photonics, 5.7 GHz wireless). Larger geometry transistors can operate with higher breakdown voltages, thereby increasing the dynamic range of the circuits. UTSi at 0.25 µm is a 2.5-volt technology, whereas bulk at 0.13 µm operates at 1.2 volts.

When comparing to SiGe BiCMOS, the trade space is more complex. Multiple process options are available for the designer ranging from the highest frequency technology, which uses the bipolar transistors for speed but consumes greater power to lower power processes, which use more of the CMOS attributes at the expense of speed. In general, SOS performance is in the upper speed range for a given geometry, but it has significantly lower power because it is a true CMOS process.

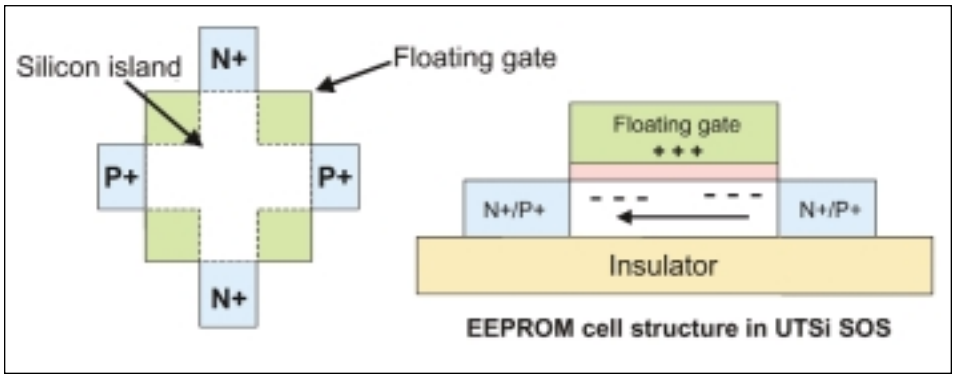
The trade of SOS versus other technologies hinges on more than just the speed and power. Because of the insulating properties of the substrate, multiple functions, including high-quality passives (inductors and capacitors), can be integrated onto the chips.

By using a thick top metal, inductors with *Q*s in the 40 to 50 range are possible at frequencies up to 5 GHz. These compare to *Q*s of below 10 in bulk CMOS. When combined with high *Q* MIM capacitors, very high performance tuned elements, matching circuits, oscillator tanks and transformers are possible.

Further integration of multiple active functions on single die is enabled because of the isolation provided by



▲ **Figure 5. Quality factor (*Q*) versus frequency for (a) large and (b) small spiral inductors in the UTSi process.**



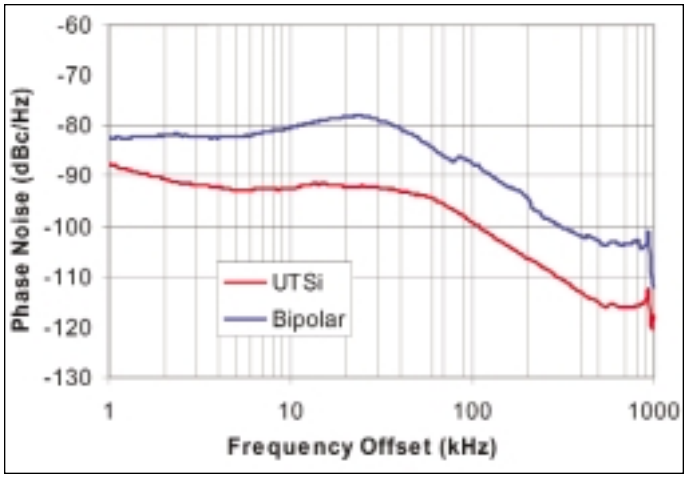
▲ **Figure 6. Cross-channel EEPROM cell structure in UTSi SOS.**

the sapphire substrate. Since virtually no current flows through the substrate, the dominant crosstalk terms are due to metal to metal coupling, which can be dealt with in a highly predictable manner during layout. This allows close packed layouts of RF functions, and can lead to very compact designs for integrated functions like in-phase and quadrature (I and Q) modulators and demodulators or *n* by *m* switches.

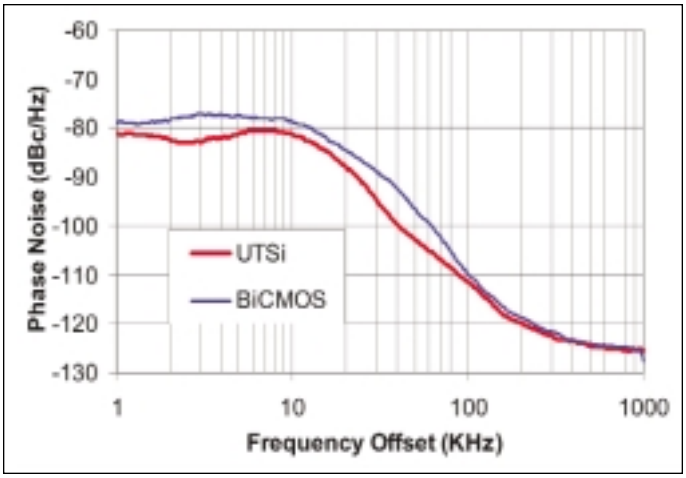
Another outgrowth of the excellent isolation is the ability to combine digital and RF functions on the same chip without detrimental crosstalk. SOS at 0.5 µm and 0.25 µm geometries is poorly suited for million gate digital functions, but modest digital logic up to the 100,000 gate class yields very well in this technology. This allows the inclusion of control and interface functions on the same chip as the mixed signal functions, often eliminating the need for separate chips. Another advantage is the ability to include electrically erasable programmable read-only memory (EEPROM) on chip with no additional masking steps. A simple crossed channel structure using a floating gate provides a low-complexity, high-density, non-volatile memory cell. By driving either positive or negative charge into the gate, one of the crossed channels is turned on (i.e., when the gate is charged positive, electrons are allowed to flow through the intrinsic layer below the gate). Up to several thousand bits of EEPROM can be included to mixed signal chips with little area penalty. This allows electrical setting of bias points, center frequencies or other control functions without having to include a microcontroller.

An area where SOS suffers is in-phase noise, particularly 1/f flicker type. Since the core technology used is CMOS metal semiconductor field-effect transistors (MESFETs), the close in-phase noise performance suffers in comparison to bipolar junction transistors. The lack of substrate effects does give SOS very sharp rise times, which can be used in the circuit design to overcome some of the deficiencies. These generally take the form of differential current mode designs that have been at the core of low-phase noise designs to date. In addition, the ability to integrate high-quality passives helps in the design of resonant circuits, used in oscillators. When the ultimate performance parameter is phase noise, however, inclusion of bipolar transistors, perhaps flip chipped onto the sapphire die itself, is warranted.

Another trade is the cost of SOS versus other technologies, particularly tighter geometry bulk CMOS and SiGe, plus GaAs for mixers and switches. The comparison hinges on two issues: the cost of the starting material and the cost of the wafer processing. In general, other issues of design, test and packaging are fairly



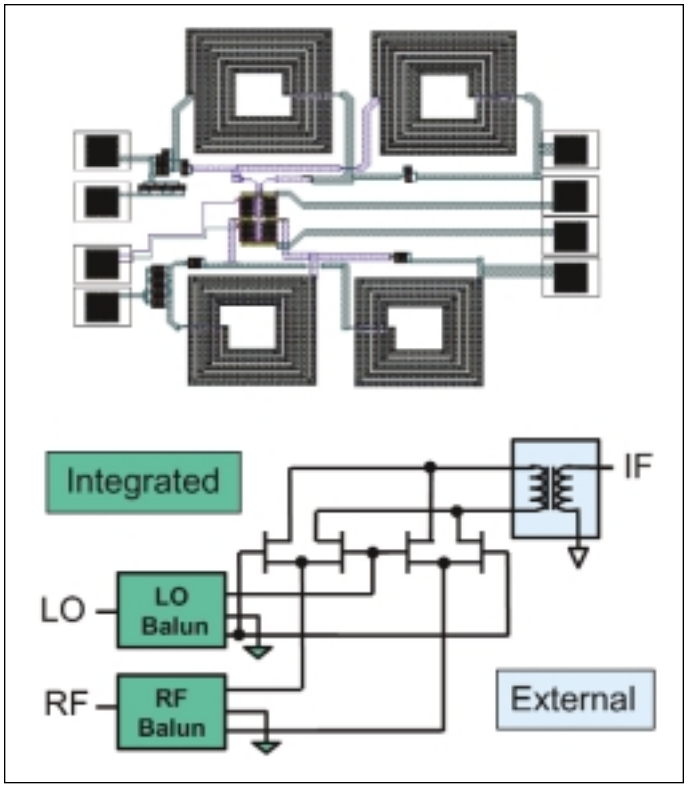
▲ **Figure 7. Integer N PLL phase noise.**



▲ **Figure 8. Fractional N PLL phase noise.**

insensitive to the choice of technology, with the exception that UTSi allows tighter layouts due to reduced crosstalk, which in some cases can be significant.

The starting material for UTSi is sapphire, which is produced in large volume for blue lasers. Six-inch material is readily available and is coming down in price as the volumes increase. The wafer processing costs for UTSi after the silicon layer is deposited are somewhat less than bulk processes, due to the lack of deep implants. Compared to SiGe, the difference in processing is even greater because of the extra masking steps needed for BiCMOS.



▲ **Figure 9. Integrated high linearity tuned mixer.**

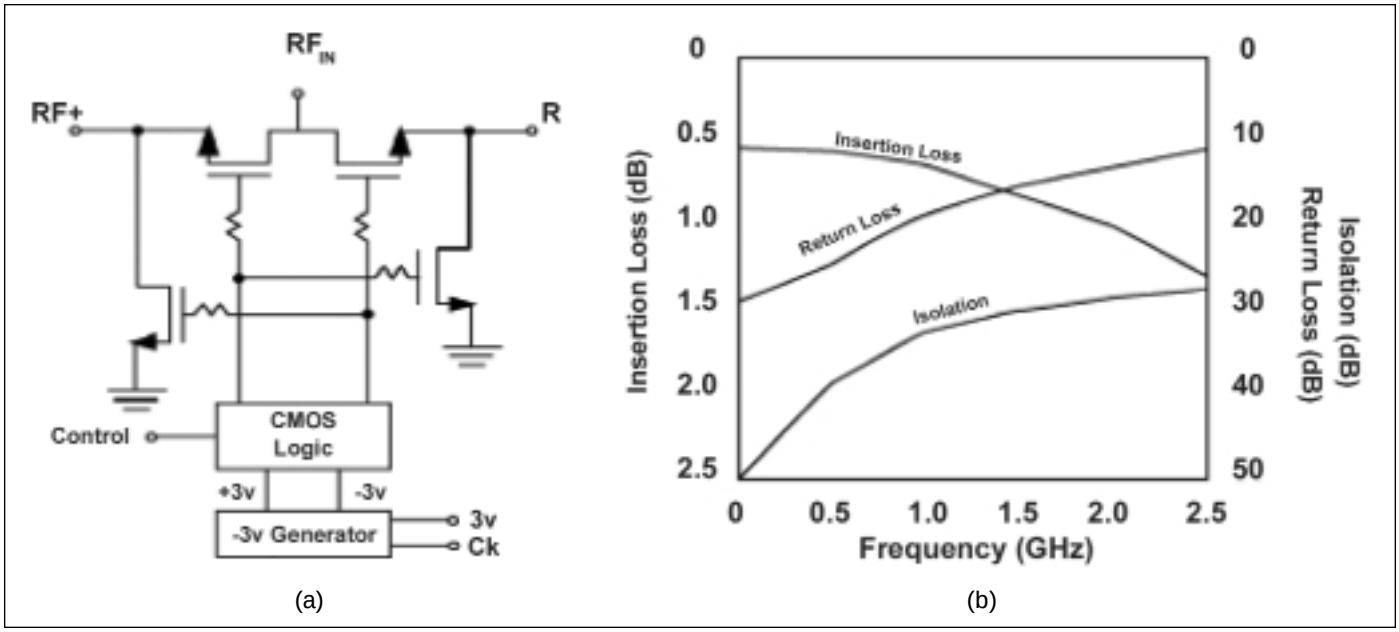
Based on Fabless Semiconductor Association (FSA) *Q*1 2001 pricing data, UTSi is the same price per square millimeter as bulk silicon CMOS from the major foundries. Factors responsible for achieving this are: the higher starting material cost for sapphire is offset by the simplified process and the lower cost of owning and operating a six-inch 0.25 micron versus an eight-inch deep sub-micron fab. Compared to SiGe, UTSi is less costly by about 40 percent, largely due to extra processing steps and yield issues. Compared to GaAs, UTSi is less costly by as much as 70 percent.

In deriving these estimates, the processes are assumed to be appropriate for mixed signal design of the class of parts described here (i.e., double poly) and the wafer sizes are assumed to be eight inches for bulk and SiGe, six inches for SOS and four inches for GaAs. Although these cost differences are significant, for the types of parts described here they amount to less than $.01 for small parts (i.e., mixers) and about $.10 for larger parts (i.e., phase-locked loop (PLL)).

For all but the largest volume handset parts, these costs represent a small fraction of the average selling price total cost of the product. Our conclusion is that the actual cost differences are often less important than the performance advantages in sensitive mixed-signal designs. It may not be possible to achieve the isolation and linearity in silicon-based technologies and the cost issue becomes secondary.

UTSi capacity

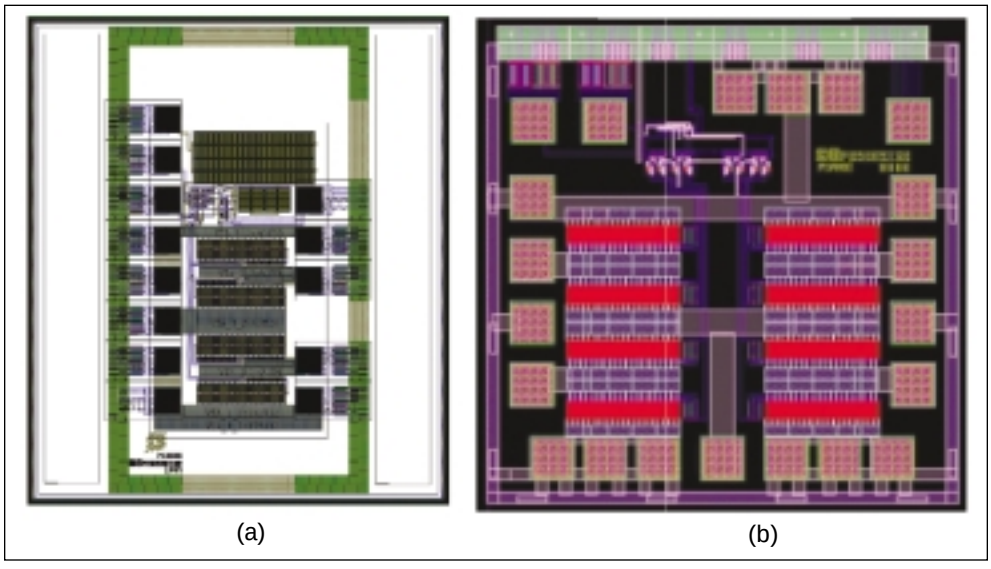
The availability and capacity of the UTSi process also is a discussion topic. Currently, the process is running in a six-inch, 24/7 facility in Sydney, Australia. The capacity of this facility is currently 3,000 six-inch wafers per month, and an on-going upgrade to 0.25 µm includes increasing the capacity to 5,000 wafers per month. These quantities are currently adequate since typical designs have between 1,000 and 10,000 sites per wafer,



▲ **Figure 10. (a) Integrated RF switch functions and (b) integrated RF switch performance. Switch desgins in UTSi, exhibiting very high isolation due to the insulating substrate, can be combined with on-chip control and negative voltage generation to produce a family of highly integrated switches.**

and the yields are greater than 95 percent for the high-volume products. Like most mixed-signal processes, the issue is not large wafer volumes but rather performance and cycle times. The fab is currently running five weeks typical and three weeks hot lot cycles, which allows both rapid design cycles and fast production turnaround.

For high-volume handset products, the capacity would have to be increased — most likely in a separate facility — to provide independent supply sources. Since this process is standard CMOS, bringing up another fab would be straightforward.



▲ **Figure 11. (a) A single-pole double-throw switch layout and (b) a single-pole four-throw switch layout.**

Wireless products

UTSi SOS products are in volume production for wireless applications. The initial products were a family of PLL ICs. These included both integer N and fractional N designs for both the infrastructure and handset markets. Initial penetrations of the products were the result of excellent phase noise performance for infrastructure applications. The first plot in Figure 7 shows the phase noise of this integer-N part compared to the bipolar part it replaced. This level of phase noise is still among the best available. The plot in Figure 8 shows the phase noise of a fractional-N low-power part compared to a BiCMOS competitive part. The SOS part roughly matches the BiCMOS part in both phase noise and power consumption.

Both of these parts utilized the 0.5 µm UTSi process. Subsequent design releases in this family have taken the frequency above 3 GHz, with prescalars running above 5 GHz. As the 0.25 µm process comes online in mid-2002, the PLL products extend the operating frequency to 8 GHz and further reduced the power consumption. By taking advantage of the ability to integrate EEPROM, next generation parts will

include a family of PLLs where the designer is able to electrically select and program the synthesizer frequency at the time of deployment and have it stay tuned to that frequency until it is reprogrammed. This eliminates the need for a microcontroller in fixed-frequency radios and allows a single-part type to be stocked for a wide variety of fixed local oscillator (LO) applications.

The second group of products that emerged as applications for SOS were a family of high-linearity mixers. Because there is no depletion region into the substrate, there are no nonlinear voltage-dependent capacitance effects from the source and drain to the substrate. When these terms are absent, the linearity — as measured by IP3 — is world-class. Quad field-effect transistors (FET) mixer die made in UTSi are at the heart of the family of high-linearity mixers being offered by MiniCircuits. IP3s as high as +38 dBm are available using Peregrine's UTSi mixer core in a hybrid package with discrete baluns. By taking advantage of the ability to integrate passives, a family of tuned mixers with integrated RF and LO baluns are in early sampling.

The performance of these ICs is exceptional, realizing an IP3 of +31 dBm, while simultaneously shrinking the size (these devices are packaged in a tiny, 8-pin thin small outline package (TSOP)) and lowering the cost of production. By building up the mixer core through first metal, any combination of RF and LO baluns can be added in the top metal layer, allowing a form of RF gate array where a custom mixer can be produced with a simple metal mask change.

We believe that SOS is able to produce the best performing mixers on the market. Future products will combine multiple mixers and passives on the same substrate to generate complex modulators and demodulators, and integrated LO and RF amps with the mixers to produce tuned frequency conversion blocks.

The third family of products based on the UTSi capabilities is a family of high-isolation switches. The initial products are single-pole, double-throw switches, which have a high isolation of 29 dB at 2 GHz and a low insertion loss. Because of the isolation and integration capabilities of SOS, a negative 3-volt source can be integrated onto the chip allowing the use of a single supply.

Derivative parts from this initial base are series switches with improved isolation and wider *n* by *m* configurations. These parts replace module switches with multiple pin diodes or ICs and offer a new generation of integrated high-performance switches.

Summary

SOS has come of age, in part because of the UTSi process breakthrough which produces a defect-

free silicon layer and, in part, because of the technology's integration advantages. UTSi SOS has some unique properties, which make it attractive for RF and mixed-signal integrated circuits. These include:

- excellent high-frequency performance, with Fmax typically three times Ft,
- the elimination of substrate capacitance effects,
- high-quality integrated passive elements,
- low levels of crosstalk,
- exceptional linearity, particularly in mixer applications,
- exceptional isolation, particularly in switch applications, and
- integrated analog and digital functionality, including EEPROM.

The cost of the technology is comparable to bulk CMOS and is less than SiGe and GaAs. As a result, for mixed-signal products where the insulating substrate and integrated passives enable better performance and higher levels of functionality, SOS offers significant competitive advantage. ■

Author information

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