Design of a Low-Voltage 5 to 6 GHz Voltage-Controlled Oscillator for 802.11 Applications

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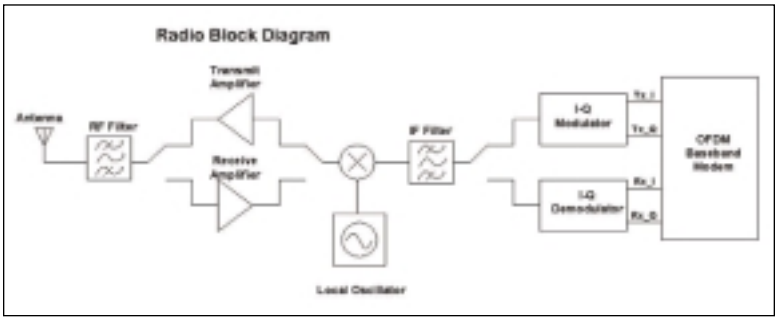
In response to the growing demand for high-speed, wireless networks, 300 MHz of unlicensed bandwidth has been allocated by the Federal Communications Commission (FCC) for the unlicensed national information infrastructure (U-NII), as shown in Table 1.



▲ **Figure 1. Typical radio block diagram for an 802.11A WLAN.**

The U-NII bands are well suited for high-speed wireless local area network (LAN) standards, such as the IEEE 802.11a. The operational restrictions for the U-NII bands are unique in that any modulation scheme can be used as long as the peak power limits are not exceeded. This affords the radio frequency (RF) system designer flexibility because the allowable modulation techniques are not limited to spread spectrum as in other unlicensed bands, such as industrial, scientific and medical (ISM). The IEEE 802.11a standard specifies orthogonal frequency division multiplexing (OFDM). The OFDM modulation approach uses several narrowband transmissions. Figure 1 illustrates a typical OFDM radio architecture used for IEEE 802.11a.

Frequency Band	Frequency Range	Peak Power Up to 20 MHz
U-NII Lower Band	5.150-5.250 GHz	2.5 mW/MHz
U-NII Middle Band	5.250-5.350 GHz	12.5 mW/MHz
U-NII Upper Band	5.725-5.825 GHz	50 mW/MHz

▲ **Table 1. U-NII bands.**

One of the most critical components in an 802.11a transceiver is the voltage-controlled oscillator (VCO). A VCO is required as a local oscillator to tune the transceiver to a specific channel within the operating band. In the 802.11a case, the channel spacing is 20 MHz with 48 312.5 kHz subcarriers. The channel frequency could be one of several available between 5.15 to 5.25, 5.25 to 5.35 or 5.725 to 5.825 GHz.

Although the actual operating frequency range of the VCO will depend on the overall radio design, most transceivers utilize the heterodyning architecture illustrated in Figure 1, in which the RF carrier is downconverted to an intermediate frequency (IF). Typical IF frequencies are 70 to 500 MHz. The required VCO frequency is either the sum (high-side injection) or difference (low-side injection) of the IF and RF frequencies. In either case, the VCO must operate near 5 to 6 GHz, depending on the band of operation.

By carefully analyzing the performance requirements for this VCO and using low-risk design techniques, a low-cost integrated solution can be achieved.

Rate (Mbits/sec)	Modulation	Symbol Rate	Sub-carrier Symbol Rate
6	BPSK	12	0.25
9	BPSK	12	0.25
12	QPSK	12	0.25
18	QPSK	12	0.25
24	16 QAM	12	0.25
36	16 QAM	12	0.25
48	64 QAM	12	0.25
54	64 QAM	12	0.25

▲ **Table 2. Summaries of the bit rate, symbol rate and modulation for 802.11a.**

Determining VCO requirements for 802.11a

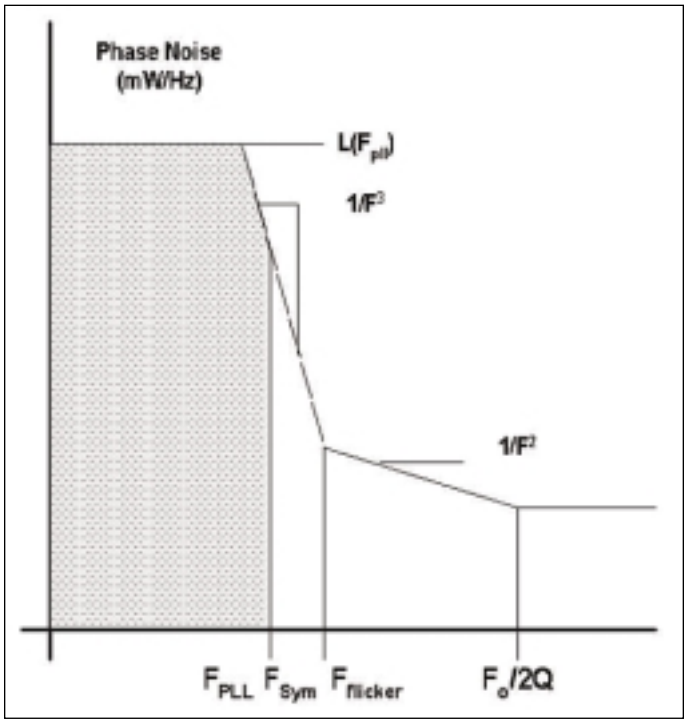
The three primary design specifications for this VCO are tuning range, phase noise and power consumption.

Tuning-range specification

For 802.11a applications, the tuning range must cover the entire 100 MHz for a given band. Ideally, the tuning range would be wideband enough to encompass all of the bands, so that the VCO can be programmed to operate in any of the three U-NII bands without component change. This allows a single VCO design to be used for all three bands, thereby reducing component inventory and yielding lower unit cost. Thus, a tuning range of at least 5.1 to 5.9 GHz is recommended.

Phase-noise specification

The OFDM specified by IEEE 802.11a places stringent requirements on the phase noise of the VCO because narrowband subcarriers are used. Phase noise is typically specified in terms of dBc per hertz at offsets of 10, 100 and 1 MHz. Because IEEE 802.11a specifies multiple data rates up to 54 Mbits per second, using BPSK, QPSK, 16-QAM and 64-QAM modulations, phase-noise requirements vary for each case. A simplified method to approximate the VCO phase noise requirements is as follows:



▲ **Figure 2. Frequency synthesizer phase noise curve.**

1. Identify the bit rate, modulation, and symbol rate.
2. Calculate maximum rms phase error per symbol allowed based on the maximum bit error rate (BER).
3. Calculate maximum phase-noise spectral density that when integrated over a symbol period is less than the maximum rms phase error.

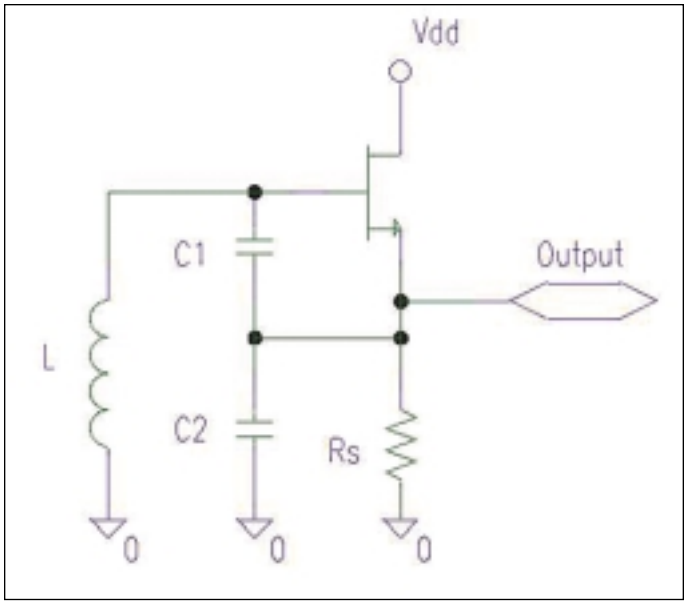
Table 2 summarizes the bit rate, symbol rate and modulation for 802.11a. The most phase-sensitive case for 802.11a is 54 Mbits per second with 64-QAM, which has a minimum constellation angle difference of 9.5 degrees. Because 802.11a utilizes interleaving and forward error correction, acceptable channel BER is 10^{-4}. For 64-QAM, the total required carrier to noise ratio (C/N) at 10^{-4} BER is 17 dB. Although calculating the precise degradation due to phase error requires rigorous mathematical derivation and statistical analysis, a worst case limit can be estimated by assuming both local oscillator (LO) phase error and channel noise have a Gaussian distribution and combine accordingly [5]. Because LO phase noise will act as an irreducible noise floor, C/N_{lo} must be >> 17 dB for 64-QAM. This means total integrated phase noise over one symbol should be less than at least 17 dBc for negligible impact on the BER.

Because the precise phase noise versus frequency envelope depends on numerous implementation specifics, such as phase-locked loop (PLL) response, frequency reference purity, we will assume the following:

- The PLL has a 10 kHz loop bandwidth.
- Close-in phase noise tracks the reference and is approximately constant up to the PLL bandwidth.
- Symbol bandwidth is 312.5 kHz. Single-sideband cutoff is 156.25 kHz.
- Worst-case cuffoff frequency of flicker noise is > symbol bandwidth and PLL bandwidth.

With these assumptions made, N_{lo} is found by integrating total VCO rms phase noise over one symbol bandwidth (Fsym) by calculating the total shaded area under the piece-wise linear curve in Figure 2.

For simplicity, let us assume the carrier is 1 mW and $L(f)$ is measured in terms of mW per hertz. We will solve for the phase noise density $L(f)$ at F_{pll} and then extrapolate to an offset of 100 kHz.



▲ **Figure 3. Simple Colpitts oscillator topology.**

$$N_{lo} = \int_0^{Fsym} L(f) \cdot df \tag{1}$$

where phase noise density $L(f)$ is fitted to:

$$\begin{aligned} L(f) &= L(F_{pll}) \quad 0 \le f \le F_{pll} \\ L(f) &= L(F_{pll}) \cdot \left(\frac{F_{pll}}{f}\right)^3 \quad F_{pll} \le f \le F_{sym} \end{aligned} \tag{2}$$

Inserting these equations into the integral for N_{lo} with F_{pll} = 10 kHz and F_{sym} = 156.25 kHz, we get:

$$\begin{aligned} N_{lo} &= \int_0^{F_{pll}} L(F_{pll})\, df + \int_{F_{pll}}^{F_{sym}} L(F_{pll}) \cdot \left(\frac{F_{pll}}{f}\right)^3 \cdot df \\ N_{lo} &= L(F_{pll}) \cdot F_{pll} \cdot \left(1 + 0.5\left(1 - \left(\frac{F_{pll}}{F_{sym}}\right)^2\right)\right) \\ N_{lo} &\cong 1.5 \cdot L(F_{pll}) \cdot F_{pll} \end{aligned} \tag{3}$$

This equation illustrates the significant effect that the PLL loop response can have on overall phase noise. Writing C/N_{lo} in terms of C_{ref} and N_{lo}, we achieve:

$$\left(\frac{C}{N}\right)_{lo} = \frac{C_{ref}}{N_{lo}} = \frac{C_{ref}}{1.5 \cdot L(F_{pll}) \cdot F_{pll}} \ge \left(\frac{C}{N}\right)_{min} \tag{4}$$

Rearranging terms and solving for $L(F_{pll})$ relative to the carrier, we achieve the following:

$$\begin{aligned} L(F_{pll}) &\le \frac{C_{ref}}{1.5 \cdot F_{pll} \cdot CN_{min}} \\ L(F_{pll})_{dBc} &\le C_{ref\,dBc} - CN_{dBc} - 10 \cdot \log(1.5 \cdot F_{pll}) \\ L(F_{pll})_{dBc} &\le 0_{dBm} - 17_{dB} - 41.7_{dB} = -58.7_{dBc} \end{aligned} \tag{5}$$

Extrapolating the phase noise density to 100 kHz, we achieve:

$$\begin{aligned} L(100\text{kHz})_{\text{dBc}} &\le L(F_{\text{pll}})_{\text{dBc}} - 30 \cdot \log\left(\frac{100\text{kHz}}{F_{\text{pll}}}\right) \\ L(100\text{kHz})_{\text{dBc}} &\le -88.7_{\text{dBc}} \end{aligned} \tag{6}$$

Power consumption specification

Since many 802.11a devices will be portable, power consumption must be minimized. This is achieved by using minimal supply current and bias voltage. In general, less than 10 mA bias current is possible. Minimum bias voltage is usually limited by the technology chosen to implement the oscillator. Operation as low as 1.0 volts is possible with power consumption at 10 mW.

Designing the VCO

Theoretical oscillator design

A Colpitts oscillator topology was selected for the VCO. The basic Colpitts oscillator is shown in Figure 3. Because the transistor amplifier used in a Colpitts topology is common source, excellent power supply noise rejection is also possible.

The first step in designing the VCO is to extract design equations for the oscillator using circuit analysis. Loop gain (A) at resonance is

$$A = gm \cdot Rs \cdot \frac{C_2}{C_1} \tag{7}$$

Loop gain must be greater than 1V/V or 0 dB at 180 degrees phase shift to ensure oscillation. Because Rs tends to reduce transistor bias current, which leads to lower transconductance g_m, the circuit designer needs to carefully select the C2/C1 ratio to achieve sufficient closed loop gain.

Oscillator frequency F_o is calculated using the following equation:

$$F_o = \frac{1}{2\pi\sqrt{LC_{eff}}} \tag{8}$$

Effective tuning capacitance C_{eff} at resonance is the series combination of C1 and C2:

$$C_{eff} = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1} \quad (9)$$

Several factors must be considered when selecting L and C_{eff}. Both L and C_{eff} have physical limitations when implemented in an integrated circuit. Inductors are typically implemented using a spiral pattern on a metal layer. Because the metal layers in an integrated circuit are only 10 to 20 um thick, the inductors typically have several ohms of resistance, which usually limits inductor Q to less than 20. In addition, inductor values are typically restricted to several nH's for circuits operating in the 6 GHz range due to self-resonance. Tuning capacitance range is limited by physical constraints of the varactor devices in the selected foundry process. Both inductor and varactor limitations must be evaluated carefully when selecting the final resonator component values.

The next specification to consider is the phase noise. Theoretical phase noise can be predicted using Leeson's phase noise equation in terms of dBc per hertz:

$$L(\Delta f) = 10\log\left[\frac{1}{2}\left(\left(\frac{Fo}{2Q\Delta f}\right)^2 + 1\right)\left(\frac{Fc}{\Delta f} + 1\right)\left(\frac{FkT}{Po}\right)\right] \quad (10)$$

where:

- F_o = Oscillator frequency
- Q = Loaded resonator quality
- Δf = Frequency offset with respect to the carrier
- F_c = Flicker noise cutoff frequency of the transistor amplifier
- F = Noise factor of the transistor amplifier
- k = Boltzmann's constant = 1.38×10^{-23}
- T = Temperature in Kelvin
- P_o = Oscillator output power

According to Leeson's noise equation, Q and P_o should be maximized and a transistor that has a low flicker noise cutoff and noise figure should be selected. In order to maximize Q, the following equation is derived for the Colpitts oscillator:

$$Q = \frac{\omega_o \cdot Rs \cdot (C_1 + C_2)}{\left(1 - \omega_o{}^2 \cdot C_1 \cdot L\right)} \quad (11)$$

From this equation, it is evident that Rs should be maximized to achieve the highest Q. It also appears that C1 should dominate C_{eff} in order to maximize Q. This would require, however, the tuning capacitance C2 to have little effect on C_{eff}, which would greatly limit tuning range. Optimization of Q for phase noise is best achieved using simulation.

Equation (11) is valid as long as loaded resonator Q is lower than the inductor Q; otherwise, resonator Q is approximately equal to the inductor Q.

Finally, to achieve low power operation, the transistor amplifier must be biased so that adequate loop gain is achieved throughout the specified supply voltage range. Because a Colpitts oscillator utilizes a transistor amplifier in a voltage follower configuration, the drain-source voltage can be reduced significantly while still sustaining oscillation.

Circuit design and simulation

Process selection

There are several excellent foundry processes, that can be used to integrate a VCO. Here, 0.6 um GaAs metal electrode semiconductor field effect transistor (MESFET) process by TriQuint Semiconductor was selected for the design. Circuit simulation was performed with Pspice using TOM3 transistor models for the MESFETS. Both depletion and enhancement mode FETs were available.

Transistor selection

The transistors were scaled and biased just large enough to achieve a transconductance gm, which yields adequate open loop gain. The gain transistor is implemented using a depletion mode MESFET with two interleaved gates, which were 50 um long.

Transistor biasing

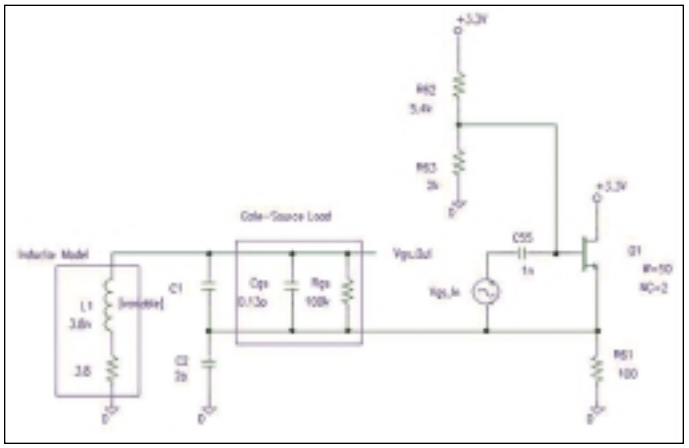
Nominal bias current was set to 8.2 mA. The gate is biased above ground to increase the dynamic range of the transistor amplifier and to allow a larger value for R_s to maximize resonator Q. DC simulation was used to fine-tune the gate voltage.

Open loop oscillator design

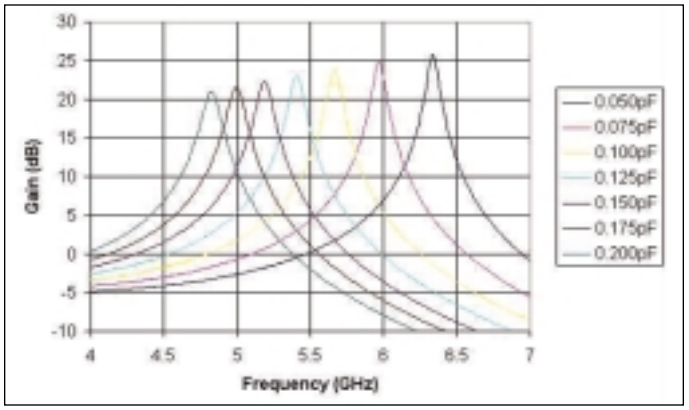
The next step is to simulate the open loop oscillator response. An important decision that must be made before simulation can be performed on the oscillator is where to break the loop. All circuit nodes should be loaded properly to achieve a representative open loop simulation.

We chose to break the loop at the gate-source junction of the amplifier. The input/output signal for the open loop analysis is a differential gate-source voltage, rather than a node voltage referenced to ground. The impedance across the gate-source junction for a Colpitt's oscillator is virtually unaffected by closed loop loading, even at resonance. Secondly, the gate-source impedance load presented to the oscillator feedback can be modeled using a simple RC parallel circuit, which is extracted at the nominal operating point of the transistor amplifier. Figure 4 illustrates the open loop simulation circuit.

The circuit was then simulated with Pspice using AC analysis. By plotting the open loop gain and phase ver-



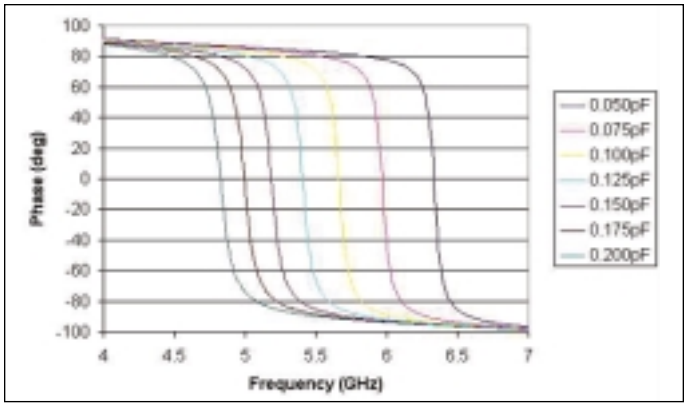
▲ **Figure 4. Open loop simulation circuit.**



▲ **Figure 5. Simulated open loop gain versus frequency plot showing tuning range and *Q*.**

sus frequency, the tuning range and resonator *Q* can be verified. Open loop gain is measured by plotting Vgs_Out/ Vgs_In versus frequency. Feedback capacitors C1 and C2 are adjusted along with L until adequate tuning range and resonator *Q* is achieved. Figure 5 shows the simulation results for the open loop gain and phase.

Figures 5 and 6 show that a capacitance range of 0.075 to 0.200 pF for C2 yields a tuning range of over 1



▲ **Figure 6. Open loop phase versus frequency plot.**

Frequency	Simulated *Q*	Phase Noise (100 kHz)
5.00 GHz	19.2	–101.0
5.18 GHz	20.7	–101.3
5.40 GHz	22.5	–102.2
5.66 GHz	23.6	–101.6
5.97 GHz	26.0	–101.7
6.33 GHz	28.8	–102.1

▲ **Table 3. Simulated *Q* and calculated phase noise.**

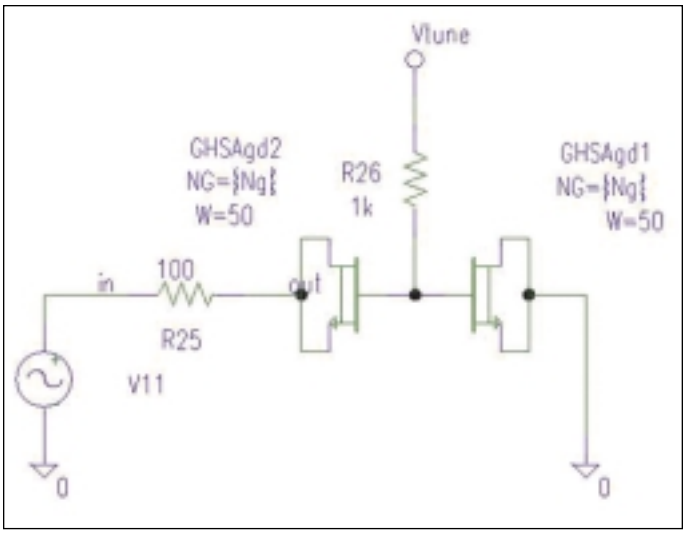
GHz. Resonator loaded *Q* can be determined from these simulation results by dividing resonant frequency by 3 dB bandwidth:

$$Q = \frac{Fc}{BW} \tag{12}$$

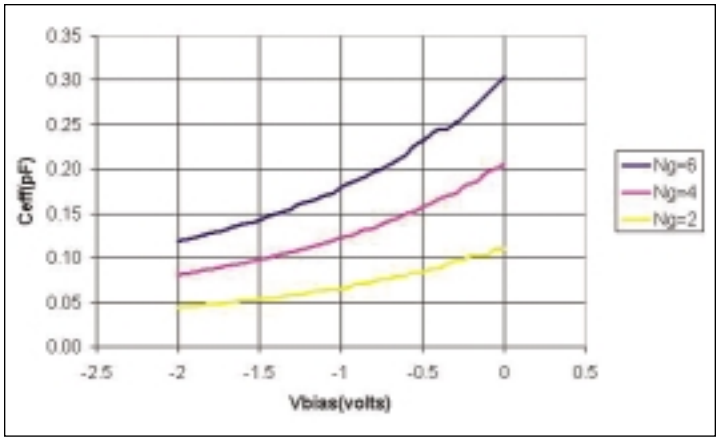
Table 3 shows simulated *Q* and calculated phase noise.

Tuning element design

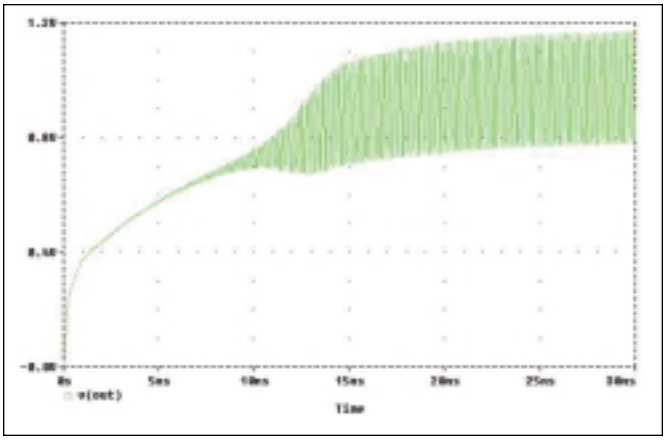
The next step is to design the variable capacitor C1. The tuning capacitor is implemented using a pair of MESFETs connected in series. The gate-source capacitance of the MESFETs provides a voltage-controlled variable capacitance. By connecting two MESFETs in series, in a back-to-back configuration, the net capacitance modulation due to Vgs signal swing across each gate-source junction is cancelled, thereby enabling greater dynamic range. Simulation is needed to determine the required size of the MESFETs. Simulated capacitance was calculated by measuring the 3 dB cutoff frequency versus transistor size and bias voltage using the circuit shown in Figure 7.



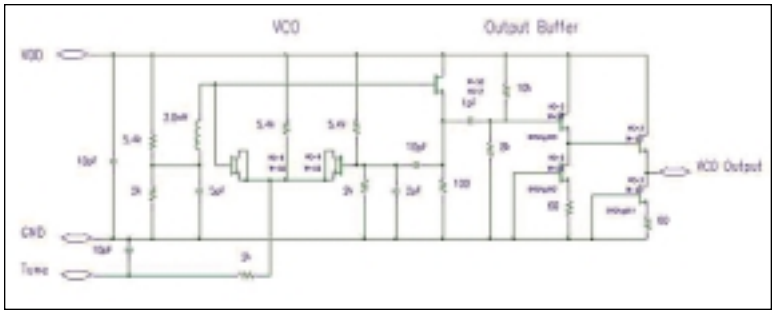
▲ **Figure 7. Simulation circuit for variable capacitance using MESFETs for tuning.**



▲ **Figure 8. Simulated capacitance curves for the back-to-back MESFET varactor.**



▲ **Figure 9. Simulated transient response for the closed loop oscillator during power-up.**



▲ **Figure 10. Complete VCO circuit.**

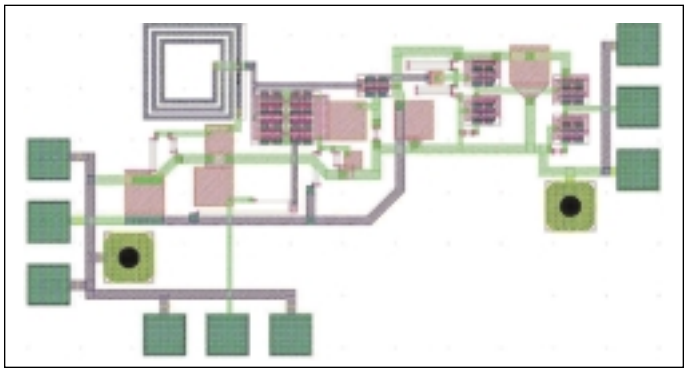
The curves in Figure 8 show that a 50 um × 6 interleaved gate MESFET will yield the required capacitance tuning range.

Inductor design

The inductor was designed using ADS by Agilient. Turns were added until 3.8 nH was achieved. DC resistance was extracted using 2-D EM simulation for oscillator simulation.

Output buffer design

Finally, an output buffer was added to isolate output loading from the oscillator. The output buffer is designed using a source follower circuit with g_m = 0.020 to achieve a 50-ohm output impedance.



▲ **Figure 11. Final VCO circuit layout.**

Final circuit simulation

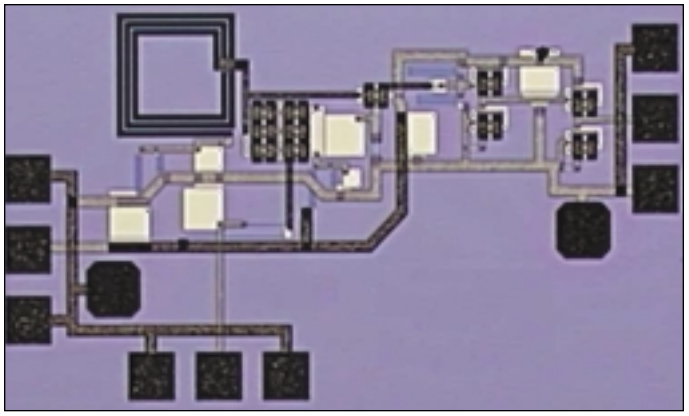
The remaining design task is to perform transient simulation of the oscillator over its entire tune range to verify start-up. Contrary to popular belief, oscillation starts because of the supply voltage step transient, rather than by noise that exists within the closed loop. Thus, to simulate oscillator start-up in a representative manner, the supply terminal was stepped from 0 to 3.3 volts.

Fabricating the VCO chip

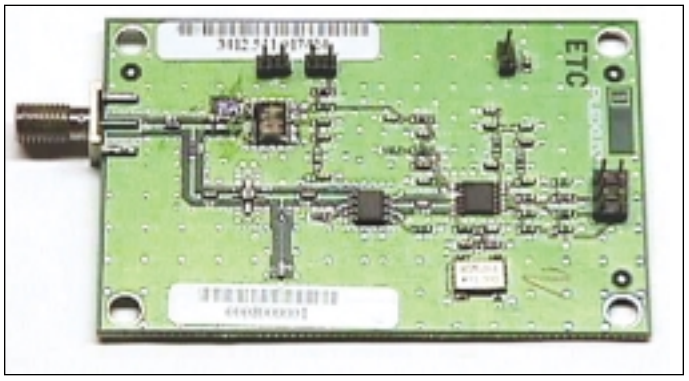
Numerous design tools can be used to perform the physical chip layout. Many tools can even perform 2-D planer EM simulation of the complete circuit, including layout effects such as interconnects and spiral inductors. This is particularly valuable for oscillator simulation, where parasitic capacitance of an interconnect may shift the entire tuning range. Another way to minimize the total development time required to complete an integrated VCO design is to include multiple versions on the same wafer. Several versions with slightly different inductor values should be included. In this way, any discrepancies between simulated inductance and parasitic capacitance are accommodated by at least one version. This design was implemented with inductor variations of nominal, ±10 percent, and ±20 percent on the prototype wafer. The final schematic is shown in Figure 10.

Chip layout

The VCO chip layout was performed with emphasis on minimizing parasitic inductance and capacitance of the resonator components. The layout plot in Figure 11 shows the compact placement of the varactor MESFETs and the inductor.

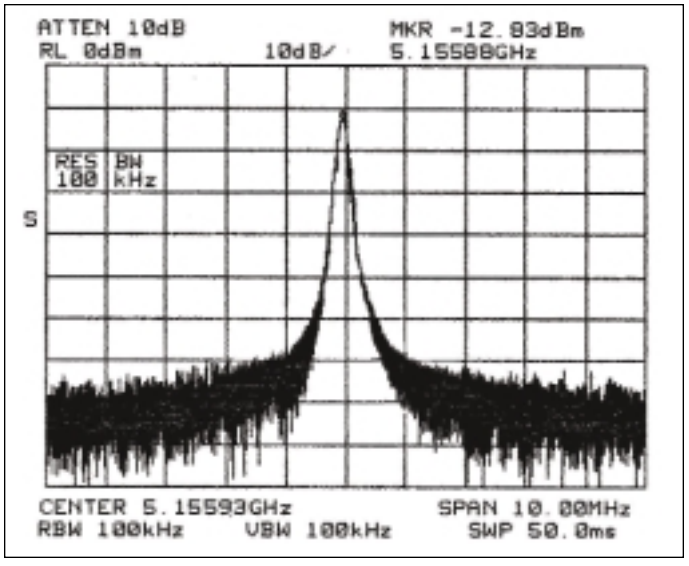


▲ **Figure 12. Photomicrograph of the die after fabrication.**

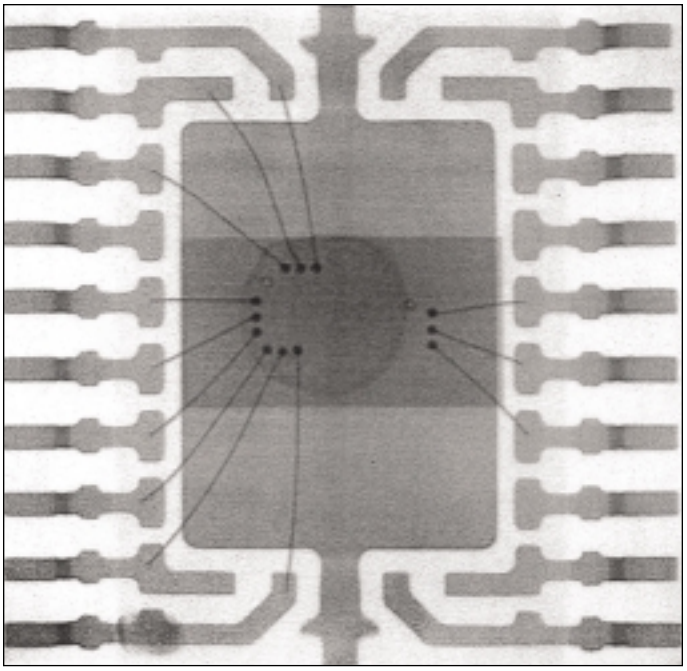


▲ **Figure 14. Test board.**

A photomicrograph was taken of the die after fabrication and is shown in Figure 12. The die was then packaged in a TSSOP-20 pin package for testing. An X-ray of the packaged IC showing wire-bond connections is shown in Figure 13.



▲ **Figure 15. Frequency spectrum of the free-running VCO measured using a spectrum analyzer.**



▲ **Figure 13. An X-ray of the packaged integrated circuit (IC) showing wire-bond connections.**

Test results

The packaged IC was assembled to an FR-4 printed circuit board for testing. A PLL was included on the test board so that the frequency could be locked for accurate phase noise measurement. A narrow bandwidth PLL loop filter was utilized so that the measured phase noise characteristics represent the VCO only. The test board is shown in Figure 14.

The plot in Figure 15 shows the frequency spectrum of the free running VCO measured using a spectrum analyzer.

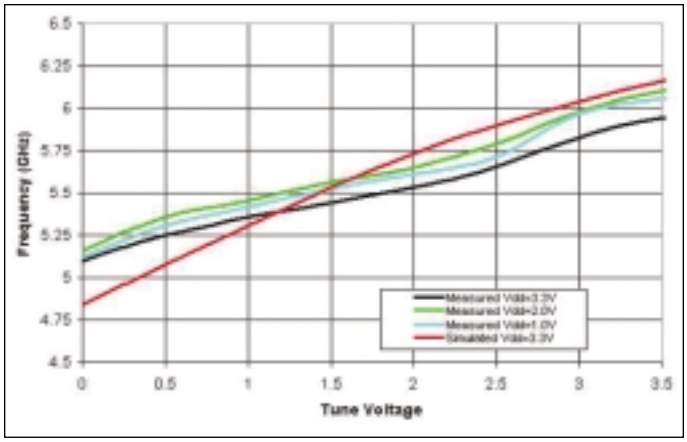
Phase noise measurements were taken by centering the spectrum analyzer on the carrier, then shifting the center to Fc+offset, and adjusting the resolution bandwidth to 1 Hz and span to 100Hz. The results are shown in Table 4.

Tuning range was measured versus supply voltage and is illustrated in Figure 16.

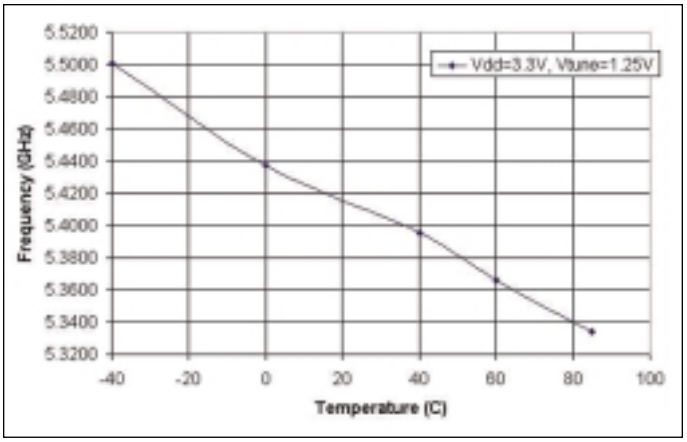
The VCO achieves 5.15 to 5.9 GHz tuning range for all supply voltages tested. The optimal circuit turned out to be the –20 percent inductor version. The full tuning range is maintained even down to Vdd=1.0 volt. Excellent operation over temperature was achieved as the VCO functions throughout the industrial tempera-

Frequency	Measured Phase Noise (dBc/hertz)	
	100 kHz offset	1 MHz offset
5.15	–89.5	–110.5
5.50	–90.0	–111.7
5.82	–89.2	–110.0

▲ **Table 4. Phase noise measurements.**



▲ **Figure 16. Oscillation frequency versus tune voltage.**



▲ **Figure 17. Measured frequency drift versus temperature.**

Parameter	Measured Value
Tuning Range	5.1 to 5.9 GHz for Vdd = 1.0 to 3.3 volts
Phase Noise	–89 dBc per hertz at 100 kHz offset –110 dBc per hertz at 1 MHz offset
Output Power	–12.8 dBm at Vdd = 3.3 volts
Frequency Pulling with Vdd	35 MHz per volt over 5.1 to 5.9 GHz
Frequency drift with temperature	2.5 MHz per degree Celsius (500 ppm) max over –40 to +85 degrees Celsius
Supply current at Vdd = 3.3 V	VCO: 8.5 mA Output buffer: 9.5 mA

▲ **Table 5. Complete list of measured VCO parameters.**

ture range of –40 to +85 degrees Celsius, as shown in Figure 17.

A complete list of measured VCO parameters is shown in Table 5.

Summary

An integrated VCO design is presented which meets the requirements for an 802.11a transceiver design, including tuning range and phase noise. Low power operation, low phase noise and wide tuning range were all achieved and demonstrated using a GaAs MESFET foundry process. Measured test results track theoretical simulations fairly well. First past design success was achieved by fabricating multiple prototype circuits at the same time with slightly different resonator component values. ■

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