

# A Hybrid Fractional-N Synthesizer for Direct Modulation Applications

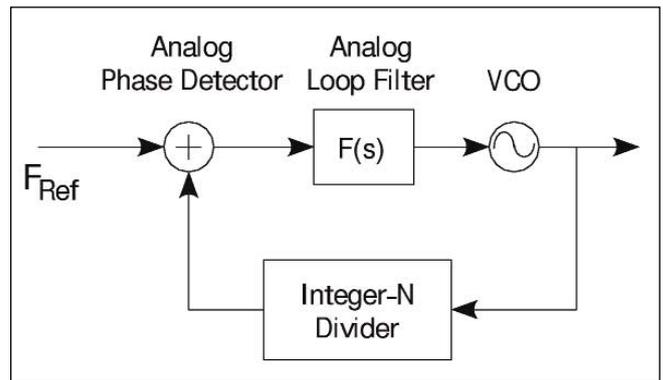
By Seste Dell'Aera and Tom Riley  
Kaben Research

The need for reduced component count and improved performance continually drives innovation in radio systems architectures. One of these innovations is a direct modulation architecture. Direct modulation is applicable to global system for mobile communications (GSM), Bluetooth™ and 802.11b, where the data is converted to frequency modulation (FM). Direct modulation in the transmitter portion of a system directly applies the data to the Delta-Sigma ( $\Delta\Sigma$ ) modulator portion of a  $\Delta\Sigma$  synthesizer.

Applying this modulation technique to high data rate systems has to date been difficult because the  $\Delta\Sigma$  synthesizer loop bandwidth remains narrow to reduce the quantization noise generated at high frequencies by the DS modulator. This narrow phase-locked loop (PLL) filter attenuates quantization noise but can cause intersymbol interference (ISI) because the data is also filtered. Therefore, in order to implement direct modulation architectures in higher data rate standards, the quantization noise must be reduced. To gain an appreciation on why the problem exists, this article will examine several types of synthesizers.

## Integer-N synthesizers

Figure 1 shows the block diagram of an integer-N synthesizer. This system is referred to as integer-N because it switches frequencies by integer multiples of the internal reference frequency ( $F_{REF}$ ). This  $F_{REF}$  is generated by dividing down a crystal oscillator using a reference divider located prior to the analog phase detector in Figure 1. In this system, the analog phase detector compares two inputs,  $F_{REF}$  and the

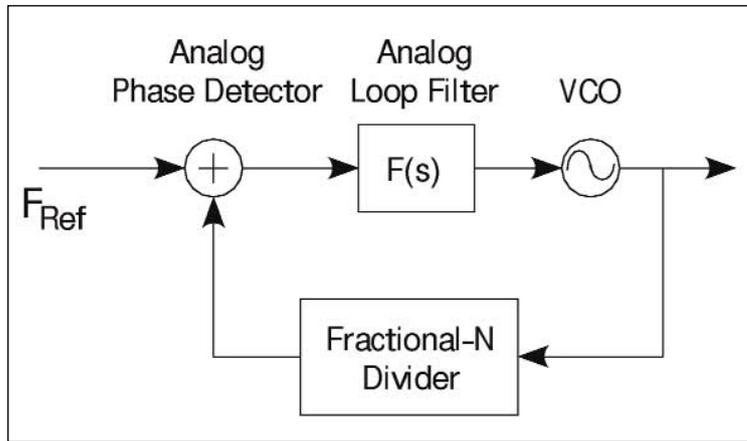


▲ Figure 1. Integer-N synthesizer.

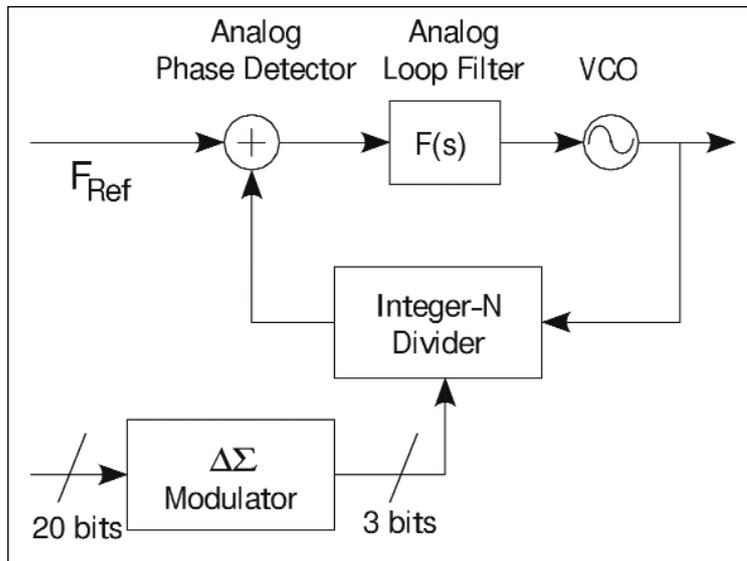
integer-N divider output, which is the divided-down voltage-controlled oscillator (VCO) output frequency. The phase detector adjusts the voltage to the VCO until both inputs are equal in phase or phase-locked.

To generate a desired VCO frequency, the integer-N divider divides the VCO frequency by a value (N). To generate an output frequency of 1000 MHz with a step size of 1 MHz,  $F_{REF}$  is 1 MHz ( $F_{REF}$  is equal to step size in an integer-N synthesizer) and N is 1,000. This system works well when the step size is relatively large. However, when a finer step size is required, the phase noise suffers.

The problem arises because the system amplifies the phase noise of the charge pump by  $20 \text{ Log } (N)$ .  $N = 1,000$  creates 60 dB of added phase noise. To achieve the finer step size, the reference divider must divide the crystal frequency by a larger number to obtain a lower  $F_{REF}$ . Thus, increasing the value of N to achieve finer step sizes results in an increase in the phase noise.



▲ **Figure 2. Fractional-N synthesizer.**



▲ **Figure 3. Delta-Sigma fractional-N synthesizer.**

The loop filter bandwidth must be much less than  $F_{REF}$ , and so the bandwidth must be narrower for fine step size applications. To complicate matters, another source of noise is the VCO. The loop filter attenuates the VCO noise at frequencies that are lower than the loop bandwidth. To keep the VCO noise down, we desire a high loop bandwidth.

### Fractional-N synthesizer

In fine-step size applications, a fractional-N synthesizer (see Figure 2) improves on the integer-N design by replacing the integer-N divider with a fractional-N divider. This fractional-N divider effectively divides the VCO by a non-integer  $N$ , typically fractions as high as  $1/16^{\text{th}}$ . The result is that this synthesizer can step by  $1/16^{\text{th}}$  of  $F_{REF}$ .

To achieve a step size of 1 MHz, we can keep  $F_{REF}$  at a higher frequency such as 16 MHz.  $N$  reduced by a fac-

tor of 16 and using  $20 \text{ Log}(N)$ , we see the phase noise is improved by 24 dB. Alternatively, if we maintain  $F_{REF}$  at 1 MHz, the step size is reduced to 62.5 kHz.

This improvement comes at the cost of introducing a spurious response generated by the fractional-N divider. RMS delay error and periodic behavior in the accumulator of the fractional-N divider cause these spurs. The spurs repeat throughout the entire spectrum every  $1/16^{\text{th}}$  of  $F_{REF}$ , which is also equal to the step size.

The loop filter attenuates these spurs, which restricts the loop bandwidth to reduce the spurs to an acceptable level. The result compared to integer-N is a wider loop bandwidth and an improvement in phase noise but at the cost of introducing unwanted spurs.

### Delta-Sigma fractional-N synthesizer

A  $\Delta\Sigma$  fractional-N synthesizer (see Figure 3) offers a different approach for achieving a finer step size than a fractional-N. A multibit  $\Delta\Sigma$  modulator signal is fed into the integer-N divider. The input to the  $\Delta\Sigma$  modulator is the desired fractional division ratio, and the output is a bit stream that has an average value that is equal to the input. In effect, this signal from the  $\Delta\Sigma$  modulator tells the integer-N divider to divide by a given integer and sometimes by other integer values resulting in an average division ratio that has a fractional component.

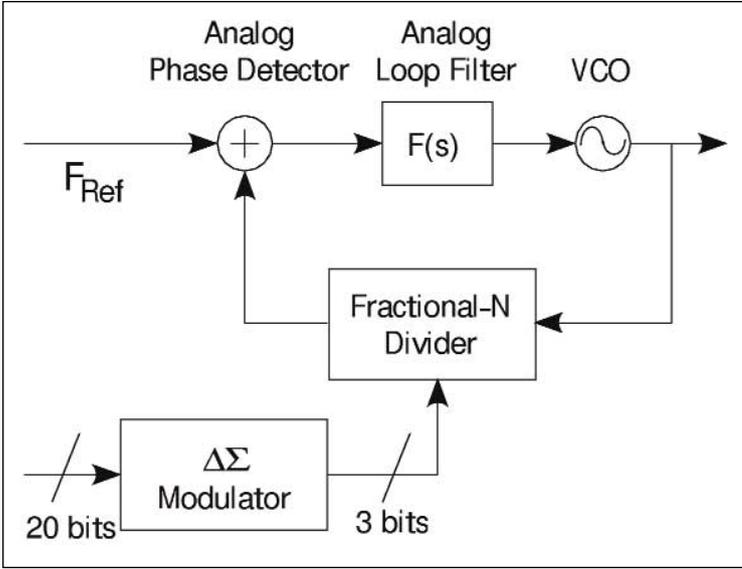
Fractionality in a  $\Delta\Sigma$  synthesizer can be 20 bits or higher. For example, using a 20-bit  $\Delta\Sigma$  modulator now improves the step size to  $F_{REF}$  divided by  $2^{20}$ . If  $F_{REF}$  were 16 MHz, then the step size would be 15 hertz. This is a huge improvement over the integer-N and fractional-N methods, and the step size can be made increasingly finer by simply adding additional bits to the  $\Delta\Sigma$  modulator. An additional benefit is that because  $F_{REF}$  remains very high, the value of  $N$  remains small, so the phase noise contribution remains as low as the original integer-N synthesizer.

As in the fractional-N example, this improvement in phase noise and step size does not come without some form of compromise. The  $\Delta\Sigma$  modulator, due to its noise shaping, introduces what is called quantization noise that occurs mostly at  $F_{REF}/2$ . The power spectral noise density contribution by a  $\Delta\Sigma$  modulator can be approximated by Equation (1), which shows the  $\Delta\Sigma$  modulator quantization noise:

$$S_b(f) = \frac{\Delta^2}{12 F_{REF}} \left[ \left( 1 - z^{-1} \right)^{O_{\Delta\Sigma}} \right]^2 \quad (1)$$

where  $z = e^{j2\pi f / F_{REF}}$

where  $\Delta$  is the quantization step size of the  $\Delta\Sigma$  modula-



▲ **Figure 4. Hybrid synthesizer.**

tor and  $O_{\Delta\Sigma}$  is the order of the  $\Delta\Sigma$  modulator. The resulting phase noise is shown in Equation (2), which shows the phase error resulting from quantization noise:

$$S_{\phi}(f) = \frac{\Delta^2}{12 F_{REF}} \left[ \left( 1 - z^{-1} \right)^{O_{\Delta\Sigma-1}} \right]^2 \quad (2)$$

This equation indicates the level of the phase error is controlled by  $\Delta$ . For an integer-N divider, the quantization step size is 1 VCO cycle, which means that  $\Delta = 2\pi$  radians. Therefore, decreasing the  $\Delta$  leads to reduction in the phase error.

Equation (2) also indicates that higher order  $\Delta\Sigma$  modulators reduce the low frequency phase error at the expense of increased phase error at  $F_{REF}/2$ . Conveniently, the loop bandwidth filters noise at  $F_{REF}/2$ , and no additional loop filter components are required for lower order modulators. In this method, the loop bandwidth needs to remain narrow to filter the phase error resulting from the quantization noise.

The  $\Delta\Sigma$  fractional-N synthesizer offers an additional

advantage at the system level in that the  $\Delta\Sigma$  modulator is ideal for direct modulation techniques. This technique removes an entire upconversion stage in the transmitter. However, in filtering the quantization noise, the relatively narrow loop bandwidth restricts direct modulation to low data rates due to ISI. Higher order modulators permit the use of larger loop bandwidths and higher data rates. This, however, requires additional filtering at  $F_{REF}/2$  (see Equation (2)). These additional components raise the cost and level of complexity in keeping the loop stable over process and temperature variations. This complexity often prevents the use of higher order  $\Delta\Sigma$  modulators.

One way to improve on the  $\Delta\Sigma$  synthesizer is to reduce the quantization noise. This allows the use of higher order  $\Delta\Sigma$  modulators to increase the loop bandwidth without additional filtering. Then data rate may be increased when using direct modulation.

### Hybrid synthesizer

Improvement in the  $\Delta\Sigma$  synthesizer may be achieved by combining fractional-N and  $\Delta\Sigma$  fractional-N techniques to create a hybrid synthesizer, as shown in Figure 4. In the hybrid, we replace the integer-N divider in the  $\Delta\Sigma$  synthesizer with the fractional-N divider from the fractional-N synthesizer, with additional techniques to glue it together.

The main advantage of the hybrid compared to  $\Delta\Sigma$  synthesizers is that the quantization step size of the  $\Delta\Sigma$  modulator is reduced to a fraction of a VCO cycle. For example, if we use a 16-phase fractional-N divider providing steps of 1/16th of a VCO cycle, then the quantization step size  $\Delta$  in Equation (2) is reduced from  $\Delta = 2\pi$  radians to  $\Delta = \pi/8$  radians. This lowers the quantization noise at all frequencies by 20 log (16) or 24 dB.

Because of the lower quantization noise at  $F_{REF}/2$ , we can now use a higher order  $\Delta\Sigma$  modulator and a higher loop bandwidth. Direct modulation is also possible at significantly higher data rates.

As previously mentioned, using a fractional-N divider produces spurs at the synthesizer output. This problem

must be solved for this method to be applied successfully. It turns out that instead of a periodic accumulator in the fractional-N divider, we have a pseudo-random  $\Delta\Sigma$  modulator. This causes the RMS delay error to spread spectrally over the bandwidth of  $F_{REF}$ , thus converting the spurs to pseudo-random noise rather than a series of tones. The expected improvement in the whitening of the delay error is  $10 \log (F_{REF})$ . For example, when using  $F_{REF} = 16$  MHz, spurs at  $-50$  dBc are reduced to  $-122$  dBc per hertz. This noise is insignificant compared to other noise sources in the synthesizer.

## Conclusion

This article has shown that the hybrid  $\Delta\Sigma$  synthesizer offers an improvement in overall phase noise and loop bandwidth over its predecessors when fine step size is required. This is achieved by using a standard PLL loop filter that requires no additional external components. The synthesizer also supports direct modulation transmitter architectures for high data rate applications, significantly reducing the cost of future radio designs. ■

## Acknowledgement

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## Author Information

Seste Dell'Aera is vice president of sales and marketing with Kaben Research. He has more than 18 years of experience in technical sales and marketing. Over the last six years, he helped to build early stage startup companies and held executive positions for Philsar Semiconductor and OEone Corporation. He can be reached via E-mail: [seste.dellaera@kabenresearch.com](mailto:seste.dellaera@kabenresearch.com); or Tel: 613-826-6649.

Tom Riley is CEO and a founder of Kaben Research. He has more than 16 years of experience in academia and industry in mixed-signal integrated circuit (IC) design. He is an internationally recognized expert in the area of  $\Delta\Sigma$  fractional-N frequency synthesis and has published 14 papers in the IC area. He also holds patents in the area of mixed-signal radio frequency design.