Wireless Antenna Interface

The demand for consumer wireless products poses design challenges with respect to cost, performance, packaging and semiconductor technology. The author provides practical guidelines, illustrating them with an antenna interface integrated circuit.

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The growing market for wireless communication products has spawned a large demand for carrier-frequency integrated RX/TX circuit functions. Many of the communications products using these RFICs require low power consumption, small size and single-polarity power supply operation. In addition, some applications require low intermodulation distortion. All applications require low cost.

With the appropriate selection of semiconductor device and packaging technologies, it is now practical to meet these design and cost goals by using integrated circuits. In this article a radio frequency integrated circuit (RFIC) is described which combines the power amplifier, LNA and T/R switch functions for a cordless telephone application. It is an antenna interface ASIC (for application specific integrated circuit).

This antenna interface ASIC was developed using a conventional GaAs MESFET technology which had been developed specifically for commercial RFIC applications. This application requires lower power and less linearity than typical cellular applications, thus FET technology is practical for single-polarity supply operation. Plastic surface-mount packaging technology is used for lowest production cost.

Design Trade-offs

Developing RFIC chipsets for the growing wireless communications market involves more cost aggressive engineering trade-offs than have customarily been encountered for other MMIC applications. These include:

1. *Package type and pin count:* For low cost production at frequencies below 3 GHz, narrowbody SOIC (small outline integrated circuit) packaging is the preferred style. The PLCC (Plastic Leadless Chip Carrier) is much less desirable due to the package thickness dimension, which is 3 times that of an SOIC. The largest available pin count for narrowbody SOIC is 16, and this includes pins allocated for low inductance RF grounding. Higher pin count widebody SOIC packages are available, but for economically-sized dice, say 50 mils square, the wirebond lead lengths required to wire the die in the larger package result in excessive parasitics, especially lead inductances. For IFIC products, which need only handle frequencies of 100 MHz or less, the widebody SOIC packages are practical.

PLCC packages have similar die-size versus package size trade-offs to be considered. In addition, PLCC packaging costs are generally higher than for SOIC packages. SSOP packages, which use 25 mil lead pitch, rather than the 50 mil pitch used by SOIC and PLCC, are being used with more frequency. The finer lead pitch allows a smaller footprint for a given pin count, and the body is vertically thinner than the 50 mil package styles. However, leadframe parasitics are higher and thermal conductivity is lower with the SSOP package than with the 50 mil pitch packages.

Depending upon the number of input/output (I/O) ports required in the RF function, along with the number of RF ground pins required for acceptable circuit performance, there may not be many pins left for off-chip connections. At some point, MCM (Multi-Chip Module) techniques may enable some passive circuit elements to be included within the same package as the active die, but this is not generally cost-effective now.

Some specific circuit functions, such as power amplifiers, require extremely low inductance ground connections and thermal conduction paths which may not be practical to achieve using plastic packaging. Such functions require considerably more attention in the area of package design than do lower signal level circuit functions, but the cost constraints are still present.

Examples of low-cost customized packages for power amplifiers include fused leadframe SOICs, embedded heat spreaders, and single-layer ceramic chip carriers. Fused leadframes are usually effective up to the point at which the magnitude of the inductive voltage developed across the RF ground path becomes comparable to the input signal magnitude. For a 900 MHz power amplifier with a Class AB output stage, the fused leadframe is practical up to approximately one watt of output power. A plastic package using an embedded heat spreader, which also serves as an extremely low inductance ground path, is an effective solution for higher power and higher frequency applications. Single-layer ceramic packages with ground vias to the backside are another cost-effective packaging solution for higher power or higher frequency products. Both alumina and aluminum nitride chip carrier technologies are becoming more affordable. The general rule to be observed in developing custom packages for wireless applications is: "The more the package physically resembles an existing SMD (Surface Mount Device) package, the more likely it is to be a commercial success."

2. *Semiconductor technology used*: Passive elements with acceptable performance may be fabricated on GaAs substrates, but require substantial amounts of die area. For example, a 600 micron gate MESFET uses approximately 18,000 square microns of die area. A 20pf MIM capacitor, which is the size required for low-VSWR DC blocking at the 50 ohm level at 900 MHz, uses 69,000 square microns. Depending upon the circuit topology, several such DC blocks may be necessary. It is easy to see how die size can grow rapidly with the number of passive elements. At 900 MHz, it is usually a good trade-off to put DC blocks and RF bypasses off-chip, whenever possible.

With high-performance silicon processes, passive elements are also practical in the 800 MHz to 3 GHz range. The high-performance silicon processes tend to approach that of GaAs in cost, however, so the same caution about area applies. On the other hand, with moderate-performance, lower-cost silicon processes, the substrate parasitics associated with passive elements can be substantial. In this case, circuit performance, rather than die cost, influences how many monolithic passive elements are included within the die.

3. *Cost versus performance trade-off for passive elements:* This particular trade-off must be made throughout an RFIC design cycle, whenever a passive element is used in the circuit topology. As noted, there is a significant cost penalty incurred, in the form of die area required, whenever a monolithic passive element is used in a design. This cost penalty must be weighed against

the circuit performance degradation penalty which will occur if the passive element is placed off-chip. In the 900 MHz band and below, this trade-off usually favors off-chip passives. Above 3 GHz, full-monolithic solutions usually are favored. The 1.9 GHz PCS and 2.5 GHz ISM bands are in an intermediate gray area from a design trade-off standpoint.

4. *How many power supply voltages?:* The answer is usually "one," and this complicates some circuit designs, particularly power amplifiers, if GaAs MESFET is the desired technology. With some performance trade-offs, single voltage supply circuits are realizable. The value of the supply voltage is also an important consideration in the selection of the design approach used. It not only influences the semiconductor technology choice, but the circuit topology choices, as well.

5. *Powerdown or standby operation*: Portable wireless applications, and some fixed applications, require a powerdown feature whereby the entire circuit function, or parts of it, have the DC bias turned off to conserve the battery charge when the circuit is not in use. Powerdown is usually straightforward to implement with most circuit functions. With power amplifiers, particularly if GaAs MESFET technology is used with a single power supply, the powerdown function presents some particular design challenges. This factor may influence the choice of semiconductor technology used in the RFIC design.

6. *What circuit functions are to be included?:* Depending upon how the overall circuit requirements are partitioned, certain semiconductor technologies are favored. Beyond the obvious partitioning of frequency range, i.e., RF versus. IF, some circuit functions may also dictate which technology is most appropriate for the application. For example, GaAs MESFET, or perhaps silicon MOSFET technology provides the most compact RF switch functions. If the circuit partitioning includes T/R or antenna diversity switches, then FET technology of some form is probably the most desirable choice.

7. *Impedance matching techniques*: As noted, monolithic passive elements may increase the die size significantly. If the impedance matching topologies commonly used with hybrid or discrete circuits are applied to a monolithic circuit, the die cost may escalate unacceptably. Significant die area conservation may be achieved by using passive feedback or active circuitry to implement the impedance matching. Lossy RC feedback methods may be practical for many wireless applications which may tolerate the resulting degradation in output power and noise figure. Cordless telephones, wireless LANs and wireless security systems are examples of applications for which RC feedback circuits may be applied for impedance matching.

8. *The tolerance for parts count*: Assuming he could procure the parts at a reasonable price, most radio manufacturers would prefer a one-chip solution, to be used with a minimum number of off-chip components, perhaps one or two RF bypass capacitors on the power supply line. This may not be practical at an acceptable cost, and a cooperative design effort is most appropriate between supplier and user.

Antenna Interface Design

RF Micro Devices recently undertook the development of a custom RF chipset for a cordless telephone, to be operated in the 902-928 MHz ISM band, using digital modulation. Single power supply operation and a powerdown feature were ancillary requirements. Since the final product is intended for a low cost consumer application, total product cost was of paramount importance. A moderate-performance silicon bipolar technology for the RX downconverter and TX upconverter functions, and a GaAs MESFET technology for the antenna interface ASIC were considered to be optimum. The antenna interface ASIC, which is the subject of this paper, consists of a low noise amplifier (LNA), a 100mW power amplifier (PA), and a transmit/receive (T/R) switch. Narrowbody SOIC-16 packaging was selected for use in both RFIC products.

A block diagram of the antenna interface ASIC is shown in Fig. 1. The LNA develops 24 dB of gain in two stages and the three-stage power amplifier has a large-signal gain of 32 dB. The supply voltage used is +5.0 volts.

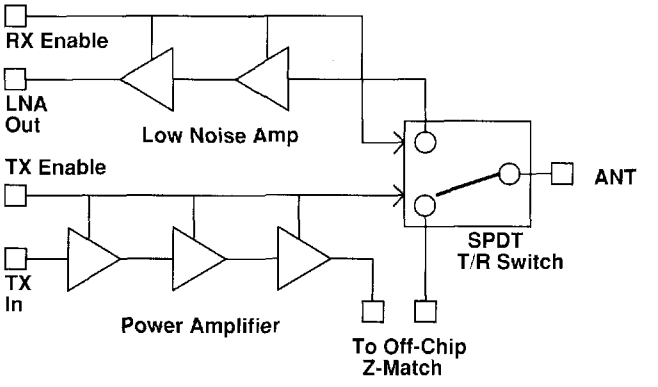

Fig. 1. Antenna Interface ASIC Block Diagram

In selecting a GaAs MESFET vendor for the antenna interface ASIC, several of the customer's requirements had to be taken into consideration. Since the RFIC design required powerdown capability from a single positive supply voltage, the process to be used needed an enhancement-mode FET (EFET) device. In addition, a low-cost process was required. The process selected uses planar MESFET structures with a 0.6 micron gate length and two-level front metal. Multiple depletion-mode (DFET) MESFET implants and one EFET implant are available. Also important, the process does not use either air bridges or via holes, resulting in better yield, and accordingly, lower cost..

The same basic circuit topology is used in both LNA stages and in the predriver and driver stages of the PA. As shown in Fig. 2, this gain block consists of a common-source EFET with resistive feedback and a DFET source-follower on the output. The EFET derives its gate bias from the feedback network, so in order to achieve powerdown, another EFET is used as a DC switch in series with the V_{DD} line for the gain block. The feedback provides the input impedance match to the gain block, and the source-follower matches the EFET drain to the load. The source-follower makes the gain block relatively insensitive to load impedance, so it is possible to use 7.5 pf interstage blocking capacitors, thereby saving considerable chip area over what a 20 pf DC block would require. The LNA output DC block and the PA input DC block are both off-chip, to save more die area.

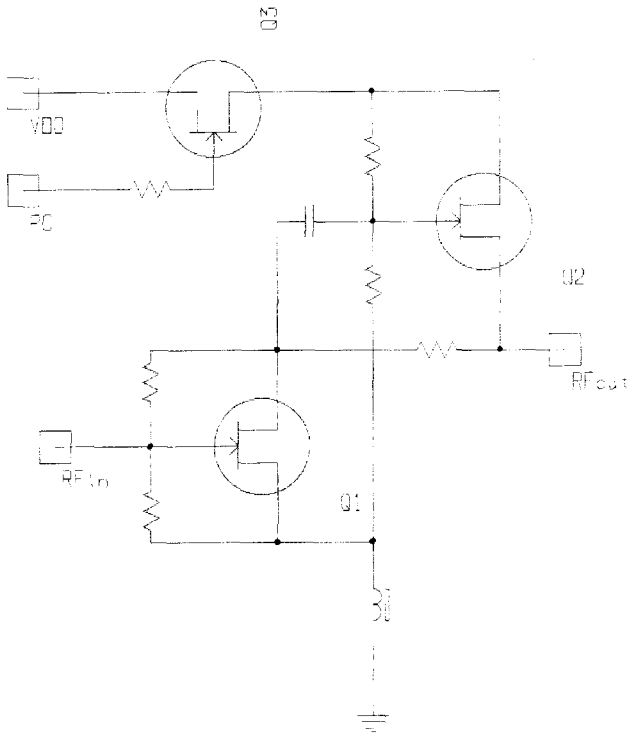

Figure 2. LNA/PA Driver Gain Block.

The PA final stage, shown in Fig. 3, consists of a common-source DFET using self-biasing. The powerdown feature is achieved using an EFET DC switch in the source circuit of the DFET. The EFET gate is connected to the TX-enable control line. The channel "on" resistance of the EFET is absorbed into the self-bias resistance network of the DFET. Because the current density capability of the EFET is lower than that of the DFET, the EFET switch uses over twice the gate width of the DFET in order to handle the current required in the final stage. The final stage also contains an RC feedback network to improve out-of-band stability. The output matching network is entirely off-chip in order to both save die area and minimize dissipative losses in the matching elements. The RF bypassing for the source self-bias resistor is off-chip.

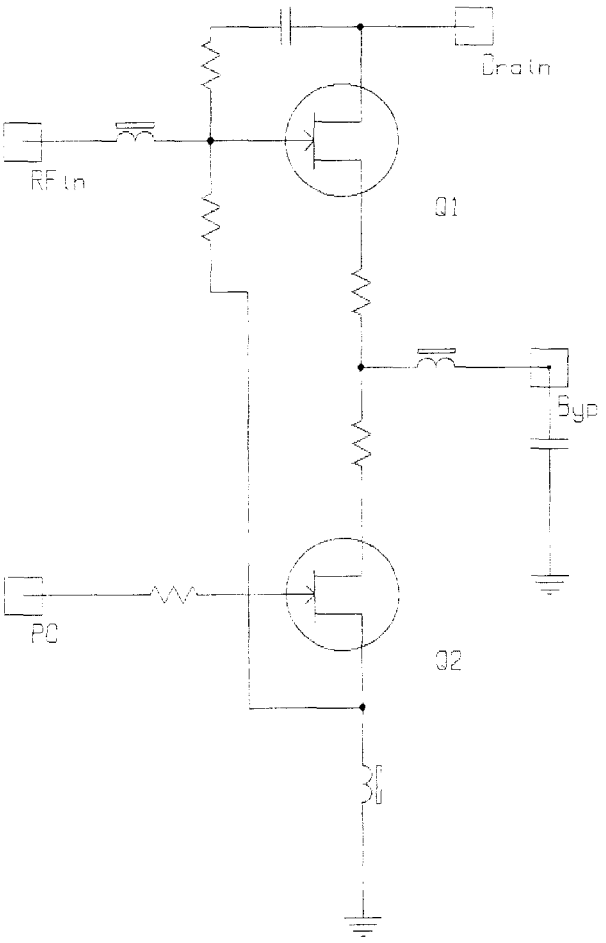

Figure 3. PA Final Stage.

The T/R switch consists of a pair of series DFETs, one in the TX leg, and one in the RX leg. Because the isolation specifications for the T/R switch are not particularly stringent, shunt DFETs were not required in the circuit. This saved die area and eliminated the requirement for another set of low-inductance ground pins on the package. The switch FET gates are tied to the TX-

enable and RX-enable control lines, respectively. The requirement for a negative bias source for the switch is eliminated by biasing the switch FET sources and drains at V_{DD} potential. This does require the use of DC blocks on the RF lines, however. The TX and antenna (ANT) line DC blocks are off-chip, and the RX line DC block is a monolithic 20 pf metal film-insulator-metal film (MIM) capacitor.

The entire antenna interface ASIC design fits on a die which is approximately 60 mils square. Every pin on the package is allocated, either to RF signal, control signal, or DC/RF ground. Although it would have been desirable to have all the RF signal and ground nodes assigned to the shortest package pins, the die layout does not permit such an arrangement. All grounds are on short pins, but several RF signal lines had to use corner pins, which have higher parasitic values than the short pins. Wherever possible, the extra lead and wirebond inductances have been absorbed into the RF circuitry associated with that lead.

Measured Performance

Modeled and measured performance of the PA circuit is shown in Figs. 4-9. Fig. 4 shows the measured IRL and large-signal gain of the PA portion of the RFIC from 715 MHz to 1.115 GHz. The input power is -13 dBm, single tone, and the bias voltage is 5.0 volts. The modeled IRL is shown in Fig. 5 under the same operating conditions, and does agree reasonably well with the measured IRL data, except the slope is backwards. The discrepancy is probably due to parasitics on the test board which were not properly modeled initially. Fig. 6 shows the modeled output power for the PA. This agrees fairly well with the measured large-signal gain from Fig. 4.

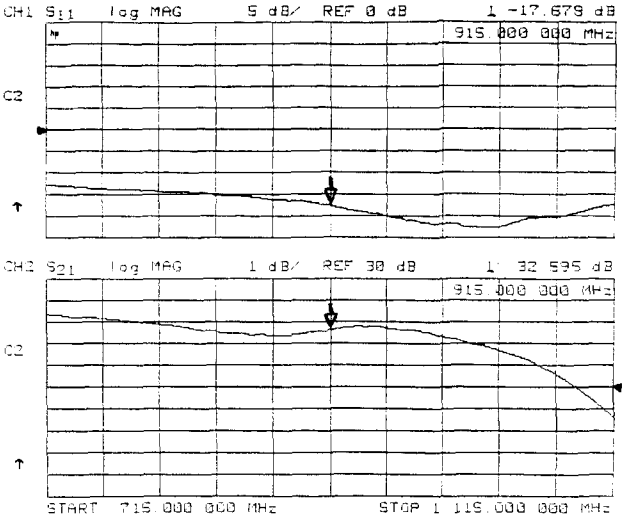

Figure 4. Measured IRL and Large-Signal Gain.

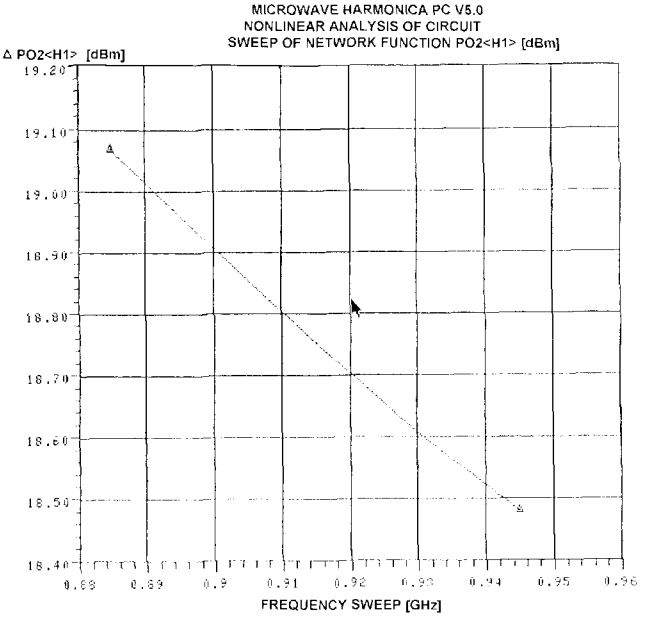

Figure 5. Simulated PA IRL.

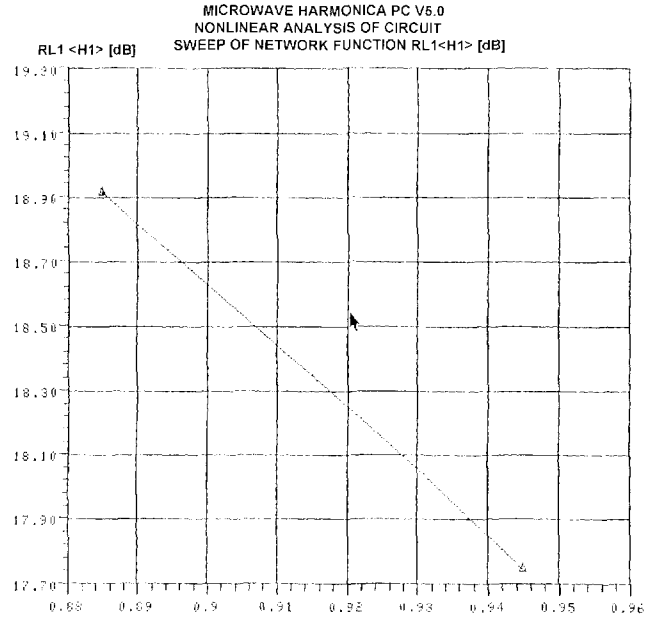

Figure 6. Simulated PA Pout.

The modeled third-order intermodulation distortion is shown in Fig. 7. The two-tone input power for this simulation is -16 dBm. The resulting two-tone output power from this simulation is +17 dBm, and the IMD is approximately -19 dBc. Fig. 8 shows the measured two-tone output spectrum resulting from a two-tone drive level of -19 dBm, and the resulting IMD is -20.6 dBc. A direct comparison of simulated-to-measured two-tone output power versus drive power is shown in Fig. 9, and simulated-to-measured IMD is shown in Fig. 10. The simulated performance, particularly in the case of IMD, becomes overly optimistic at high drive levels. This is most likely due to the inability of the TOM MESFET

model to model the device behavior accurately under these conditions.

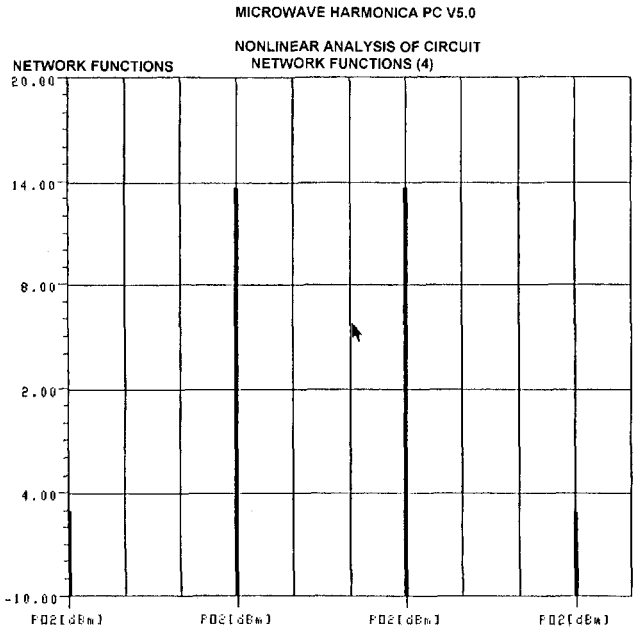

Figure 7. Simulated IM3, Pin = -16 dBm Two-Tone Avg.

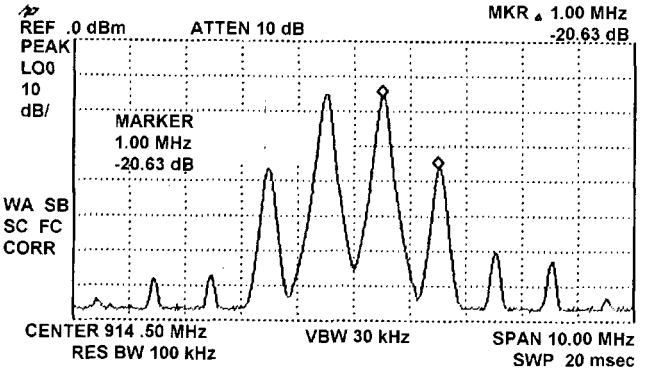

Figure 8. Measured IM3, Pin = -19 dBm Two-Tone Avg.

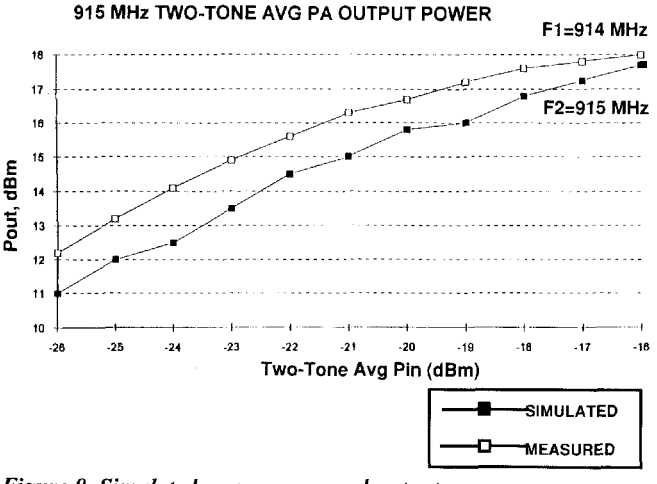

Figure 9. Simulated versus measured output power.

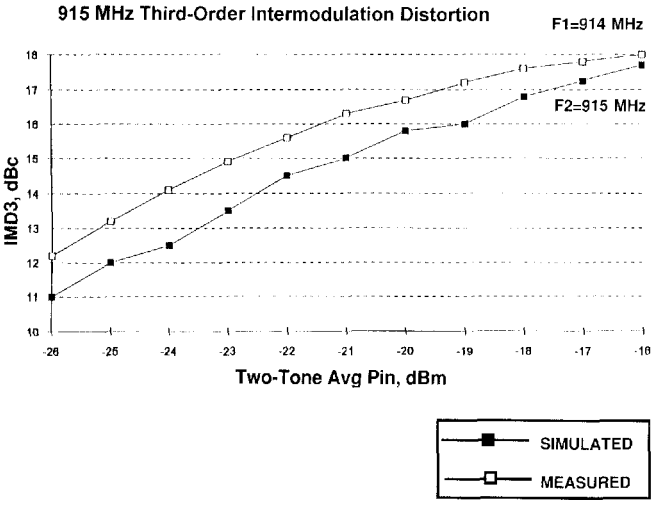

Figure 10. Simulated versus. Measured Third-Order IMD.

The specification for the PA is -25 dBc IM3. This circuit falls short in this regard. The operating condition which results in acceptable IM3 performance, shown in Fig. 11, is a two-tone input power of -21 dBm.

The performance shortfall in the PA is caused by the driver stage having lower drain bias current than had been modeled. This situation was caused by the fact that some of the EFET model parameters used in the initial design were incorrect.

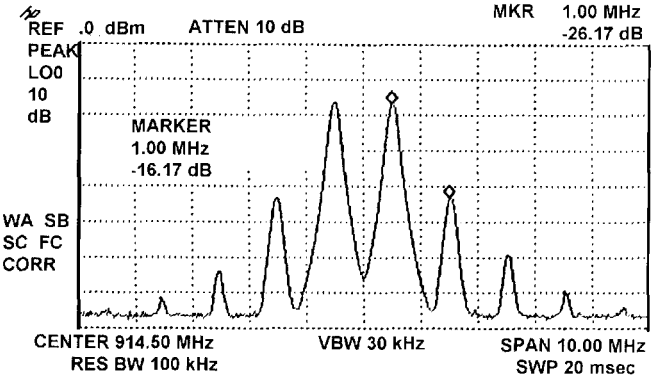

Figure 11. Measured IM3, Pin = -21 dBm Two-Tone Avg.

Although the data is not shown here, the LNA has a NF of approximately 3.0 dB at the LNA input, and the T/R switch "on" loss is 0.8 dB. The T/R switch isolation, from the TX port to the RX port, with the switch set to the TX-ANT position and ANT terminated, is approximately 18 dB at +20 dBm input power at the TX port.

Acknowledgments

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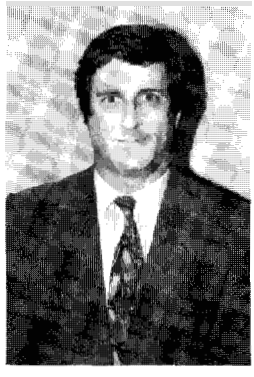

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