Compressed Video I-Q Demodulator

Compressed video systems use digital processing to reduce the transmission bandwidths of video signals for more channels in a given bandwidth. RF circuitry must handle digital frequency spectra without impacting system performance.

Eric Bausback
California Eastern Laboratories
Santa Clara, California

In compressed video systems, data compression reduces the bandwidth required for the digitized video signal by eliminating data in whose absence no visible difference would be discernible in the picture's reproduction. Specifically, when color and motion within the picture's pixels do not change from one frame to another, the corresponding data is eliminated from the transmission stream. Furthermore, color information above 1.3 MHz can be eliminated routinely with no apparent change in picture quality.

Accordingly, pictures are resolved into two sets of information, one representing still image and the other moving image components of the picture. After transmission of the still data, only updates containing moving information need be sent.

A block diagram for a compressed video system downlink receiver is shown in Figure 1. The satellite signal is received, amplified and downconverted to UHF. This UHF signal contains vector-modulated picture information (I-Q video data). The value of the I and Q components determine the chromaticity and luminance of the image using the color-difference relationships shown in Equation 1.

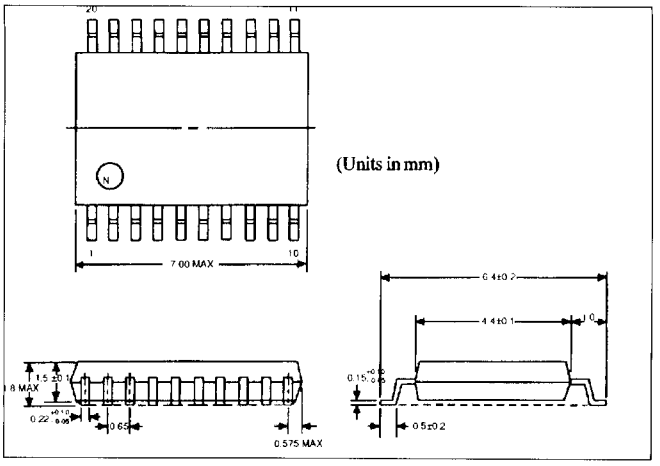

Figure 3. Dimensions of the 20-pin package.

The most important electrical characteristics of the I-Q demodulator are listed in Table 1.

I-Q Amplitude Balance: ±2 dB
I-Q Phase Balance: ±1.0°
IM3: -30 dBc @ -20 dBm input power, 2-tone
IF Bandwidth (-.25 dB): 50 MHz into 250 ohms, 2pF
Baseband Output Voltage: 1.5 V_{pp}
Input Frequency Range: 100 MHz to 1 GHz
Conversion Gain: 20 dB
AGC Range: 30 dB
LO-RF Suppression: 20 dBc
External LO Drive Level: -10 dBm

Table 1. Characteristics of the I-Q demodulator.

The circuit was designed using our firm's bipolar integrated circuit process with an f_T of 20 GHz. All electrical design work was performed using the SPICE™ simulator.

General Circuit Concepts

The use of differential cascode stages[1] throughout the circuit allowed the RF Bandwidth to be met comfortably without the customary use of peaking capacitance (Figure 4). This is desirable, because use of such capacitance has been known to cause inflections in the frequency response over process and temperature variations. This would have adversely affected the gain flatness. The value of RE1 is chosen for the best combination of noise figure and IM3 performance based upon the stage's location in the chain. RC1 is then chosen based upon the gain desired from the stage:

(2) $A_V = 2RC1 / RE1$

The mixers used are the Gilbert Cell type[2], which have good LO rejection at the output when the local oscillator (LO) signal is well balanced at the mixer's LO port.

In order to satisfy the gain flatness specification, the RF Preamplifier and RF automatic gain control (AGC) amplifier were designed to have a very flat gain response through the entire RF band.

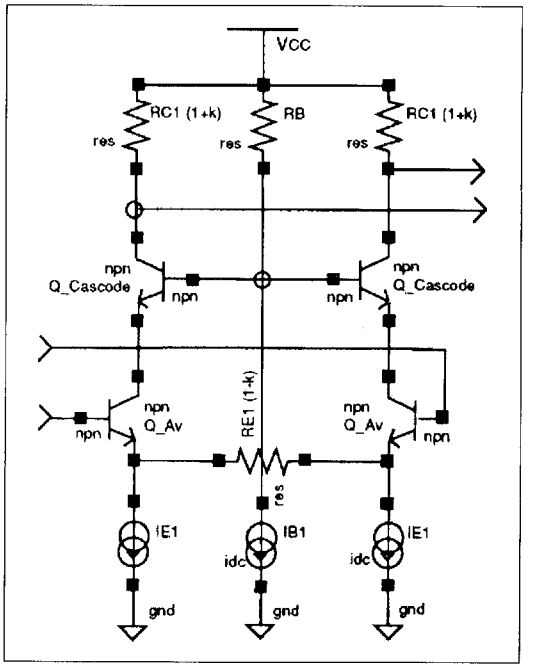

Figure 4. Cascode differential amplifier stage.

I-Q Amplitude Balance

Amplitude imbalance would be caused primarily by load and emitter degeneration resistance mismatches from channel to channel. An estimation of the contribution of each pair of mismatched stages to the overall I-Q amplitude imbalance is given by Equation 3.

(3) $dB[\,|I|/|Q|\,] = 40 * Log_{10}[(1+k)/(1-k)] = 1.74\ dB$

where the factor k = 0.05 is the mismatch factor between the I and Q channel elements for a 5 percent variation in resistance. Hence, it is desirable to minimize the number of stages in the I and Q channels. In this case, only one amplification stage is used following the mixers, so the worst case maximum I-Q gain imbalance will be ± 1.74 dB.

If the required AGC function were placed in the I and Q channels, not only would gain mismatches occur but also gain tracking problems as a function of AGC level. The latter effect would be caused by transistor mismatches. Therefore, a high frequency AGC stage was developed for inclusion in the RF path.

Output Voltage Swing Capability

The output amplifier must establish a 1.5 V_{pp} swing across a 250 ohm load, corresponding to a 3 milliampere current swing. To accomplish this efficiently, a differential push-pull stage was developed. Basically, this stage may be biased at less than half of the current required for a Class A output stage, such as an emitter follower. A schematic representation of this stage is shown in Figure 4, from which it is seen that the bias current IE2 required is 3 mA. Actually a 4 mA current was used to avoid full clipping and to allow for some head room. The gain of this stage is approximately 2*RC1/RE1, and the output voltage swing is determined as 2*IE1*RC1. Although not shown, additional transistors (normally OFF) were added to shunt Q1 and Q2. When turned on these allow for external amplitude trimming via an externally applied bias.

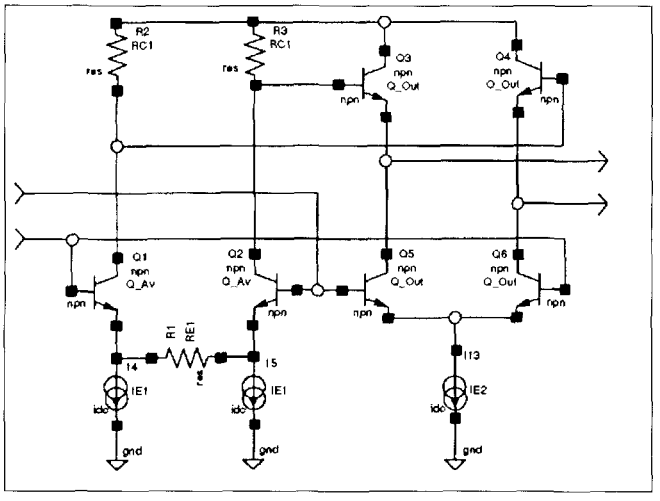

Figure 5. Output amplifier (differential push-pull).

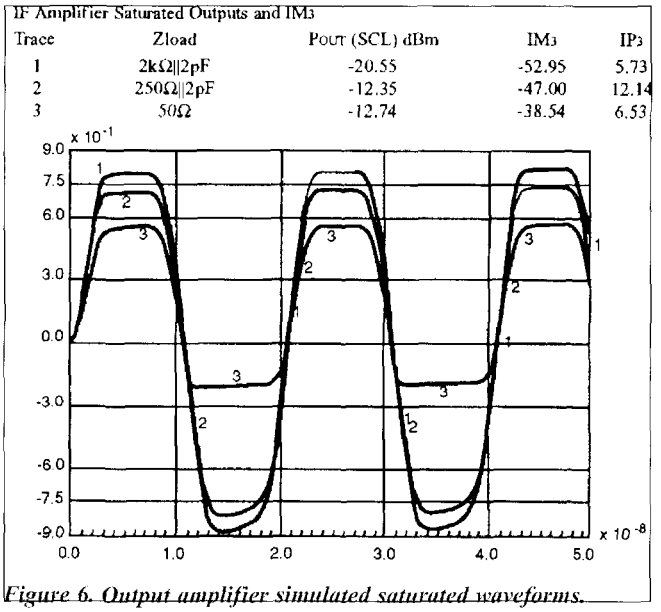

Figure 6. Output amplifier simulated saturated waveforms.

Phase Balance

Phase imbalances are caused mostly by the phase shifter. Any error in the phase shifter phase translates directly to I-Q phase error. An external RC type phase shifter such as shown in Figure 7 was incorporated into an application circuit test fixture. This type of phase shifter offers very good phase characteristics but poor amplitude balancing. To reduce the latter effects, LO buffer-amplifiers were incorporated into the design such that the I and Q channel mixers would operate in the modulator mode over a range of LO input power from approximately -10 to +5 dBm. The RC network is centered at 460 MHz.

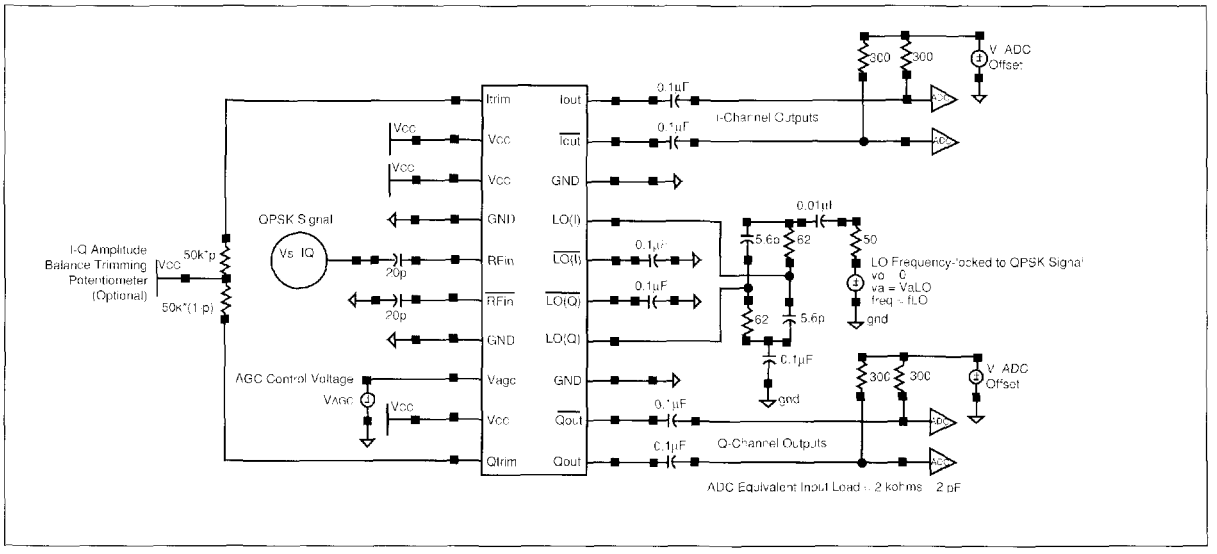

Figure 7. Application circuit with external RC phase shifter.

System simulations were conducted to determine important performance characteristics. These are shown in Figures 8 through 12.

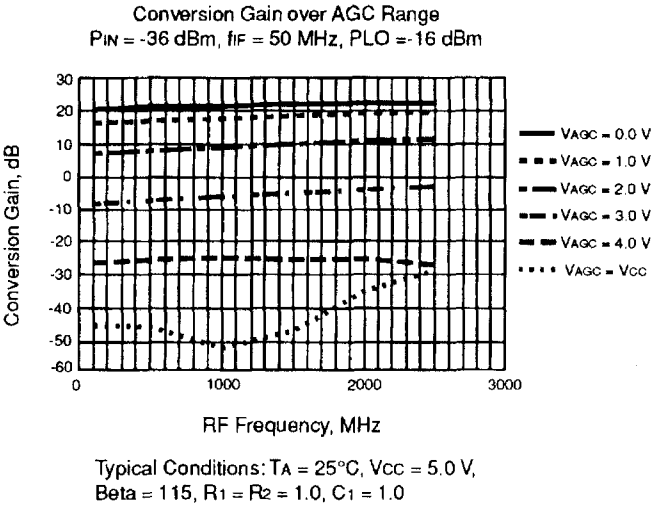

Figure 8. Conversion gain characteristic.

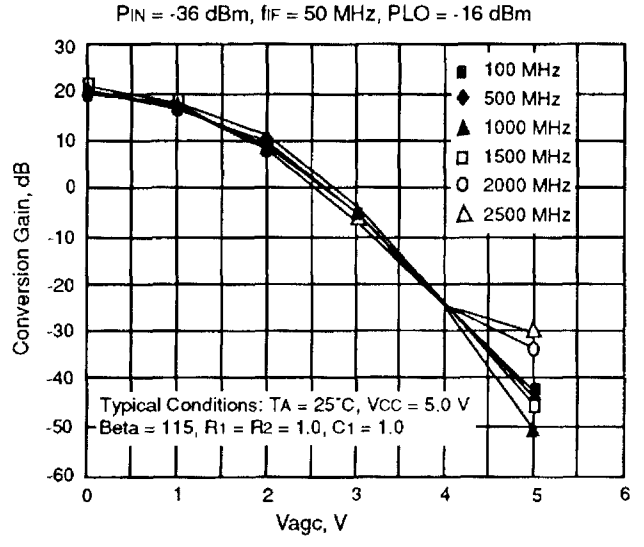

Figure 9. AGC control characteristics.

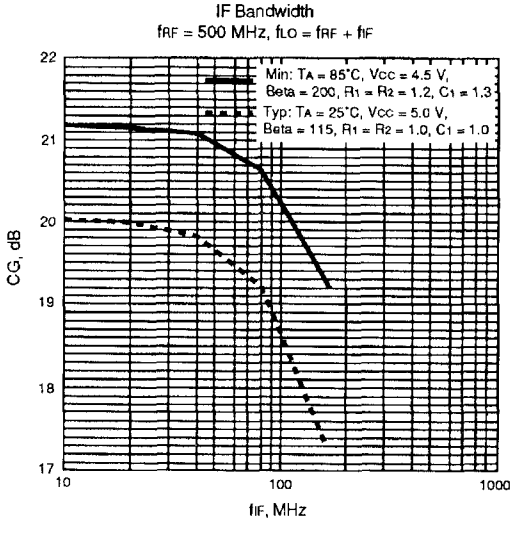

Figure 10. IF bandwidth characteristic (Z_L=250 ohms and 2pF).

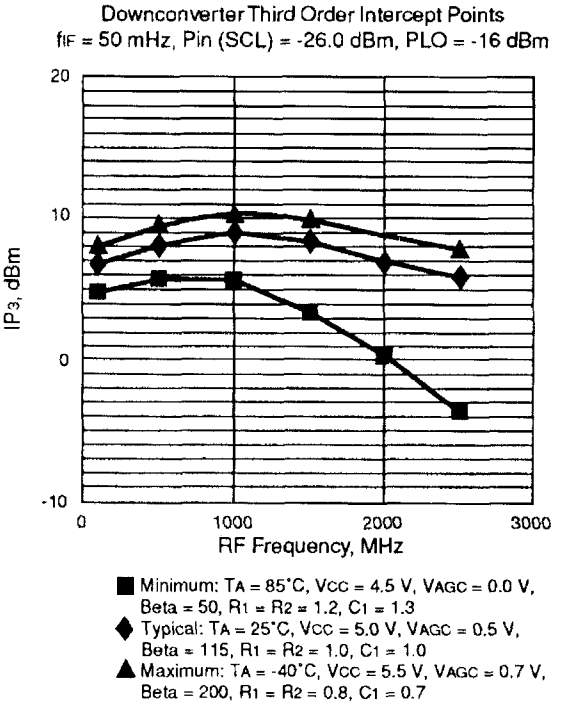

Figure 11. Third order intercept points.

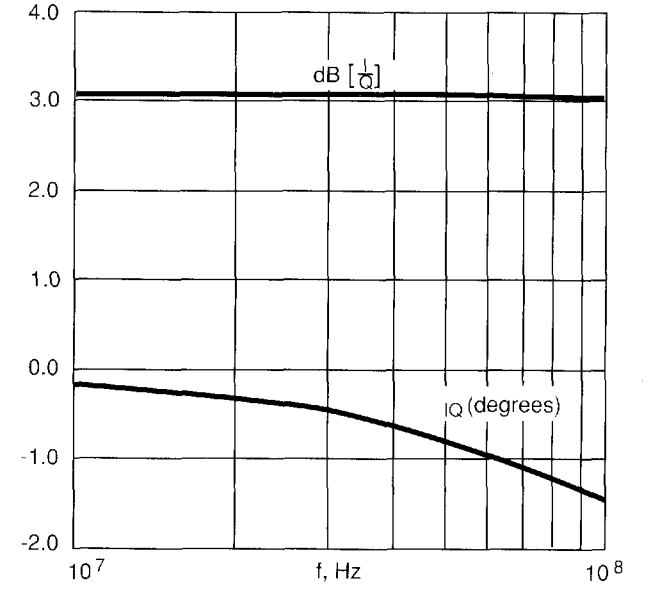

Figure 12. Worst case simulated I-Q balance over swept IF.

Characterization

The test set of Figure 13 is used to characterize the I-Q Demodulator for conversion gain, AGC characteristics, and phase and amplitude balance. Phase and amplitude balance is characterized by normalizing the Q channel output to the I channel output.

Test Data

First samples of the device were fabricated and tested

using the circuit described in Figure 13. Results are shown in Figures 14 to 16. Results using the application circuit of Figure 7 are given in Figures 17 through 19. Although not shown, the single-ended saturated output voltage was measured to be 1.2 V_{pp} at an IF frequency of 40 MHz.

These results demonstrate the design viability of an I-Q demodulator for compressed video applications realized with silicon bipolar process integrated circuitry. The resulting device has characteristics that should render it useful for other digital applications as well.

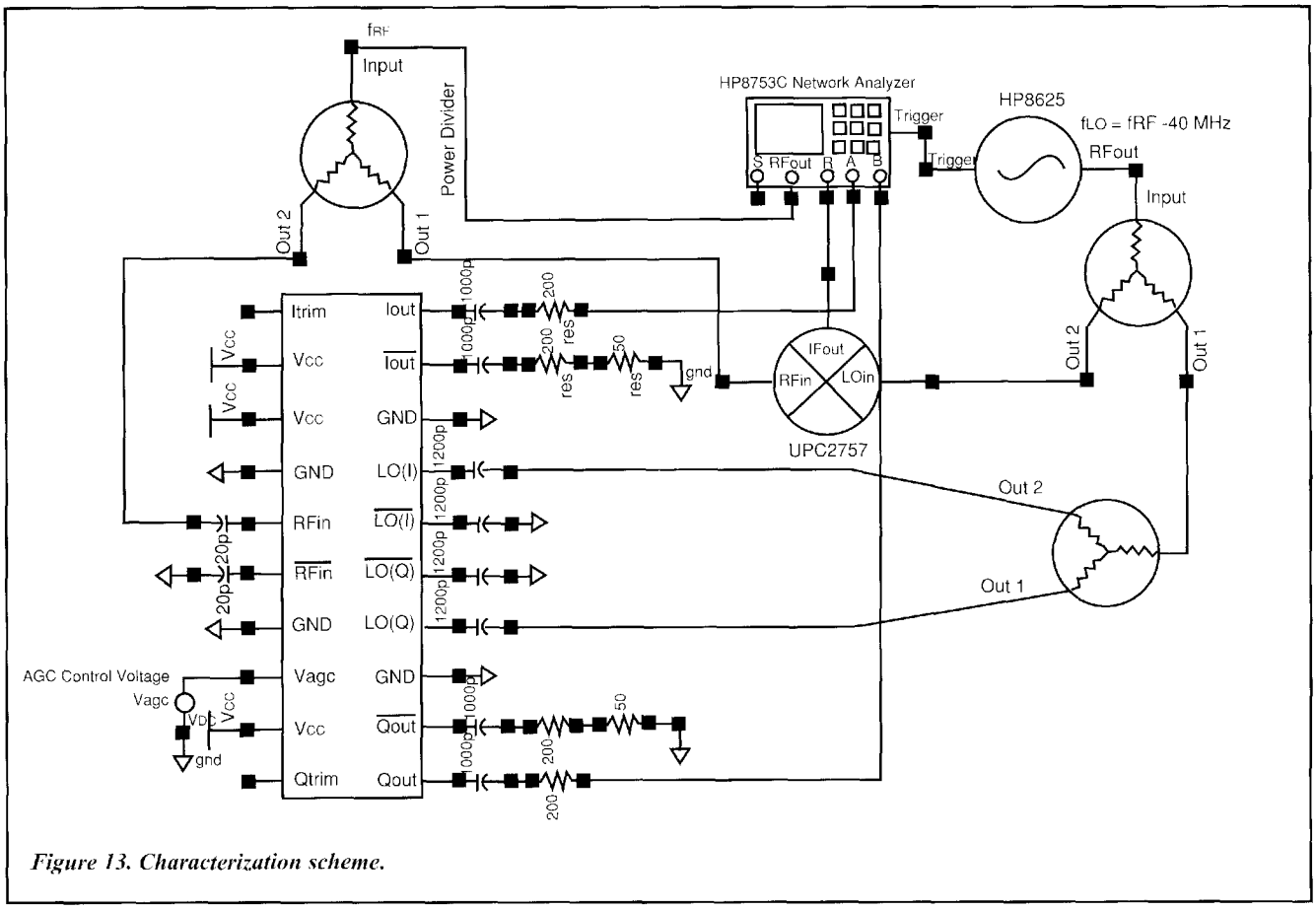

Figure 13. Characterization scheme.

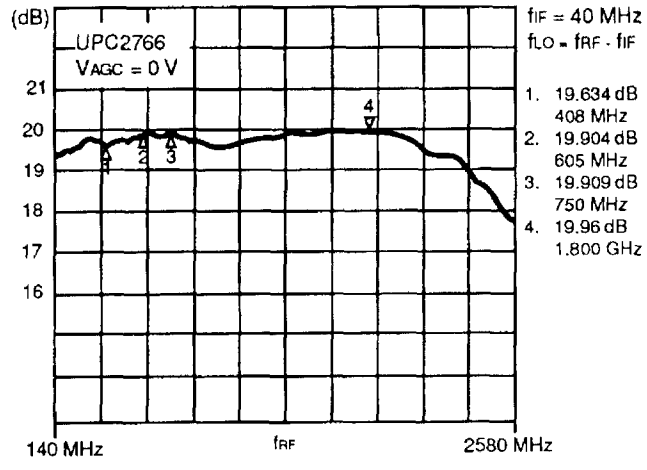

Figure 14. Wideband conversion gain

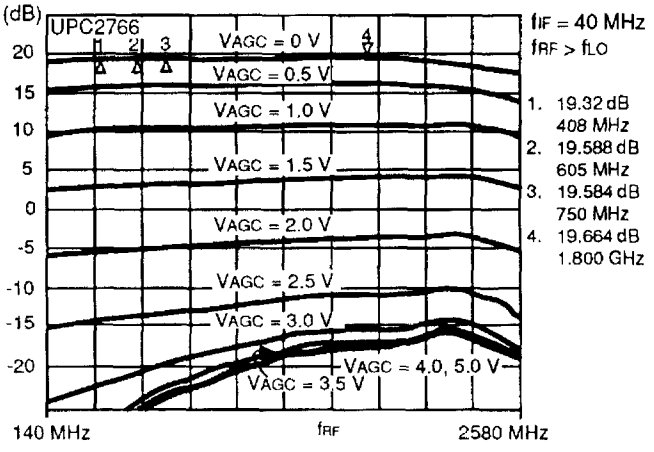

Figure 15. AGC characteristics.

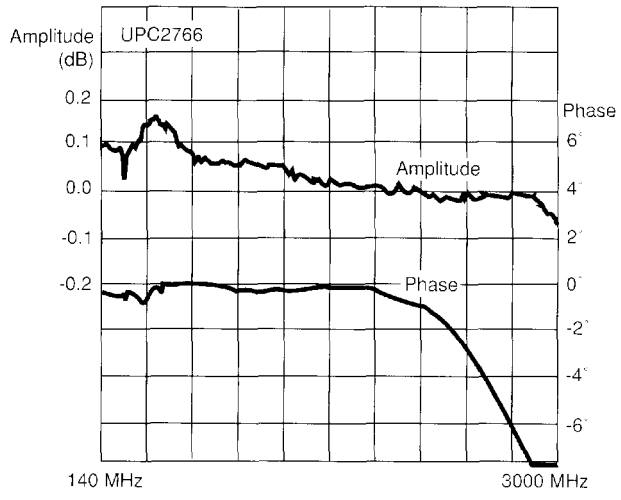

Figure 16. I-Q amplitude and phase balance.

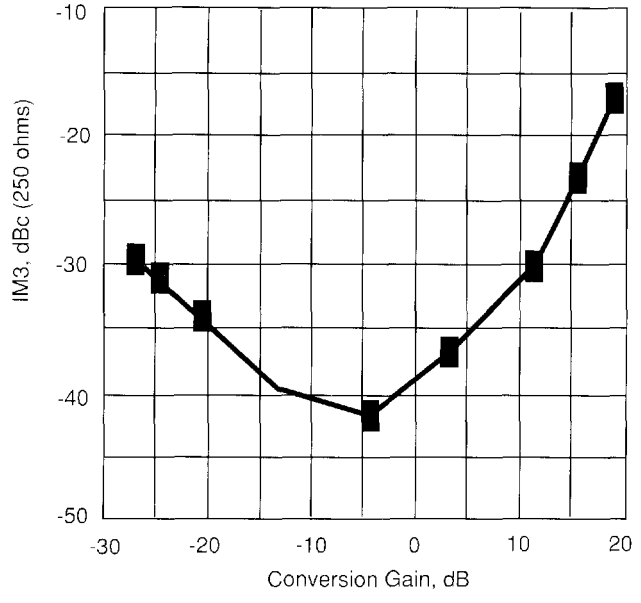

Figure 17. Intermodulation distortion.

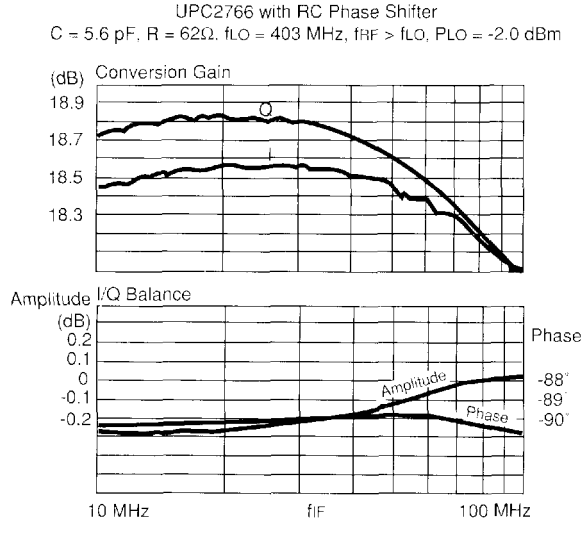

Figure 18. Performance at f_{LO} = 403 Mhz.

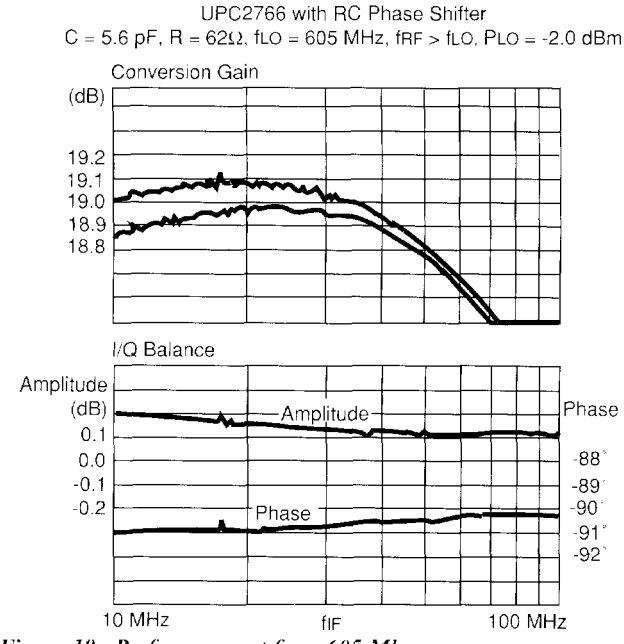

Figure 19. Performance at f_{LO} = 605 Mhz.

Acknowledgments

The author gratefully acknowledges the cooperation and assistance provided by the staff and support groups of NEC's Compound Semiconductor Device Division's Microwave Device Department in the circuit review, layout, fabrication, testing and production preparation of this device.

References

1. P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, ®1971, John Wiley and Sons, P. 415.

2. Ibid, pp.561-570.

3. Eric Bausback, "An I-Q demodulator for compressed video applications," presented at the Second Annual Wireless Symposium, Santa Clara Convention Center, Santa Clara, CA February 15-18, 1994.

Eric Bausback joined California Eastern Laboratories, Inc. in 1985 as an Applications Engineer. In 1987, he was engaged in the circuit design of power hybrid and monolithic GaAs circuits. In 1989, he became a member of the Product Development Engineering Group, wherein he was primarily engaged in the design of silicon MMIC products for CEL. These included a GPS RF downconverter, QPSK demodulators and various prescalers. He has spent one year with NEC in Japan to learn design methods, procedures and process flow associated with the development of NESAT-3 products.

Mr. Bausback received the BSEE Degree from California Polytechnic State University and the MSEE Degree from the University of Santa Clara. He is a member of the Institute of Electrical and Electronic Engineers.