Phase Locked Loop Primer and Application to Digital European Cordless Phone

The Author reviews the standard for the Digital European Cordless Telephone (DECT) and illustrates it with the design of a phase locked loop emphasizing critical design areas such as lock time, sideband rejection and phase noise effects.

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DECT is a common air (wireless) standard proposed and adopted by the European Telecommunication Standards Institute (ETSI). It describes a point to point or multipoint system to afford voice or data communications in the 1800-1900 MHz frequency range. Applications for DECT include residential cordless phones, wireless PBX and local area networks (LANs).

The standard can be described broadly as having two parts, the physical part and the network part. The physical layer includes frame structure, timing, data rate, slot assignment and voice coding, along with expected bit error rate performance. The network layer includes the method of call setup and tear-down as well as the control requirements necessary to allow this multi-party, time-division-multiple-access (TDMA) link to remain coherent. This control includes dynamic user identification and partitioning on a frequency/slot basis as well as channel monitoring to avoid collisions and maintain link integrity. Finally, call handoff is also supported by the specification.

DECT Frame Structure and Timing

The DECT standard divides the available frequency allocation into ten channels numbered 0 through 9, channel 9 being the lowest frequency. The data rate is 1152 kb/s with a bandwidth/bit-time (bt) product of 0.5. The modulation scheme is Gaussian Minimum Shift Keying (GMSK). Each RF channel is further divided into 12 time division multiple access (TDMA) channels. The RF channel spacing is 1728 KHz. Figure 1 shows the DECT frame structure, and Table 1 lists the DECT frequencies, assuming the use of low side injected mixers.

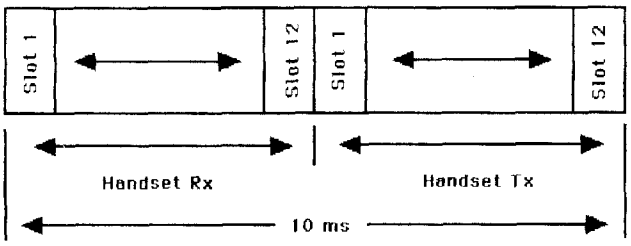

Figure 1. DECT Frame Structure.

N	Channel #	RF Freq. (MHz)	Lo Freq. (MHz)
1034	0	1897.344	1786.752
1033	1	1895.616	1785.024
1032	2	1893.888	1783.296
1031	3	1892.16	1781.568
1030	4	1890.432	1779.84
1029	5	1888.704	1778.112
1028	6	1886.976	1776.384
1027	7	1885.248	1774.656
1026	8	1883.52	1772.928
1025	9	1881.792	1771.2

Table 1. DECT frequencies.

Operation of the system can be visualized by considering Figure 1. This type of channel access is referred to time division duplex/time division multiple access (TDD/TDMA). One half the time is spent in the receive mode while the other half is spent transmitting. In either mode each user shares the available channel bandwidth with 11 other users.

A bit level view of the frame structure is shown in Figure 2. The bit time is 868 nanoseconds. The guard time allows a sufficient interval for the transmitter output power to subside, preventing leakage into the next slot.

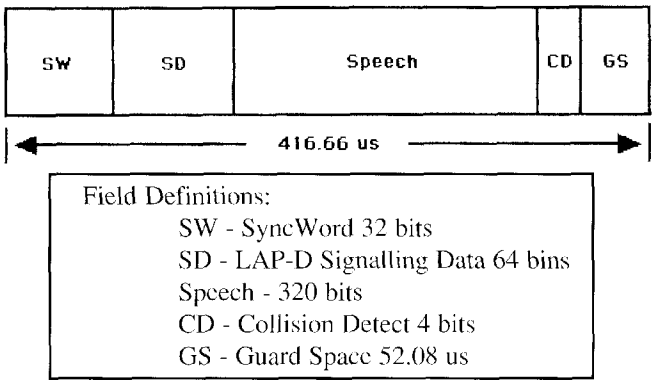

Figure 2. DECT Slot Structure.

Frame Structure Effects on PLL Lock Time

From the frame timing can be inferred the requirements of the phase locked loop (PLL) local oscillator. First note that the base station is called in DECT terms the *radio fixed part* (RFP). It can direct the *radio portable part* (RPP) or handset to park on any particular RF channel and slot. This defines the minimum usable frequency range over which the voltage controlled oscillator (VCO) must operate.

For discussion purposes assume that this PLL is being used in a synthesizer that is low side injecting the first local oscillator in a RPP receiver. The sweep range of the VCO must be (1728 KHz) x (10-1) = 15.552 MHz. This sweep range for a 110.592 MHz first I/F would then allow the VCO to run from a low frequency of 1771.200 MHz to 1786.752 MHz. High tier PLL solutions would allow this frequency range to be traversed on consecutive slots during the guard time of 58.08 microseconds.

A more common approach used to simplify the design and thus reduce the cost of the PLL is to allow for what is termed *1 blind slot operation*. In this mode the PLL is given 1 full slot time, 416 microseconds, to acquire and lock to the directed channel. Obviously in this scheme the slot time being used to lock the PLL is not available for use during this real time slot assignment process. Since the slot is not available it can not be *sniffed* for traffic and thus is *blind* to the RPP. Any detrimental effects of the scheme are minimized by the fact that the blind slot is distributed throughout all the slots on an ongoing basis. As always, when you sacrifice properly you gain something in return, in this case a reduction in loop bandwidth requirement; since we can take longer to lock the loop. This reduces the noise contribution of the loop to the system's I/F noise base. Another advantage gained is in the reduction of sideband spurs as a result of the lower loop bandwidths.

PLL Implementation

PLL Block Diagram

The closed loop block diagram of the conventional PLL is shown in Figure 3. The blocks that make up the transfer function are: Kd(s): the phase detector gain constant, given in either amps or volts per radian. F(s): the low pass loop filter transfer function given in volts/volt. Kv/s: the VCO transfer function, in radians/sec/volt. The 1/s function denotes a pure integrator, as phase is the integral of frequency and 1/N is the divide ratio

used to scale down the VCO frequency to a value usable and/or comparable to the reference oscillator.

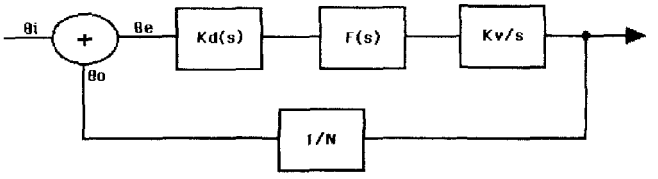

Figure 3. PLL Block Diagram.

The Loop Filter

With the exception of F(s), the loop blocks shown above are all fixed by the hardware devices chosen. For example, the Kd(s) specification of the synthesizer made by our firm is defined once the phase detector current is programmed via an external resistor. Likewise the VCO and 1/N functions all are essentially defined, given a particular vendor's VCO and divide ratio according to the reference frequency chosen. The loop filter has the primary function of adjusting the loop dynamics, i.e. lock-time, loop bandwidth, and spurious suppression. For this design a loop filter as shown in Figure 4 will be used.

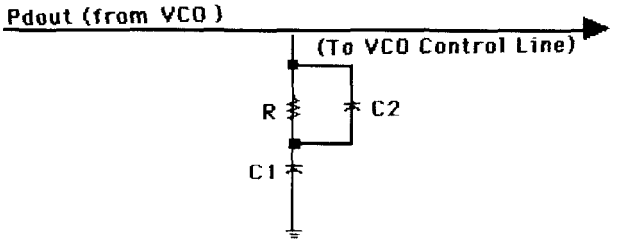

Figure 4. Type 2 Third Order Loop Filter.

The open loop transfer function of this loop is given in Equation 1, in which G(s) is the feed forward path gain and H(s) is the feedback path gain. The product G(s)H(s) is used to predict loop stability and the quantity

$$\frac{\theta_i}{1 + G(s)H(s)}$$ to check the lock time.

$$(1)\quad G(s)H(s) = \frac{Kd\ F(s)\ Kv}{S\ N}$$

The transfer function (I in versus V out) of the filter network or its impedance is found using Equation 2.

$$(2)\quad Z(s) = (R \parallel 1/C2s) + 1/C1s$$

Rearranging and simplifying yields

$$(3)\quad Z(s) = \frac{1 + t1s}{C1s} \times \frac{1}{1 + t2s}$$

which describes a lead/lag network with a pole at the origin having t1 = r(c1 +c2) and t2 = r(c2). Referring to the loop block diagram G(s)H(s) can be written in the form of Equation 4.

$$(4)\quad \frac{Kd\ Kv\ (1 + t1s)}{N\ s\ (C1\ s)\ (1 + t2s)} = \frac{Kd\ Kv}{s^2\ C1\ N} \times \frac{1 + t1s}{1 + t2s}$$

which, when expanded yields Equation 5.

$$(5)\quad \frac{Kd\ Kv + Kd\ Kv\ t1\ s}{s^3 t2\ C1\ N + s^2\ C1\ N}$$

As can be seen, this has a 3rd order s term, along with two purely factorable (distinct) integrating s terms. This type of system is classified as a type 2 third order (t23o) loop. Substituting s= jw, Equation 4 now becomes Equation 6:

$$(6)\quad \frac{Kd\ Kv}{\omega^2\ N\ C1} \times \frac{1 + j\omega t1}{1 + j\omega t2}$$

which is the more common form used to perform a Bode analysis.

Choosing the Lock Time

The method proposed to determine the lock time for a T23O loop is to use the T22O loop damping curves. Since a T23O system with a 45 degree phase margin will be well damped, a choice of wnt = 8 yields lab results which correlate well with those given by mathematical computation. An approximation of the required loop bandwidth to meet a T23O 45 degrees phase margin system is described by Equation 7.

$$(7)\quad BW_{(Hz)} = \frac{8}{(lock\ time)\ (2)\ (Pi)}$$

As noted, the lock time for a 1 blind spot system must be less than or equal to 416 microseconds. The approach used in this design will be to lock in approximately half

this allowed time, about 200 microseconds, to allow plenty of safety margin. As an initial design, select the loop bandwidth to be 6600 Hz. This will yield the required lock time.

Filter Design

The loop filter design is straightforward. The method is a minor adaptation of the approach presented in [1], wherein t1 is replaced by C1. In this approach the loop 0 dB crossing point, or the loop bandwidth as defined for type two third order systems, is forced to be coincident with the phase inflection point, in the present case 45 degrees. The principal equations used to define the loop filter time constants are:

$$t1 = \frac{1}{\omega o^2 C1} \quad , \quad t2 = \frac{\text{Sec}\theta - \text{Tan}\theta}{\omega o} \quad , \quad C1 = \frac{Kp\ Kv}{N\ \omega^2}\left(\frac{1 + j\omega t1}{1 + j\omega t2}\right)$$

Where ωo is the 0 dB crossing point of the loop's magnitude (not the 3 dB point), in this case 6600 Hz. The program shown in Appendix A calculates all of the values above when supplied with the appropriate loop constants. For a 6600 Hz loop bandwidth, the following values are specified: t1 = 58uS, t2 = 10uS, and C1 = 0.046uF. The value of R and C1 are solved using a simultaneous equation with two unknowns as follows:

(8) **R x .046 uF + R (c2) = 58us, and r (C2) = 10 us**

Solving equation 8 for R and C2 yields R = 1043 ohms and C2 = 9.58nF, approximately = .01uF. When these values are used in the circuit of Figure 4 the loop filter transfer function F(s) becomes

$$(9) \quad \frac{(1 + j\omega\ 58 \times 10^{-6})}{.046 \times 10^{-6}\ s\ (1 + j\omega\ 10 \times 10^{-6})}$$

and the overall open loop transfer function with N = 1025, **Kv = 1.256637 x 10 $^{-8}$** radians/sec/volt and **Kd = 270.56 x 10^{-6}** amps/radian becomes

$$(10) \quad \frac{270.56\ \ 10^{-6}\ \ 1.256637\ \ 10^{8}\ (1 + j\omega\ 58\ 10^{-6})}{\omega^2\ 1025\ \ .046\ \ 10^{-6}\ (1 + j\omega\ 10\ 10^{-6})}$$

A Bode plot of this function is shown in Figures 5 and 6. Note the 0 db crossing point at approximately 6600 Hz and the 45 degree phase margin.

Simulating Lock Time

Having completed the initial loop design, it is possible to simulate the lock time of the PLL. To test the lock time multiply the quantity

$$\frac{1}{1 + G(s)H(s)}$$

by the worst case frequency step function while in the frequency domain, and then plot the Inverse Laplace Transform to show the time domain response of the loop to this worst case perturbation. For DECT this perturbation corresponds to 15.515 MHz, or 95.322 kradians/sec at the phase detector input. In the frequency domain this perturbation corresponds to a $\frac{1}{s^2}$ type function with a magnitude of 95,322 radians/sec.

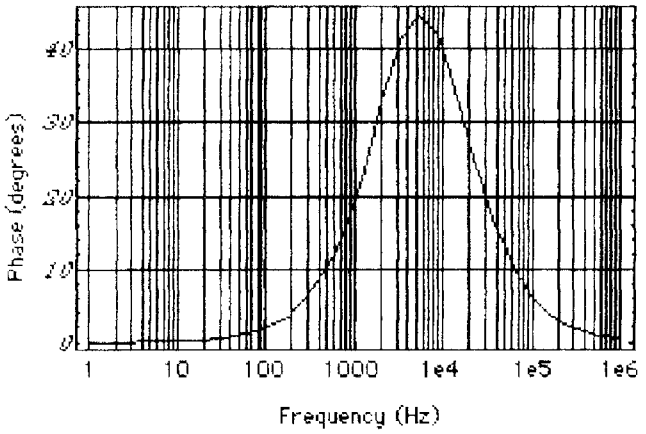

Figure 5. Type 2 third order loop phase response.

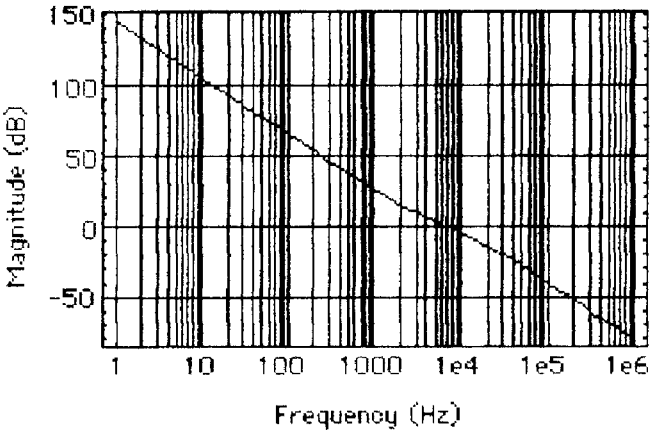

Figure 6. Type 2 third order loop magnitude response.

The results of this multiplication after simplification are (11)

$$\frac{95332\ (0.00004715 + 4.715 \times 10^{-10}\ s)}{33999.6 + 1.97198\ s + 0.00004715\ s^2 + 4.715 \times 10^{-10}\ s^3}$$

Taking the ILT of Equation 11 yields

(12)

$$\frac{5.54786}{e^{40816.2\ t}} - \frac{0.220077\ \ \text{Sin}[29849.7\ t]}{e^{29591.9\ t}}$$

$$5.54786\ \left(\frac{\text{Cos}[29849.7\ t]}{e^{29591.9\ t}} - \frac{0.991364\ \ \text{Sin}[29849.7\ t]}{e^{29591.9\ t}}\right)$$

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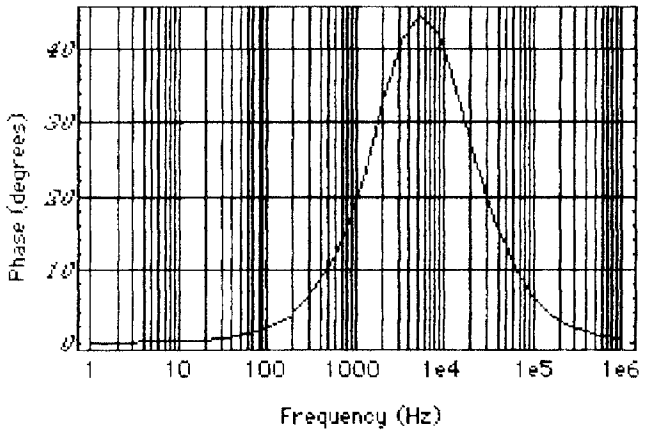
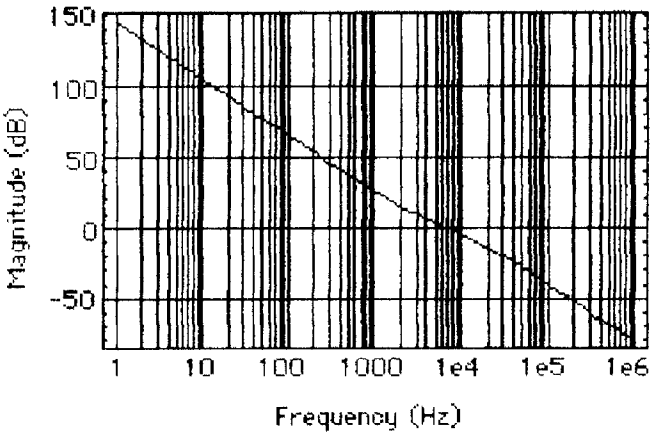


Figure 5. Type 2 third order loop phase response.



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or lesser extent common to all state of the art synthesizers. The loop designer's job is to reduce the level of the sideband spurs by proper filtering of the current sourcing/sinking output.

The first analysis step begins with a measurement of the spur current being delivered to a loop in the locked condition. The typical value for this current for a reference frequency of 100 kHz is 141 nA rms. Note that this current is proportional to the square of the reference (i.e. a 10 kHz reference would yield 1.41nA rms of spur current). Integrating this current with the loop filter transfer function, we can develop a voltage which when applied to the VCO at the reference frequency rate, will frequency modulate the VCO. Since the magnitude of this voltage and its rep rate are known, we can use the transfer function of the VCO (Hz/volt) and a calculated modulation index together with first order Bessel functions to approximate the level of the sidebands. The analysis proceeds as follows. We need the rms value of the current at the reference frequency of 1728 kHz. This corresponds to

$$\left[\frac{1728 \times 10^3}{100 \times 10^3}\right]^2 \times 141 \times 10^{-9} = 42.10 \text{ uA}$$

Next compute the impedance of the loop filter at the reference frequency

$$Z_{(filter)} = \frac{(1 + t1\ s)}{C1\ s\ (1 + t2\ s)} @\ s =$$

$$j\ 2\ pi\ 1728 \times 10^3 = 0.08851 - j\ 11.612$$

and then compute the magnitude of the this value, approximately equal to 11.612 ohms. The value of the voltage (which will drive the VCO to create the sidebands) resulting from the spur current and this magnitude of impedance is 488.8 uvolts. With this value established it is now possible to compute a modulation index (β) as

$$\beta = \frac{488.8 \times 10^{-6} \times 20 \times 10^6}{2 \times 1728 \times 10^3} = 0.00282922$$

Since the modulation index is less than 0.2 the amplitude of the first set of sidebands or the J(1) Bessel function equals $\beta/2$ or 0.00141461. This number is in units of voltage, converting it to power,

$$\text{Sideband attenuation} = 20 \log(0.00141461) = -56.98 \text{ dB}$$

With this value of attenuation we are very close to meeting our worse case requirement of -58.16 dB. Recall that the receiver side specification was much easier to meet. In order to guarantee enough margin the loop will be modified to include an additional spur filter in the form of an RC low pass section or pole. This pole will be adjusted to bring the spur level to better than -70 db below the PLL fundamental. Accordingly an additional 15 dB or better of attenuation is required referenced to 1728 kHz. The cutoff frequency of this network is determined by

$$Fc = \frac{Fr}{\sqrt{\left[\frac{1}{10^{-\frac{attn}{20}}}\right]^2 - 1}}$$

where attn is the additional attenuation required. Setting attn equal to 19.75 to make the composite attenuation greater than -70 dB yields Fc = 178.6 kHz. Standard component values of 270 ohms and 3300 pF will suffice. The complete loop filter is shown in Figure 8.

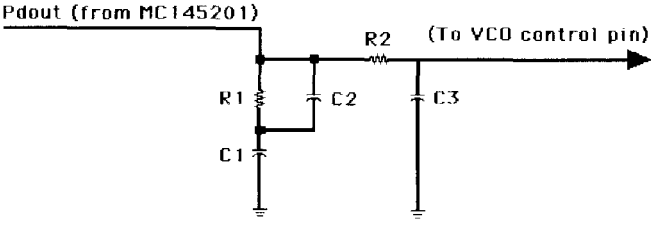

Figure 8. Type 2 fourth order loop filter.

The pre and post spur filter photos are shown in Figures 9 through 12.

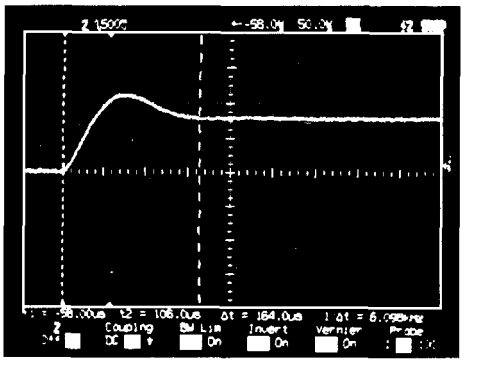

Figure 9. Pre-spur filter lock time.

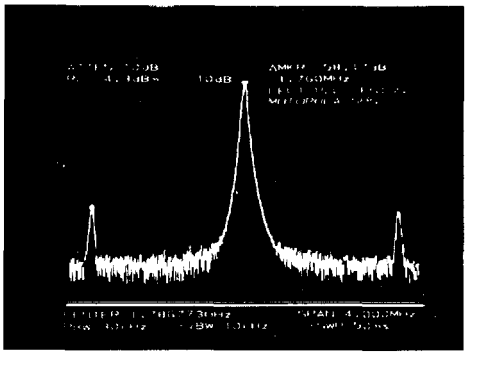

Figure 10. Pre-spur filter sideband attenuation.

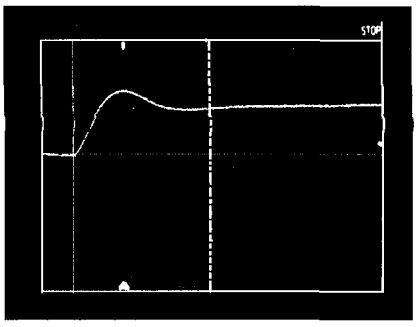

Figure 11. Lock time after addition of spur filter.

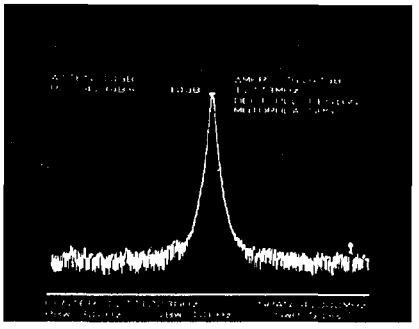

Figure 12. Side band levels after addition of spur filter.

Finally we need to simulate the composite performance of the complete loop before proceeding to the phase noise analysis of the loop. Because the cutoff frequency of the loop is greater than 10 times the loop bandwidth, we should expect this filter to have minimal effects on our initial loop phase margin and bandwidth. Again to simulate, we need to develop and plot the complete transfer function for the loop. Accordingly Equation 15 is

(15)

$$G(s)H(s) = \frac{Kd\ Kv\ (1 + t1s)\ (1 + t3s)}{Ns^4(C1t2t3) + Ns^3(C1t2 + C3t1 + C1t3) + Ns^2(C3 + C1)}$$

The Bode plot of the magnitude and phase of this equation is shown in figures 13 and 14 respectively. These plots show a new loop phase margin of 39 degrees at a loop bandwidth of 5700 Hz.

If the ILT of $\frac{1}{1 + G(s)H(s)} \times \frac{95322}{s^2}$ (rads/sec)

is taken while letting G(s)H(s) be equal to Equation 15, Equation 16 results, which when plotted will give the time domain response of the complete loop .

(16)

$$\frac{0.0000299436}{E^{1.61402 \times 10^6 t}} + \frac{3.2821}{E^{32827.8}} +$$

$$(-2.99366 + 0.988577\ I)\ E^{(-21239.2 - 32808\ I)\ t} +$$

$$(-2.99366 - 0.988577\ I)\ E^{(-21239.2 + 32808.2\ I)\ t} +$$

$$\frac{3.84063\ Sin[32808.2\ t]}{E^{21239.2\ t}} +$$

$$2.70519\left(\frac{Cos[32808.2\ t]}{E^{21239.2\ t}} - \frac{0.647375\ Sin[32808.2\ t]}{E^{21239.2\ t}}\right)$$

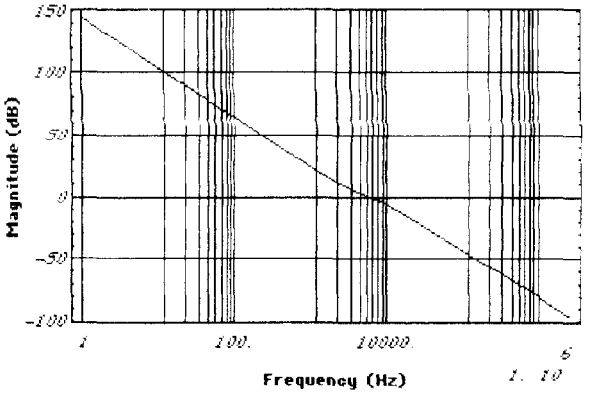

Figure 13. Type 2 fourth order loop magnitude response.

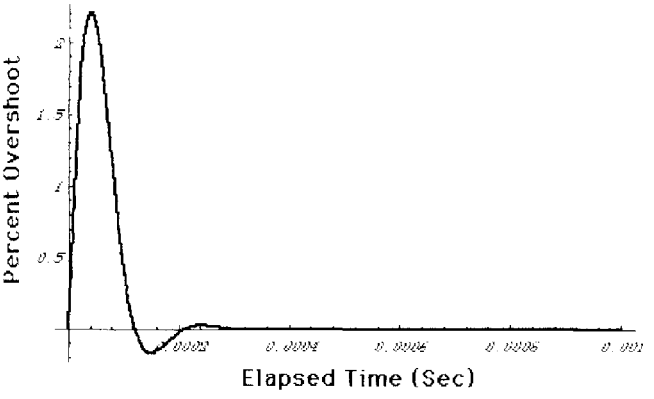

Figure 14. Type 2 fourth order loop phase response.

Figure 15 shows this response.

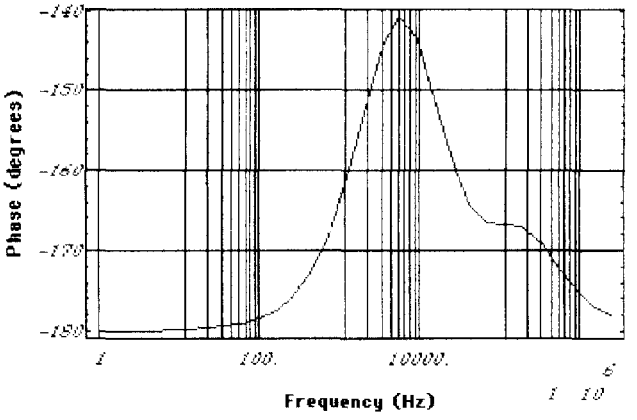

Figure 15. Type 2 fourth order step response.

Determining Overall Loop Phase Noise Performance

The concluding analysis demonstrates how to review the loop for phase noise contributions from the various sources and shows how these sources combine to yield a composite phase noise slope at the output of the VCO. This analysis uses a method outlined in [2] and some curve fitting to approximate closely the phase noise per-

The next analysis is the closed loop divider contribution to phase noise. The CMOS process is generally characterized by a fixed numerical value (in the range of -150 to -170 dBc/Hz) assigned to additive phase noise that is flat over frequency. For now let S(div) be equal to -160 dBc/Hz; the divider noise contribution is then

(19) $$Soutdiv_{(f)} = 10\ Log(10^{\frac{-160}{10}}\ ([GTR]\ 1025)^2)$$

which is plotted over frequency in Figure 19.

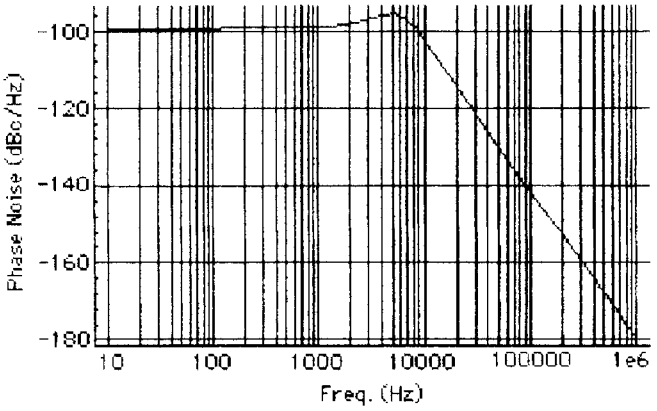

Figure 19. Closed loop divider phase noise plot.

Notice the essentially flat response out to the loop bandwidth whereupon the response drops at -40 dB/decade.

We can now evaluate the voltage regulator's effects on phase noise. Essentially the phase noise added by the regulator is a function of the rms regulation of the supply specified over some frequency range, the pushing factor of the VCO usually denoted *Kpush* in MHz/volt and GFM, the FM response of the loop.

(20)

$$Soutreg_{(f)} = 10\ Log((Kpush\ [\frac{nreg}{\sqrt{fmax-fmin}\ f}])^2\ [GFM]^2)$$

Note that Kpush is assumed to be locked in due to other factors in the design, i.e. sensitivity and cost. With nreg = 200 uvolts rms and Kpush = 2 MHz/volt, a plot of Equation 20 yields Figure 20.

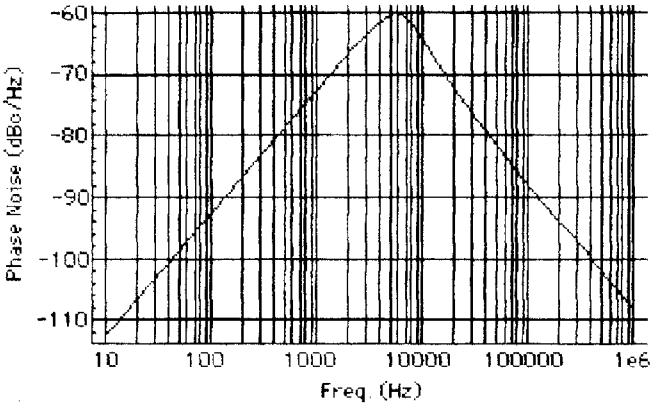

Figure 20. Closed loop regulator phase noise plot.

The last singular noise contributor is the open and closed loop VCO phase noise. As before, we need to develop a polynomial that describes the phase noise contour of the VCO based upon some sample data points obtained from the VCO data sheet. These data points are as follows: (10,-12.5),(100,-46),(1000,-76),(10000,-95),(100000,-113),(1000000,-133). Supplying these points to Mathematica[TM] and requesting a second order fit yields **Y=22.25 - 37.9375 f + 2.0625 f².**

A plot of this function is shown in Figure 21.

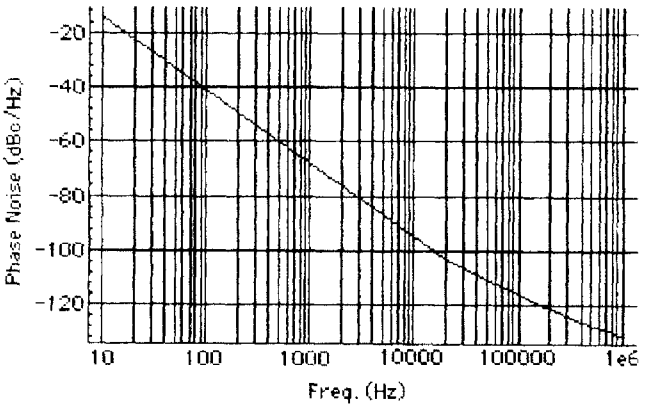

Figure 21. Open loop VCO phase noise plot.

The closed loop response is evaluated by plotting Equation 21 (Figure 22).

(21)

$$SoutVCO_{(f)} = 10\ Log\ (2\ Log^{-1}(\frac{Svco}{10})\ ([GTR])^2)$$

Note the multiplication by two because we are evaluating a double sideband noise contour.

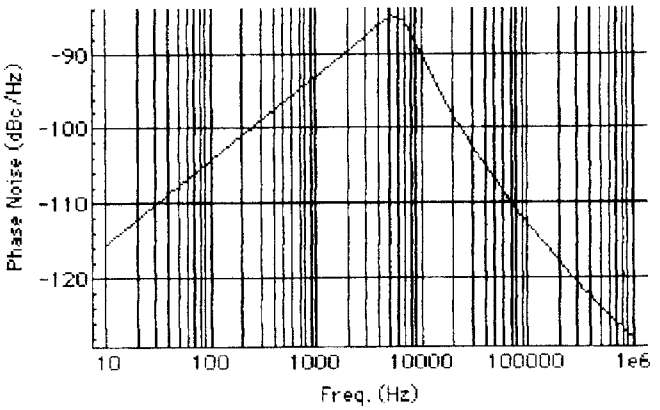

Figure 22. Closed loop VCO phase noise plot.

The overall noise performance of the loop can now be ascertained by combining all the contributors of phase noise. This is done by plotting Equation 22.

(22) **Souttot =**

$$10\,\mathrm{Log}\left(10^{\frac{Srefout}{10}} + 10^{\frac{Sresout}{10}} + 10^{\frac{Soutdiv}{10}} + 10^{\frac{Soutreg}{10}} + 10^{\frac{SoutVCO}{10}}\right)$$

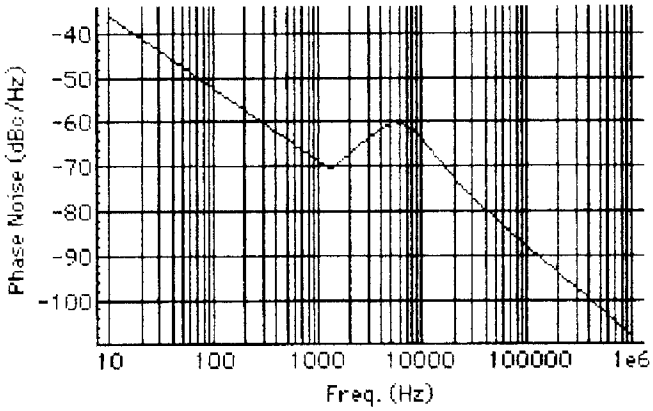

Figure 23. Composite closed loop phase noise plot.

Accumulated Phase Noise Effects on Eb/No.

The phase noise contour shown in Figure 23 can now be used to evaluate the effects of phase noise on the signal to noise ratio of the system. The phase noise curve is divided into three line segments, with an appropriate equation fitted to each. The equations for this contour are:

Segment 1 (10 to 1318 Hz)

$$0.112299\ f^2 - 16.7369\ f - 19.3754$$

Segment 2 (1318 to 4897 Hz)

$$-3.31263\ f^2 + 40.4992\ f - 164.678$$

Segment 3 (5000 to 600KHz)

$$-0.344472\ f^2 - 18.2732\ f + 12.8041$$

Note that these equations, as in previous curve fitting, assume that the Log(f), in this case frequency, is used as the actual variable value. Integrating these equations over their respective frequency range and summing the results as 10 LOG (a + b + c) gives a total phase noise component of -19.82 dBc. We assume that the noise power is symmetrical and thus the double side band component of the noise will be 3 dB greater, -16.82 dB.

To determine the effect of this phase noise component on the signal to noise ratio we calculate the thermal noise present in the system and compare the two noise sources to see which causes the greater degradation. The thermal noise present in a DECT system using GMSK modulation at a bit rate of 1152 Kb/s is

$-174\ \mathrm{dBm} + 10\ \mathrm{LOG}(1152 \times 10^3) = -113.39\ \mathrm{dBm}$

Thus with the assumption that the rest of the receiver is implemented to have an overall noise figure was 6 dB, the noise floor is at approximately -107.4 dBm. The DECT specification states that a bit error rate of 0.001 must be maintained at an input signal strength of -83 dBm. An inspection of generally available bit error probability curves indicates that a static Eb/No of 10 dB is required for this error rate. Note that since FM modulation scheme with non-coded symbols is employed, the Eb/No and S/N ratios are equal and can be used interchangeably. Given the power level of -83 dBm we can determine the signal to noise ratio established by the combination of the thermal noise and the system noise figure and compare it to the Eb/No requirement, thus

-83 dBm - (-107.4 dBm) = 24.4 dB from which it is seen that there is a margin of 14.4 dB, considering these two noise sources.

The effects of the -16.82 dBc integrated phase noise component on the system's signal to noise ratio can be explained as follows. An input signal presented to a mixer mixes with the integrated phase noise power. This mixing in effect causes the integrated power to be spread over the bandwidth of this signal and essentially creates a new noise floor that is a function of the integrated noise power relative to the carrier. In this case the carrier is the received signal and not the local oscillator, and the new noise floor is -16.82 db below this carrier.

Again, with the system implemented noise figure of 6 db this leaves approximately 0.8 dB as a margin relative to the bit error rate curves. Of course, every dB of reduced noise figure in the receiver, albeit difficult to obtain at this point since the target noise figure is already quite low, will add directly to the margin of the system. As an alternate approach to ease the task of design, particularly in the receiver, it would be advantageous to use a lower noise regulator, having better filtering, to lower the pushing effects to additive phase noise. A further step would be to invest the design with a VCO having better mid to high-end phase noise density and better pushing figure as a means of improving the integrated phase noise power.

Reciprocal Mixing Effects

The effect of the reciprocal mixing process is to sum the adjacent channel power with the noise density present on the local oscillator at an offset equal to difference in frequency between the desired and adjacent channel, 1.728 MHz in the case of DECT. For example, assume an adjacent channel power level of -55 dBm (from DECT spec) and a local oscillator phase noise density of approximately -116 dBc (extrapolated from Figure 23). At

an offset of 1728 KHz, the resulting apparent noise floor is -55 dBm + (-116 dBc) or -171 dBm. The noise floor has been degraded by 3 dB. This is because our starting reference is no longer -174 dBm but is now -171 dBm. This effect propagates through the rest of the thermal noise evaluation to cause a KTB noise floor of -110.39 dBm verses the previous noise floor of -113.39 dBm. This effect would have been more pronounced had the phase noise density been higher at the adjacent channel offset. Since, this is not the case in this system, the noise is still dominated by the phase noise contour of the local oscillator, and additional steps, as with the improvement recommendations above, need be taken if it is desired to increase the signal to noise margin.

Acknowledgments:

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John Hatchett - Staff Engineer, Motorola SPS, Phoenix, AZ

Brian Dacey - MTS, AT&T Bell Labs, Middletown, NJ.

Editor's Note:

The author's firm markets the integrated circuit synthesizer described in this article as the MC145201.

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7. Plots and miscellaneous equation solving provided by Mathematica[TM] A System of doing Mathematics by Computer.

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Appendix - A
MS-DOS Q Basic Language

```
REM PROGRAM TO CALCULATE LOOP FILTER COMPO
    NENT  VALUES FOR TYPE 2
REM 3RD ORDER PLL.
REM PASSIVE LOOP FILTER ADAPTATION OF THE AP-
    PROACH PRESENTED IN
REM PRZEDPELSKI'S ARTICLE REPRINTS (AR254) FROM
    MOTOROLA SPS
REM AVF 1/23/94
1 OPEN "TEST.DAT" FOR OUTPUT AS #1
5 PI = 3.14159
10 CLS
11 DEFDBL A, Z
20 INPUT "ENTER PHASE DETECTOR GAIN CONSTANT
        (VOLTS/RAD) ", KD
30 PRINT
40 INPUT "ENTER VCO GAIN CONSTANT (RADIANS/VOLT)
        ", KV
50 PRINT
60 INPUT "ENTER REF FREQ. MULTIPLICATION FACTOR
        (N)                ", N
70 PRINT
80 INPUT "ENTER REF FREQ (HZ)                ", RFQ
90 PRINT
101 INPUT "ENTER DESIRED LOOP BANDWIDTH
        (Hz)                ", DLB: PRINT
102 REM IF DLB > RFQ / 50 THEN PRINT "LOOP BW OUT
        OF RANGE": GOTO 101
110 Wo = 2 * PI * DLB
120 INPUT "ENTER DESIRED LOOP PHASE MARGIN (DE
        GREES)    ", DPM
121 PRINT
130 WPM = DPM: REM + 57.3 * ATN(DLB / VMB) + (360 *
        DLB * (N - 1) / (2 * PI * RFQ * N))
140 T3 = ((1 / COS(WPM / 57.3)) - TAN(WPM / 57.3)) / Wo
150 T2 = 1 / (Wo ^ 2 * T3)
151 T1MAGN = SQR((Wo * T2) ^ 2 + 1)
152 T1MAGD = SQR((Wo * T3) ^ 2 + 1)
160 T1 = (KD * KV) / (N * (Wo ^ 2)) * (T1MAGN / T1MAGD)
162 CLS
163 PRINT "      Filter network Time Constants as Follows:":
    PRINT
```

```
165 PRINT "              C1 = "; : PRINT USING ("###.######");
    T1; : PRINT "      "; "  or "; T1; "Farads"
166 PRINT "              T1 = "; : PRINT USING ("###.######");
    T2; : PRINT "  Sec. "; "  or "; 1 /T2; "Hz"
167 PRINT "              T2 = "; : PRINT USING ("###.######");
    T3; : PRINT "  Sec. "; "  or "; 1 / T3; "Hz" 168 PRINT
211 PRINT "FREQ", "MAG OF GH(S) (DB)", "  PHASE MAR
    GIN (DEG)"
220 FOR FREQ = 1 TO 100000 STEP (FREQ * 10)
221 W = FREQ * 2 * PI
285 TMP1 = ((KD * KV) / (N * W ^ 2 * T1))
286 GHN = SQR((W * T2) ^ 2 + 1)
287 GHD = SQR((W * T3) ^ 2 + 1)
288 GHM = 20 * .43429 * LOG(TMP1 * (GHN / GHD))
290 GHP = -180 + ((ATN(W * T2) - ATN(W * T3)) * 57.3)
292 DNR = TMP1 * (GHN / GHD) * COS(GHP / 57.3): REM
    REAL NOISE DENOM
294 DNI = TMP1 * (GHN / GHD) * SIN(GHP / 57.3): REM
    IMAG  NOISE DENOM
296 DNR1 = DNR + 1
298 DNMAG = SQR(DNR1 ^ 2 + DNI ^ 2): REM MAG OF
    REAL  AND IMAG
299 NMAG = 20 * .43429 * LOG(1 / DNMAG)
300 PRINT FREQ,
302 PRINT USING ("######.##"); GHM;
303 PRINT "                    "; GHP
330 FREQ = FREQ * 10
335 PRINT "NOISE MAG    ", NMAG
340 NEXT FREQ
350 END
```

Appendix - B
Motorola 68 HC05 Assembly Language

```
;*****************************************************************
;** ROUTINE TO LOAD MC145201 REGISTERS AND CHECK
;   FULL BANDWIDTH
;** HOP SETTLING TIME
;** AVF 4/11/94
;** ROUTINE IS WRITTEN TO RUN ON AN 68HC05C9 EVM
;   BOARD
;** BUT CAN BE EASILY MODIFIED TO RUN ON ANY EVM
;   WITH AN
;** SPI PORT
;** STARTING LOCATION FOR PC = $0C00
;** WHILE RUNNING, THE LOOP WILL CONTINUALLY
;   JUMP FROM
;** DECT CHANNEL 0 TO 9
;*****************************************************************
;** REGISTER C - CONFIG REG    BIT#
;                    0 - OUTB FUNCTION 0 = 0 1 = HI Z
;                    1 - OUTA FUNCTION PORT OR PDOUT
;                        CURRENT CNTRL
;                    2 - PDOUT CURRENT SELECT
;                    3 - PDOUT CURRENT SELECT
;                    4 - STANDBY 0 = GO, 1 = STANDBY
;                    5 - LOCK DETECT ENABLE
;                    6 - PD SELECT 0 = VR,VV, 1 = PDOUT
;                    7 - PDPOL 0 = NO INVERT, 1 = INVERT
;
;** REGISTER A - A,N DIV
;                    0  - 7  A COUNTER DIVIDE 0->63
;                    8  - 19 N COUNTER DIVIDE 5->4095
;                    20 - 21 NOT USED (MUST BE 1)
;                    22 - 23 OUTA SELECT PORT,DOUT,
;                            FV,FR
;
;** REGISTER R - REF DIV
;                    0  - 12 REF DIVIDE 0 -> 8192
;                    13 - 15 MODE SELECT CRYSTAL,
;                            REF MODE, REF W/DIV
;
;              SYSTEM EQUATES
RREGL   EQU $50     ;TEMP STORAGE FOR R-REGL DATA
RREGH   EQU $51     ;TEMP STORAGE FOR R-REGH DATA
CREG    EQU $53     ;TEMP STORAGE FOR C-REG DATA
AREGL   EQU $54     ;TEMP STORAGE FOR A-REGL DATA
AREGM   EQU $55     ;TEMP STORAGE
AREGH   EQU $56     ;TEMP STORAGE
OUTLP   EQU $57     ;TEMP STORAGE
SPIDT   EQU $0C     ;SPI DATA REG
SPIST   EQU $0B     ;SPI STATUS REG
SPICN   EQU $0A     ;SPI CONTROL REG
PTADT   EQU $00     ;PORT A DATA REG
PTADD   EQU $04     ;PORT A DATA DIR REG
PTDDD   EQU $07     ;PORT D DATA DIR REG (ENABLES
;                    SPI PIN I/O)
;
;** PLL REGISTER INITS
;
        ORG $800
ENTRY0  LDA #$A0    ;SET REFOUT= REFIN/2 AND REF
;                    DIV = 12
        STA RREGH
        LDA #$0C
        STA RREGL   ;R-REG NOW CONFIGURED
        LDA#$6C     ;SELECT NOINV,PDOUT,LDE,NO
;                    STBY,MAXI,10%STEPS,BOUT=0
        STA CREG    ;C-REG NOW CONFIGURED
        LDA #$B0    ;SELECTOUTA =
;                    FV,NDI=1024,ADIV=0
        STA AREGH
        LDA #$10
        STA AREGM   ;DIV = 16*64+1
        LDA #1
        STA AREGL   ;A-REG NOW CONFIGURED
        RTS
;** PORTA & D REGISTER INIT
;
        ORG $900
ENTRY1  LDA #$FF    ;SET PORTA ALL OUTPUTS
        STA PTADD
        STA PTADT   ;MAKE ALL BIT HIGH (ONLY USING
;                    BIT 0 FOR THE ENABLE)
        LDA #$DA    ;MAKE MOSI AND SCLK OUTPUTS
;                    ,SS/ AN INPUT (FOR HC05C9)
        STA PTDDD
        RTS
;
;** SPI REGISTER INIT
;
        ORG $0A00
```

```
ENTRY2 LDA #$51      ;SET CLK IDLE=LOW,RATE=ICLK/4,
;                    DATA SETUP BEFORE RE
       STA SPICN     ;DONE
       LDA SPIST     ;DUMMY STATUS READ (C9 EVM
;                    QUARK)
       LDA #00       ;
       STA SPIDT     ;DUMMY WRITE
       RTS
;

       ORG $0B00
START  LDA SPIST     ;GET CURRENT SPI STATUS
       AND #$80      ;SPI BUSY?
       BEQ START     ;WAIT FOR NOT BUSY
       LDA #$FE
       STA PTADT     ;SET PORTA BIT 0 LOW (ENABLE
;                    TO MC145201)
       LDA RREGH     ;GET R-REG MSB
       STA SPIDT     ;WRITE IT
       JSR GETSTAT ;GET SPI TRANSFER STATUS
       LDA RREGL
       STA SPIDT     ;WRITE IT
       JSR GETSTAT
       LDA #$FF
       STA PTADT     ;SET PORTA BIT 0 = 1 (LOADS R-
;                    REG 1ST BUFFER)
       LDA #$FE
       STA PTADT     ;SET PORTA BIT 0 = 0
       LDA CREG
       STA SPIDT     ;WRITE CREG
       JSR GETSTAT
       LDA #$FF
       STA PTADT     ;SET PORTA BIT 0 HIGH (LOADS C-
;                    REG)
       LDA #$FE
       STA PTADT     ;GET READY TO CONFIGURE A-
;                    REG
       LDA AREGH
       STA SPIDT     ;WRITE AREG BITS 16-24
       JSR GETSTAT
       LDA AREGM
       STA SPIDT     ;WRITE AREG BITS 15-8
       JSR GETSTAT
       LDA AREGL
       STA SPIDT     ;AREG NOW CONFIGURED (A,N,R
;                    COUNTERS NOW WRITTEN)
       JSR GETSTAT
       LDA #$FF
       STA PTADT     ;CLOSE OUT TRANSFER, WRITE
;                    ALL COUNTERS
       LDA #$FE
       STA PTADT     ;LOWER ENABLE LINE
       LDA CREG      ;GO DO CREG AGAIN
       STA SPIDT
       JSR GETSTAT
       LDA #$FF
       STA SPIDT     ;NEGATE ENABBLE LINE
       RTS
DELAY  LDA #$3F      ;OUTER LOOP COUNT
DELAY1 STA OUTLP
       LDX #$FF      ;FREQ JUMP DELAY LOOP
DELAY2 DECX
       BNE DELAY2
       LDA OUTLP     ;GET OUTER LOOP COUNT
       DECA
       BNE DELAY1
       RTS
SWHFREQ LDA #$0A
       STA AREGL     ;SET LARGER DIVIDE RATIO
       RTS
SWLFREQ LDA #1
       STA AREGL
       RTS
;** SPI TRANSMIT STATUS SUBROUTINE
;
GETSTAT LDA SPIST
       AND #S80      ;SPI STILL BUSY?
       BEQ GETSTAT
       RTS           ;OK TO XMIT ANOTHER BYTE
;**
       ORG $0C00
MAIN   JSR ENTRY0    ;LOAD UP TEMP REG STROAGE
;                    WITH CONFIG VALUES
       JSR ENTRY1    ;INIT PORTA
       JSR ENTRY2    ;INIT SPI
       JSR START     ;LOAD UP PART
MAIN1  JSR DELAY     ;DO DELAY
       JSR SWHFREQ   ;RECONFIGURE FOR HIGH
;                    FREQ DIV
       JSR START
       JSR DELAY     ;DO DELAY AGAIN
       JSR SWLFREQ   ;RECONFIGURE FOR LOW
;                    FREQ DIV
       JSR START     ;LOAD UP PART
       JMP MAIN1     ;TOGGLE VCO FREQ
       END
```