3 Volt MMIC Power Amplifier For Wireless Phones

The elimination of dual voltage requirements for wireless PBX (WPBX) and Digital European Cordless Telephones (DECT) provides a significant cost advantage. The author descrives linear and non-linear designs for single bias, 3 volt, 1900 MHz amplifiers costing under $5.

James R. Griffiths
ITT Gallium Arsenide Technology Center
Roanoke, Virginia

Wireless PBX (WPBX) telephones and Digital European Cordless Telephones (DECT) soon will be introduced in the USA and Europe. Digital WPBX phones, which are loosely based on the European DCS1800 standard, will become an extension of the conventional office telephone, while DECT phones will become the standard cordless telephone for home subscribers. In addition, DECT will find applications in the office environment, because it can handle both voice and data.

It is expected that the growth of WPBX and DECT will be substantial over the next few years, with millions of phones being manufactured each year. The phones, which operate near 1900 MHz, must be very small, battery efficient and inexpensive. A linear RF power amplifier is required for WPBX and a highly efficient RF power amplifier for DECT. The plastic packaged power amplifiers described in this paper cost less than $5 and meet the requirements of the two systems.

This paper describes a power amplifier design that is realized using a self-aligned gate FET optimized for low voltage operation; the amplifier operates from a single 3 volt DC power supply. Until recently, heterojunction bipolar transistors (HBTs) and silicon transistors were the only devices which could operate from a single DC voltage.

Normally depletion mode MESFETs require an additional negative gate voltage to control the drain-to-source current. But this negative gate voltage requirement adds cost and complexity to the finished wireless communications product, because an additional battery or power supply must furnish it. Also the MESFET power supplies must be switched on and off in the proper sequence to prevent damage, thereby adding another level of complexity. Thus, a single voltage amplifier is a doubly significant improvement.

Finally, an additional cost reduction in these telephone amplifiers can be obtained by designing them for plastic encapsulation in a SOIC-16 outline, permitting low cost, surface mount assembly into the telephone circuit. As will be seen, modelling of the package at 1900 MHz was the key to its successful use in this application.

During device development, data obtained from I-V curves (Figure 1) showed thatoperating at IDSS would yield a ClassA amplifier. Grounding the source and DC-grounding the gate on the MESFET resulted in a single-supply power amplifier (Figure 2).

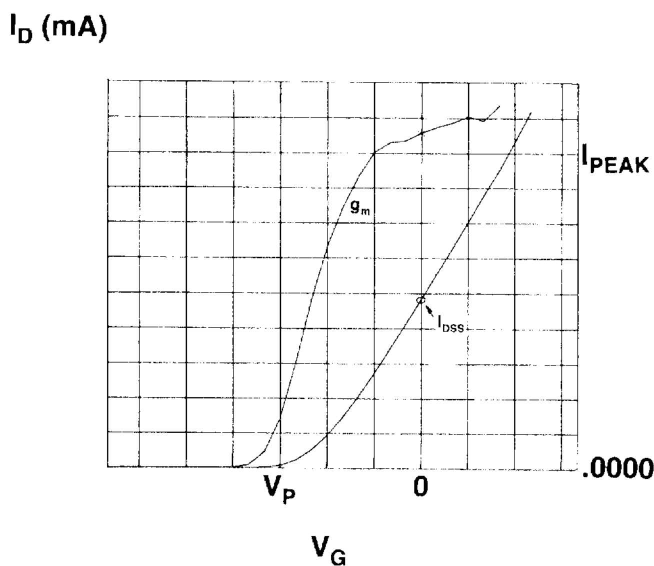


Figure 1a. Transfer Curve.

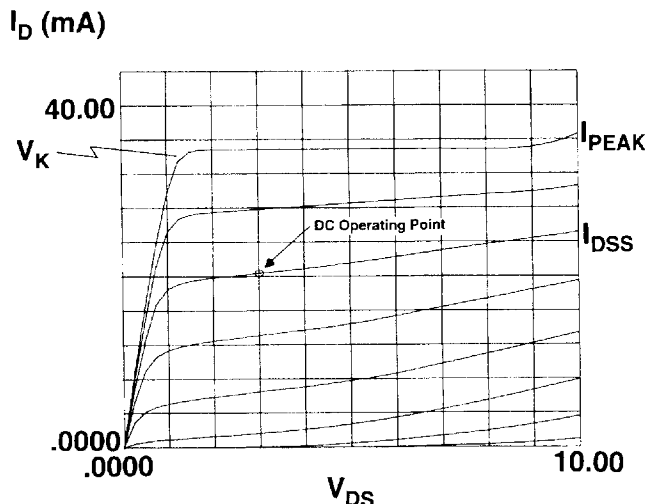


Figure 1b. I-V Curves.

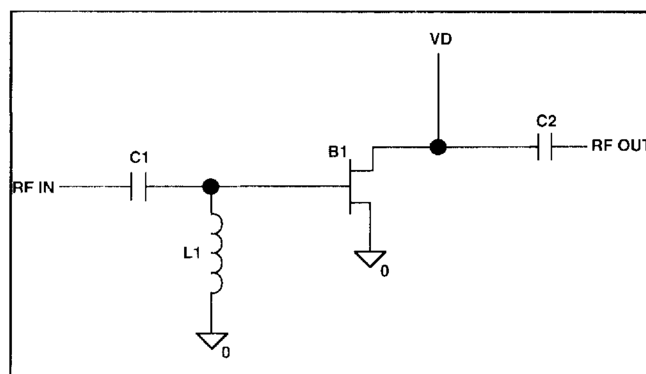


Figure 2. Schematic of grounded gate amplifier.

Load-pull measurements indicated we could obtain more than 45% Power Added Efficiency (PAE) while operating the device in a compressed Class A mode. Typical load-pull data for a 1.2 millimeter (mm) MESFET made with the self aligned process are shown in Table 1. Calculations from I-V data predicted a 31% PAE for a Class A amplifier at the 1 dB compression point and this was verified by measurement (Table 2). It is to be noted that the text-book, Class A amplifier drain efficiency (DE) of 50% presupposes that the knee voltage at IPeak is 0V.

INPUT POWER (dBm)	OUTPU POWER (dBm)	GAIN (dB)	GAIN COMPRESSED (dB)	PAE (%)	ID (mA)
-20.00	2.07	22.07	0.00	0.30	182.44
-18.00	4.06	22.06	0.01	0.47	182.33
-16.00	6.09	22.09	-0.03	0.75	181.89
-14.00	8.08	22.08	-0.02	1.19	181.00
-12.00	10.13	22.13	-0.07	1.91	180.11
-10.00	12.15	22.15	-0.08	3.07	178.67
-8.00	14.15	22.15	-0.09	4.91	177.11
-6.00	16.15	22.15	-0.09	7.85	175.56
-4.00	18.10	22.10	-0.04	12.47	173.11
-2.00	19.88	21.88	0.19	19.25	168.56
0.00	21.28	21.28	0.78	27.69	161.78
2.00	22.14	20.14	1.93	35.10	154.89
4.00	22.67	18.67	3.40	40.35	151.44
6.00	23.13	17.13	4.94	44.59	151.44
8.00	23.52	15.52	6.55	47.90	152.89
10.00	23.82	13.82	8.25	49.73	155.56
12.00	24.02	12.02	10.04	50.16	158.00

Table 1. 1.2 mm load-pull data compressed class-A, 3.0vds.

KNEE VOLTAGE (VK) = 1.2V
PEAK CURRENT (IP) = 276 mA
SATURATION CURRENT (IDSS) = 132 mA
POWER (mW/mm) = (2* (3VDS-VK)*IP)/8 = 124.2
DE (%) = 124.2/(3VDS*IDSS)*100 = 31

Table 2. Prediction of drain efficiency from I-V data.

Typically in designs above 3 GHz, distributed matching techniques are used. However, to meet the $5 cost goals for this power amplifier, a die size of 2 sq. mm was dictated. Consequently, lumped element matching was the most cost effective, given the chip size requirements.

Commercially available microwave simulation tools for transmission line matching generally are quite accurate. However, lumped element inductor models are difficult to simulate due to their self resonant frequency and loss. An effort was started early in the project to develop inductor models that were scaleable and optimized for inductance per unit area (cost) and Q (insertion loss). To accomplish this task, an electro-magnetic (EM) simulator[2] was used to develop a family of rectangular inductors.

The rectangular inductor was selected over spiral inductors due to its inherently higher inductance per unit area. The EM simulation showed that 4 inductor pitches (width/space in micro-meters) could cover our requirements. These pitches are: 50/6, 50/10, 30/6 and 20/6. The discrete model of the inductor is shown in Figure 3 andplots from the scaleable model are shown in Figure 4.

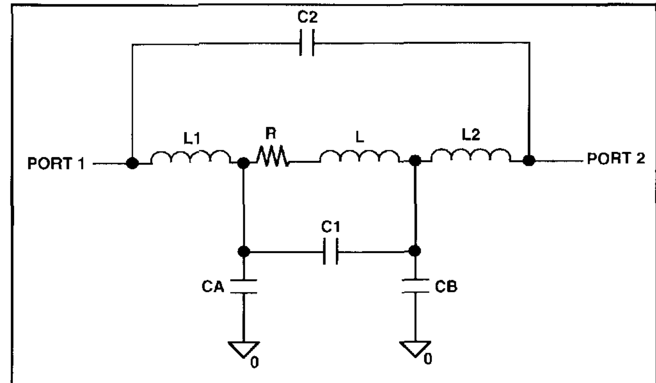


Figure 3. Inductor model.

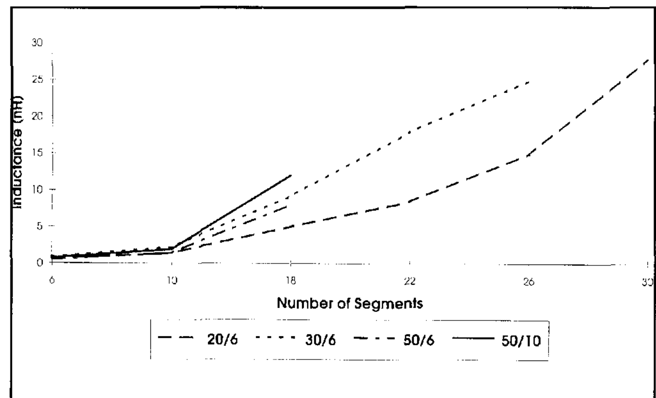


Figure 4. Effective scaled inductance at 1 GHz.

The initial amplifier goals are described in Table 3. However, during the course of this project, it became apparent that the requirements for PBX and DECT would be better served by separate linear and non-linear power amplifier designs.

Frequency	**1800 to 1900 MHz**
Power Out	**27 dBm (0.5 Watt)**
Input Power	**0 dBm (1 mW)**
Stability	**Unconditionally stable**
Available DC Power	**3 Volts**
RF Impendence	**50 Ohms**
Power Added Efficiency>	**25% (DECT has a 4% duty cycle)**
Packaging	**SOIC 16**

Table 3. Initial goals for the single voltage amplifier design.

For WPBX applications, wherein high linearity is required, a Class A amplifier is the better choice. The Class A amplifier bias point is centered in the I-V curve, allowing the input/output voltage to sweep the maximum range on the load line before clipping occurs. The linear amplifier is seldom operated at the 1 dB compression point. Rather, in actual operation. It will be backed off 5 to 20 dB.

For DECT applications, and in any other Time Division Multiple Access (TDMA) system wherein non-linear amplification is allowable, lower PAE can be accepted since the transmitter operates for only 4% of the total communication time. Therefore a non-linear amplifier for this application was designed to be driven compressed-class-A.

The linear and non-linear power amplifiers were designed from load-pull measurements, I-V data and Cripps' method[3]. Load pull measurements indicated 120 to 150 mW/mm operating at 3.0V. To insure good performance at the outset, the MESFET's chosen were designs already available from process development, with known performance characteristics. These MESFETs included models with gate peripheries of 0.3, 0.6, 1.2, 2.4, 3.6, 4.8, and 7.2 mm.

Linear Amplifier

In the linear amplifier the MESFET used in the first stage must be oversized 3 to 5 dB. This was accomplished using a 1.2 mm MESFET which can provide 20 dBm with 0 dBm drive.

Non-linear Power Amplifier

For the 0.5W non-linear power output, a 3.6 mm MESFET driven 3 to 5 dB into compression was chosen. The device has compressed gain of outputs of both the linear and non-linear power amplifiers. In this non-linear amplifier, a 0.3 mm MESFET for the first stage amplifier was chosen. This device can deliver 16 dBm and has over 15 dB of gain.

Matching Circuits

The output match for a power amplifier is critical. The insertion loss of the matching structure must be kept below 0.5 dB. This is difficult when using matching structures on the IC. Rectangular inductor Q's range from 10 to 25 resulting in losses from 0.8 to 0.3 dB respectively. The output match for the 3.6 mm MESFET corresponds to a reflection coefficient in a 50 ohm circuit having a magnitude of 0.855 at an angle of 180 degrees.

Both high-pass and low-pass matching circuits could be employed with equal success. The high-pass requires only two elements (series capacitor, shunt inductor) while the low-pass needs 3 elements (series inductor, shunt capacitor and a DC blocking capacitor). The fewer element high-pass matching circuit was chosen, for which the insertion loss is 0.4 dB.

To achieve unconditional stability, a 3 ohm resistor was added to the gate. The input match for the 3.6 mm MESFET was determined from small signal S-parameters.

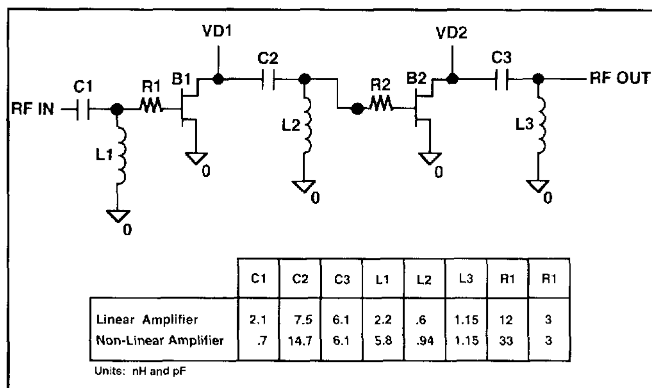
Both the 0.3 and 1.2 mm MESFETs were power matched to the output stage. For the 0.3 mm MESFET, the output match referred to 50 ohms was 0.08 at 180 degrees and the 1.2 mm MESFET was 0.48 at 180 degrees. Both first stage MESFETs were directly matched to the second stage using a high-pass structure, requiring the fewest matching components and providing a DC ground for the second stage.

The first stage was small signal matched at the input. Again, high-pass matching was utilized to provide the DC block and DC ground for the MESFET.

Plastic Package Effects

It was not known during the design what the effect would be of the plastic package on the GaAs integrated circuit (IC). A modest study effort was conducted in cooperation with the Virginia Polytechnic Institute and State University to measure and model the effects of plastic (dielectric and loss tangent) on the inductors, capacitors, and MESFETs. The lead frame effects (source and lead inductance) comprised a part of this study, too.

The results of this effort and in other published work[4] indicated that a lead inductance of 1.5 nH could be expected for this package. This was taken into account in the circuit design of the amplifier and the specific value of this inductance was incorporated into the designs of the input and output matching circuits. The complete schematics for the linear and non-linear amplifiers are shown in Figure 5 and an IC layout in Figure 6.



	C1	C2	C3	L1	L2	L3	R1	R1
Linear Amplifier	2.1	7.5	6.1	2.2	.6	1.15	12	3
Non-Linear Amplifier	.7	14.7	6.1	5.8	.94	1.15	33	3

Units: nH and pF

Figure 5. Linear power amplifier schematic.

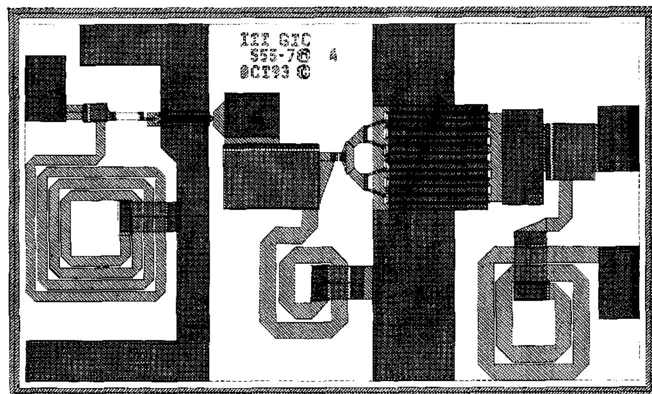


Figure 6. Power amplifier IC layout.

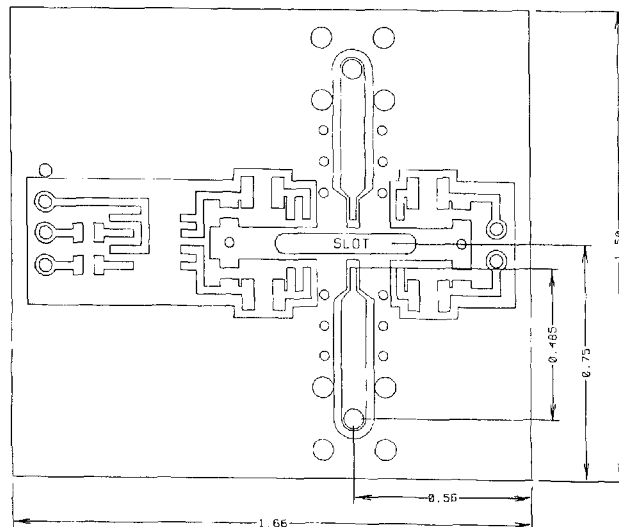
Test Circuitry

The final problem addressed was how to demonstrate the packaged power amplifiers and how to control the bias. The standard board material used in commercial systems is FR-4. This board material is low cost and easily processed, however it is not a low loss and consistent dielectric constant microwave substrate. To minimize inaccuracies that might arise in its use as a test board, a quasi-microstrip/grounded co-planar wave-guide transmission line test circuit was chosen (Table 4).

BOARD MATERIAL	FR-4
DIELECTRIC CONSTANT	4.6
LOSS TANGENT	0.03
BOARD THICKNESS	60 MILS
METALIZATION THICKNESS (COPPER OZ, SOLDER 1 OZ)	2.8 MILS
LARGE LINE WIDTH GAP	78 MILS 25 MILS
SMALL LINE WIDTH GAP	20 MILS 10 MILS

Table 4. Demonstration Board 50 ohm line.

Calibration standards were developed (short, open, load and thru) to determine the insertion loss of the test board design and to remove by calibration its loss and reflection characteristics from the measurements. As measured, the test circuit standard has 30 dB return loss and 0.2dB insertion loss. The board layout is shown in Figure 7. The slot shown in the Figure was not used for this design.



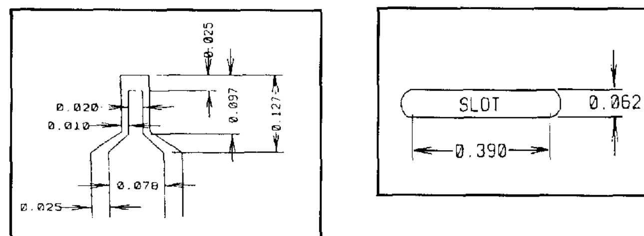


Figure 7. Demonstration Board layout.

DC Power Control

A major problem to be addressed was control of the DC power. Typically this would have been addressed using dual gate MESFETS, wherein the second gate would be used for output power control. However, due to the non-linearities and additional modeling effort that would be required had dual-gate MESFETs been so employed, silicon P-MOSFET switches were utilized instead. These devices are CMOS compatible, operate at 3V, are inexpensive and provide for RF attenuation by means of partial conduction. In addition, the 10 micro-second turn-on/off requirement can easily be met with a single series resistor.

input and output tuning to achieve these respective performances.

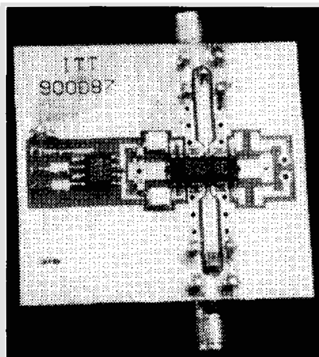


Figure 8. Demonstration Board

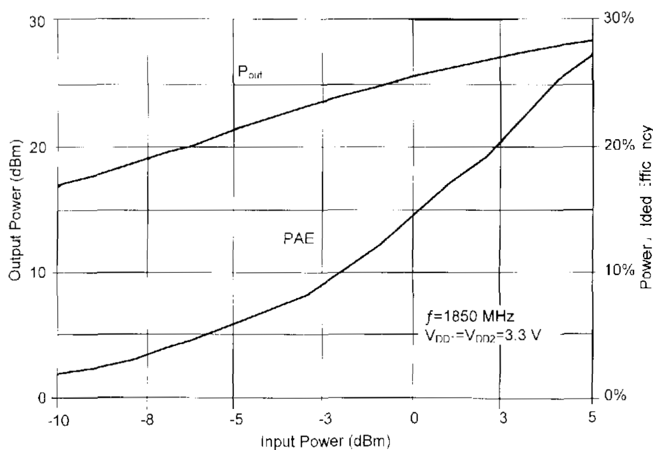


Figure 9. Output power and efficiency versus input power, for linear power amplifier.

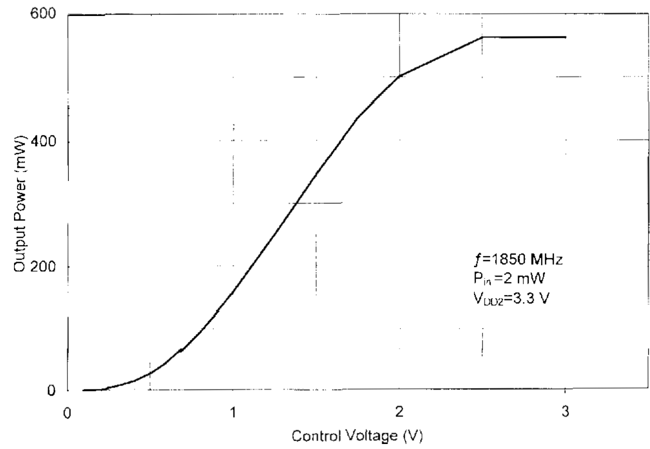
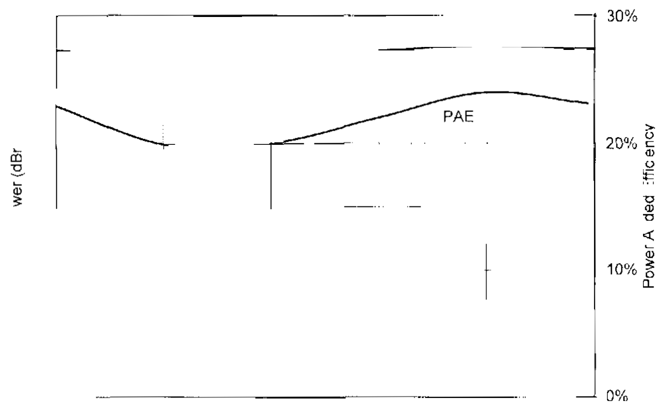
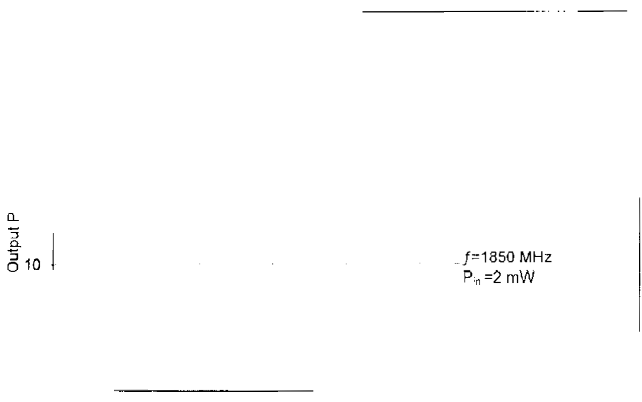


Figure 10. Output power versus control voltage (VDD1), for





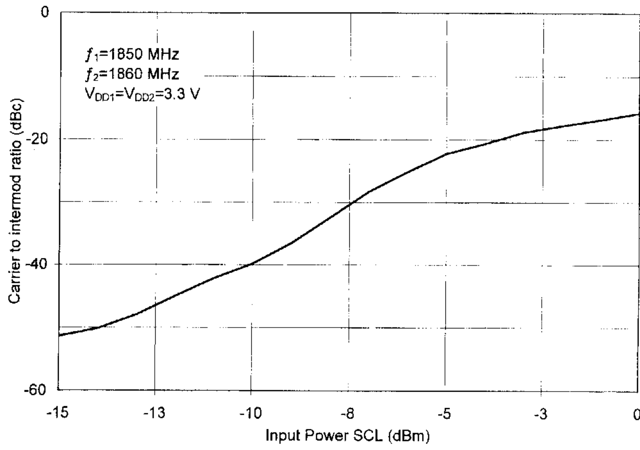


Figure 13. Carrier to intermodulation ratio as a function of input power, for linear power amplifier.

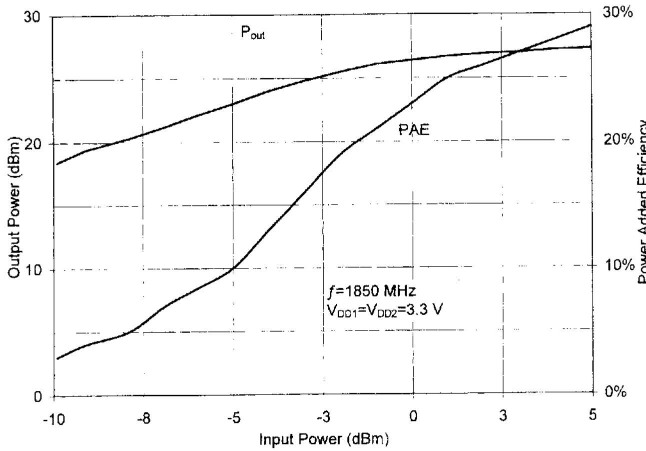


Figure 14. Output power and efficiency versus input power for non-linear power amplifier.

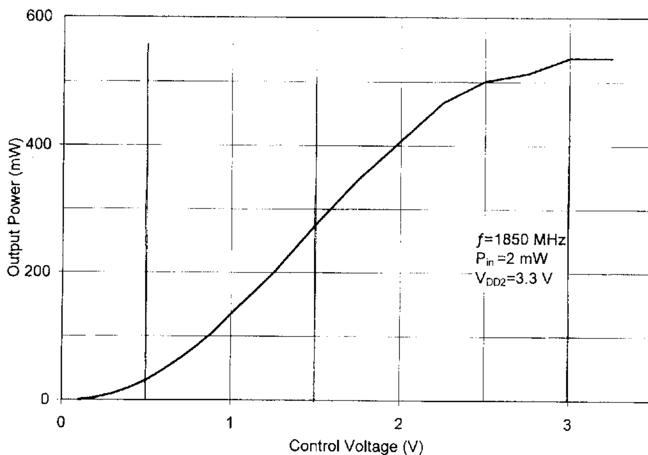


Figure 15. Output power versus control voltage (VDD1), for non-linear power amplifier.

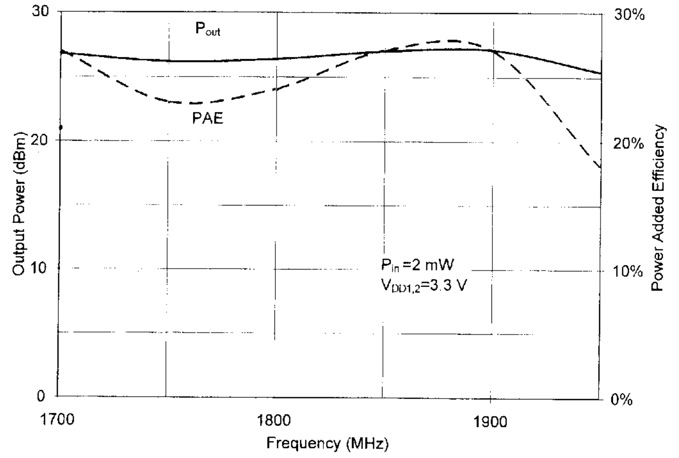


Figure 16. Output power and efficiency versus frequency, for non-linear power amplifier.

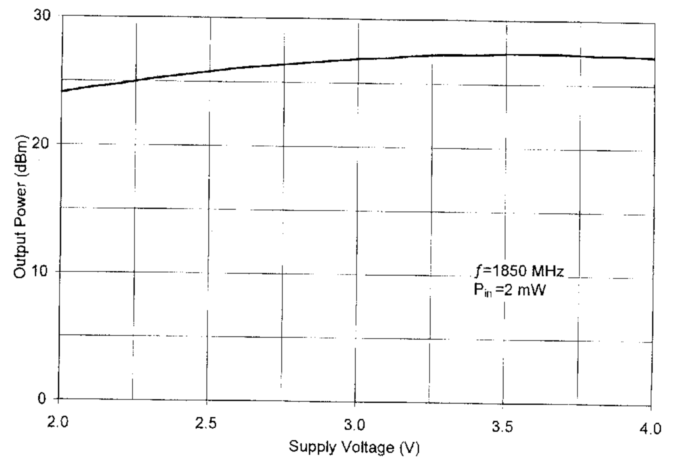


Figure 17. Output power versus supply voltage for non-linear power amplifier.

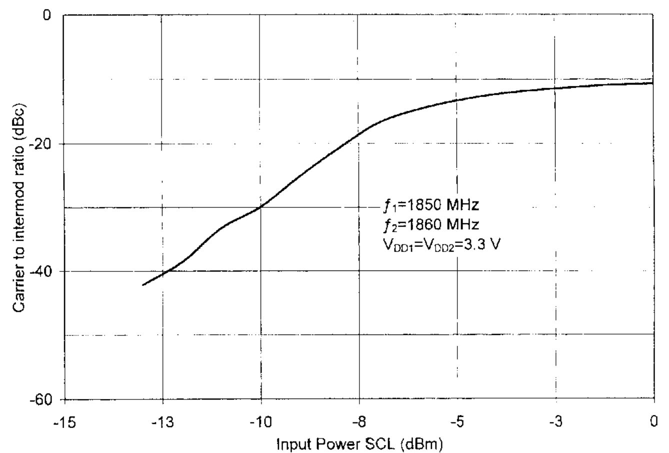


Figure 18. Carrier to intermodulation ratio as a function of input power for non-linear power amplifier.

These results represent what was obtained on a first pass design basis using the self aligned process opti-

mized for single bias, Class-A, 3 volt operation. The reproducibility of the results has been established by measuring devices assembled from different wafers.

Next, the design will be fine tuned to eliminate the need for external matching, resulting in devices that have 50 ohm input and output match. Also, the PAE will be increased to 40% minimum for the DECT power amplifier.

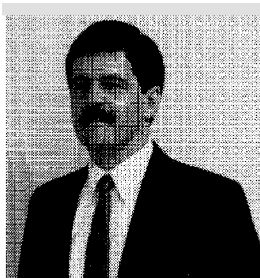
References

1. I.J. Bahl et al., "Multifunction SAG Process for High-Yield, Low-Cost GaAsMicrowave Integrated Circuits," IEEE Trans. Microwave Theory Tech., vol. 38, pp. 1175-1182.

2. Zeland Software, Inc. 3910 Mission St. San Francisco, Ca. 94112.

3. S.C. Cripps, "A Theory for the Prediction of GaAs Load-Pull Power Contours," IEEE MTT-S Int'l. Microwave Symposium Digest, 1983, pp. 221-223.

4. F. Ndagijimana et al., "The Inductive Connection Effects of a Mounted SPDT in a Plastic SO8 Package," IEEE MTT-S Int'l. Microwave Symposium Digest, 1993, pp. 91-98.



James R. Griffiths received the BSEE Degree from Purdue University and the MSEE Degree from Arizona State University in 1976 and 1981 respectively. From 1976 to 1978 he was engaged as a systems engineer at Sperry Flight Systems in Phoenix Arizona. In 1978 he joined Motorola Government Electronics Group to perform microwave test, circuit and system design. In 1982 he joined Texas Instruments and was engaged in the development of receivers, T/R modules and system design.

In 1991 he joined the ITT Gallium Arsenide Technology Center and currently is leading the commercial design and development for wireless telecommunications.