The Operation of Low-Order RF Frequency Multipliers

A review of various doubler and tripler circuits with notes on narrow-band and wideband designs

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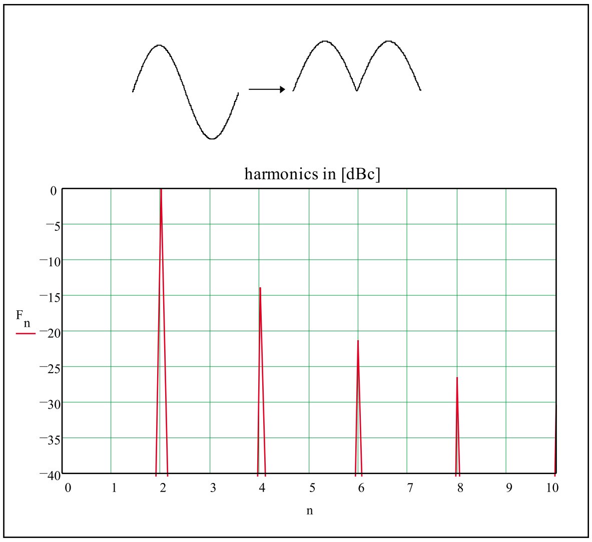
The most common frequency multiplying practice can be easily described. Simply use any nonlinear device, such as a diode or a slightly biased transistor, tune the input selective circuit for the input frequency and the output high-Q circuit to the desired harmonic, and supply a sufficiently high input signal. You can expect the desired output, even though it is usually pretty rich in undesirable and even unexpected contents. Experimental work is greatly encouraged, if not necessary, with such an approach. Rather than offer advice or describe that technique here, I will try to show why different approaches should be sought.

In handbooks, frequency multiplying is often described as an inherently narrow-band process, bound with selective circuits. I will try to prove throughout this paper that this description is neither general nor obvious.

As the title indicates, only low-order multipliers are discussed within the scope of the paper, indicating multiplication factors lower than 5, with special attention given to 2nd and 3rd order basic multipliers. Other multiplication factors can be accomplished as simple extensions of these basic approaches or by cascading them. When higher harmonics are needed, the Step Recovery Diode (SRD) technique should be considered, which, along with complex PLL or DDS methods, is beyond the scope here.

I am going to look critically at the common frequency multiplying practice. Many of what I think to be its best examples are in amateur radio schematics. Let us imagine a chain of two or three transistor multipliers, each a stage of the same topology. The emitters are directly at ground and the bases are grounded for DC with selective harmonic coupling between the stages.



▲ **Figure 1. Illustration of frequency doubling by wave-shaping with spectrum analysis results (DC component neglected).**

So simple, and yet it really does work! But how does it work?

First of all, it is known that such circuits are designed mostly from experimental work, without any analysis which, if involved, would require sophisticated software, tedious modeling of active elements and, after all that, could still give inaccurate results. Such differences between practice and theory are discouraged. These circuits include many tuned components, which require very careful adjustment. Circuit sensitivity to any variations may be troublesome. No wonder that it may not work with transistors from another lot or vendor.

Reliable and predictable behavior of any multistage chain requires that each stage is described separately, so the overall characteristic can be well-determined by composing the individual ones. Such a criterion is hardly met by the mentioned approach. In fact, when the particular multipliers are measured separately (usually in a 50 ohm system) and then connected to a chain, serious problems can arise. To "quiet" their instabilities, one can insert an attenuator of about 3 dB between the stages, yet this will badly affect the efficiency of the circuit, its cardinal advantage. It may also be expected that such a multiplier chain is significantly susceptible to the input signal level and does not ensure steady output power. Temperature dependence creates another critical constraint.

Now it is already possible to define the opposite approach, the one I am seeking, by simply inverting what has been given above. It should satisfy professional applications. There should be no wide expanse between theory and practice. Its analysis ought to be straightforward, without the need for experimental trimming. It would be desirable to eliminate any tuning elements if possible. Component tolerances cannot affect the overall circuit behavior. Connecting the multiplier stages should give the prescribed effect without any tuning. There should not be any significant power level instability or temperature dependence.

That is quite an ideal goal. Let us approach it regarding frequency doublers and triplers.

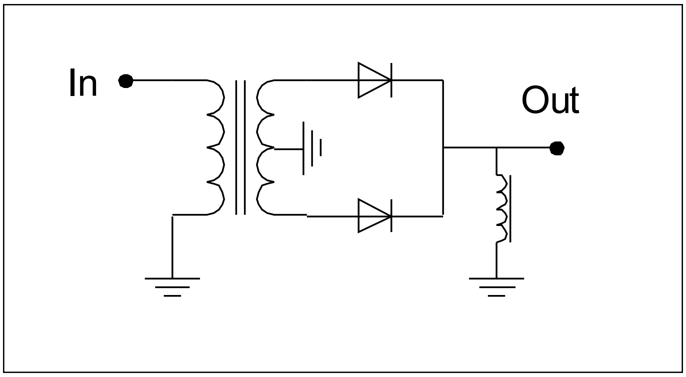
Frequency doublers

When looking for a frequency multiplier and preparing a review on the subject, one should do so in a consequent manner. I think the manner in which the input sinewave is treated may serve as a criterion here, beginning with any ideal processing with analog function operators, through wave-shaping with switching elements, down to "brutal" harmonics produced with highly nonlinear devices. In other words, one should consider the most to the least subtle wave processing.

Looking for an analytic description for frequency doubling, one can quickly find it in trigonometry. Describing the needed waveform with a common notation as $\sin 2a$, where $a = \omega t$, a simple equation can be written:

$$\sin a \times \cos a = \frac{1}{2} \times \sin 2a \qquad (1)$$

Translated into physical meaning, the expression states that two sinusoids with 90 degree phase shift delivered to an analog voltage multiplier produce a sinewave of doubled frequency. If the phase shift was any different, some DC voltage would also appear at the output. There are many integrated circuits accomplishing analog voltage multiplier functions, capable of operation up to hundreds of MHz. Yet, they can hardly operate as frequency doublers at RF frequencies. The main criterion needed to consider when applying them as frequency doublers is the undesired harmonics level, that is F1, F3 and F4, in reference to the desired F2 harmonic. Taking –30 dBc as a reasonable value, one may expect such a result to be lower than tens of MHz and –40dBc still below single MHz. It is also sensitive to the input signal level. The fact that these devices are rather complicated active circuits, with supply required, may also be considered drawback, whereas there are passive, wideband and practical doublers working on a different basis. Here, they serve as an example of the second group, or wave-shaping multipliers.



▲ **Figure 2. Basic wide-band frequency doubling circuit.**

Looking at a sinewave, it is not difficult to guess how to process it, so as to obtain a shape close to the double frequency sinewave in the easiest way. One must simply cut and invert the negative halves of the sinewave. Note that the process can be described mathematically as $|\sin a|$, the absolute value of $\sin a$. The wave-shaping approach is bound with the spectrum analysis of derived shapes by the Fourier transform, which can be accomplished by various software. Figure 1 shows the result for $|\sin a|$ obtained with use of Mathcad.

The figure indicates that the resultant wave has no odd harmonics, which is extremely advantageous. It means that the nearest unwanted harmonics, F1 (the input one) and F3, are theoretically canceled and the nearest undesired harmonic is F4 (at pretty low level, –14 dB below F2).

One can easily identify the topology for the above wave-shaping process: the full-wave rectifier (see Figure 2).

The application related difference is that when rectifying, the DC component is desired and AC shorted by a capacitor. Here, inversely, DC is shorted by a choke, enabling diode self-bias, and the AC component of $2 \times f_{in}$ frequency is delivered to the load.

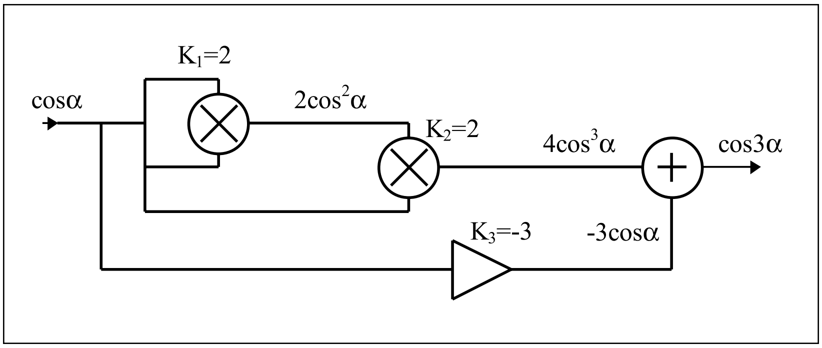
Such circuits implemented as RF doublers employ transmission line transformers and Schottky diodes which can be considered, with the first approximation, as ideal switches. Figure 1 indicates that the output wave is twice as low in voltage, which gives –6 dB initial loss. But any physical wave can not have as sharp edges as those at the bottom. Real diodes have some bias voltage, as well as series resistance. Including some mismatch and transformer loss, the typical loss of this structure is –10 dB. As these real diode properties cause some "rounding" of the wave at the bottom, it may be a good idea to lower the second harmonic of the resulting signal to below –20 dBc. Real values of F1 and F3 levels of –40 dB below F2 are readily available, depending on the circuit symmetry.

Frequency doublers of this type available on the market usually have a more complicated structure than that shown in Figure 2, resembling that of the double balanced mixer, with two transformers and a diode ring. The difference is in the direction of the diodes (one pair opposite to the other) and the transformer winding with only one input and output. These devices can be as wideband as the similar mixers, with an input frequency range of 50 MHz to 1.5 GHz, for example. The typical input power range is 10 to 20 dBm. One may notice that the double balanced mixers can also be implemented as frequency doublers, yet it is a significantly less efficient and more troublesome solution.

I mentioned at the beginning that frequency multipliers should not be regarded as inherently narrowband devices. Despite some limitations, both approaches mentioned thus far are essentially wideband. The first is in the MHz region and the second through microwaves. Yet, it should be noted that, when cascading several doublers of the second type, sharp filtering may be needed, especially in the first and second stage. This is because any spurious will increase, like phase noise, by 20logN (in this case, 6 dB per stage) with its offset from the carrier not changed. So the F1 and F3 spurs from the first stage may increase excessively after all the cascaded stages if they are not filtered out, and their filtering is most effective in the first two stages.

The truly narrowband circuits can be marked out by the harmonics redistribution approach. This technique relies on the production of intensive harmonics with a highly nonlinear device and the filtration of the the desired one. Extending the kitchen terminology, one could say that as the previous approach used "cutting" the wave, now it will be "chopping." With this approach, varactor diodes are used, especially at microwaves and higher. They are biased to avoid the conduction region, and with idle circuits implemented for unused harmonics, which do not absorb energy themselves but allow the effective recovery of the unwanted harmonics' energy, directing it into the wanted one. This makes high efficiency possible (above 80 percent), by the process of harmonics energy redistribution. Yet, high efficiency may turn out not so advantageous regarding all the drawbacks discussed at the beginning of the article. Making a cascade of such doublers would require attenuators or buffer amplifiers for its reliable work, thus canceling the gain in efficiency compared to the second type of doublers. After all, such multipliers can potentially behave in a hazardous manner, showing instability in noise amplification.

The prior approach is the most recommended, as opposed to the third method, which should be restrained to special cases (e.g. high power circuits or very high frequencies).



▲ **Figure 3. An "ideal" frequency tripler.**

Frequency triplers

For this task, as in the previous section, the same three approaches will be taken. The first, wave processing, is the most gentle method. Applying "kitchen" terminology it may be called "mixing" the wave. The second (medium) process could be described "cutting," while the third can be described as "chopping."

So at first, let us look for any analog function realization. Similar to the doubling case, the needed function can be found among trigonometry equations, that is:

$$4 \times \cos^3 a - 3\cos a = \cos 3a \qquad (2)$$

A modular schematic of a frequency multiplier based on this formula (employing two analog voltage multipliers, inverting amplifier and an adder) is presented in Figure 3.

Such a circuit can be built with only two integrated circuits, each including an analog multiplier with amplifier functions. Yet, an unsuspecting designer can encounter discouraging results. Even restrained to the region of several MHz, it is difficult to get a reasonable level of undesired harmonics. Any DC balance difficulties, as well as delays and phase shifts, are disturbing factors. But what is most important is the sensitivity to the input signal level. In fact, examining Figure 3, one may notice that the circuit will work properly only at one input voltage value, as when it changes, the wave coefficients at the adder inputs will also change.

It is worth noticing that the idea illustrated in Figure

3 can be accomplished even without any voltage multiplier, but with the use of a wave-shaping process instead. This means that the $\cos^3 a$ function can be well approximated by what is received after putting the sinewave through an anti-parallel diode pair (Figure 4a), which will be shown later in the article. With such a simplification, the entire circuit can be built based on two operational amplifiers. Nevertheless, the input level of sensitivity remains the prevailing drawback, with so small a change as ±0.2 dB significantly disturbing circuit operation. Although several solutions for the problem can be proposed, it would be only practical to compose all the circuitry in a specialized integrated circuit. I have not composed such a circuit, but I hope to see one in a small SMD case, capable to operate at about 100 MHz, with undesired harmonics below –40 dBc.

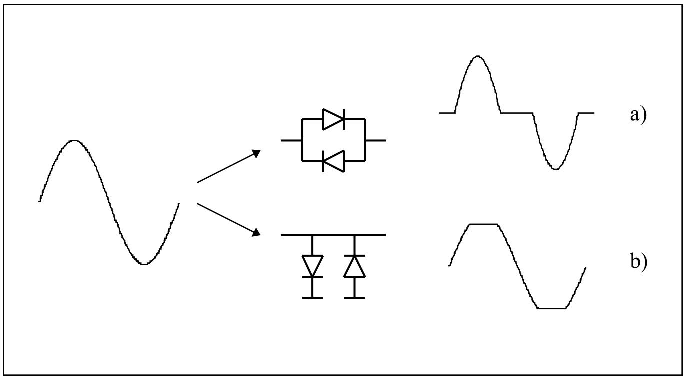
Despite any practical difficulties, I would like to emphasize that analog function frequency multipliers are essentially broadband. The relevant functions for higher orders are readily obtainable. Moreover, higher order multipliers can be realized by cascading lower ones. So virtually any order multiplier could be made as a broadband one, theoretically, of course. And no one knows what future technology will make possible. Despite the level to which the today's practice limits the goal, at least one statement may be held true: one should not regard frequency multipliers as inherently narrowband devices.

Now, to show a practical frequency tripler, let us move to the next approach, the wave-shaping method. The needed shapes should not include even harmonics, with the odd ones set off. They should be obtainable in a simple and reliable process. Examining the spectrum of various shapes, a general criterion is evident: the cut wave must be symmetric. There are two simple ways for to achieve that symmetry: cutting the sinewave inside or outside. The illustration for each case with an anti-parallel diode pair is shown in Figure 4.

The first case is especially interesting, cutting out about 61 percent with the fifth harmonic significantly reduced, according to the spectrum analysis shown in Figure 5.

Note that the shape of Figure 4a, with slight smoothing on real diodes, can resemble the $\sin^3 a$ function, which, analyzed spectrally, presents only two harmonics: F1 and F3 at the –9.5 dB level. So, looking from the spectrum contents point of view, the process illustrated in Figure 3 is more understandable. With the sinewave in the third power, one only needs to cancel the base component to obtain the tripled wave alone.

The limitations on Figure 4 are not directly practical. They serve rather for general knowledge purposes here. The second one is even worse, yet its idea may be useful. Note that it forms something like a rectangular wave. It is worth remembering the spectrum of an ideal symmetric rectangular wave, shown in Figure 6.

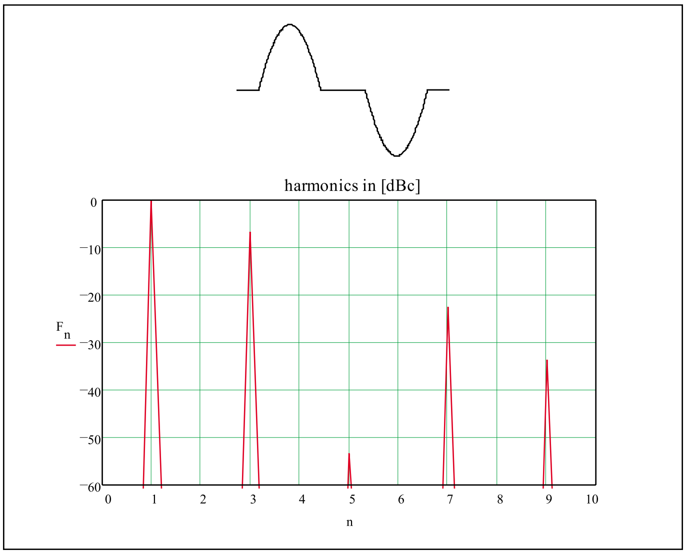


▲ **Figure 4. Two basic wave-shaping directions to create odd harmonics (the diodes are idealized as ideal switches with some forward voltage).**

In practice, it is not useful to derive the rectangular wave with diode limiters, but rather to magnify the wave to the full circuit supply voltage in active limiters. The task can be simply accomplished with the help of standard logic gates or flip-flops. Then by filtering the desired harmonic, an effective 3 (or 5) order multiplier can be obtained. This is the way to get the most efficient odd harmonics multipliers. First of all, the optimal logic family should be chosen, with the rectangularity of the output waveform as the main criterion. Two fast series, capable of operating beyond 100 MHz, are compared here: the FAST TTL Logic series and the Advanced CMOS Logic series, AC or ACT.

The ACT circuits, compatible with TTL, having low and well determined input threshold (~1.5V) may be even more suitable here, as input control by RF sinewave voltage can be accomplished more strictly than with a normal CMOS type.

Output waveforms from D flip-flops ('F74 and



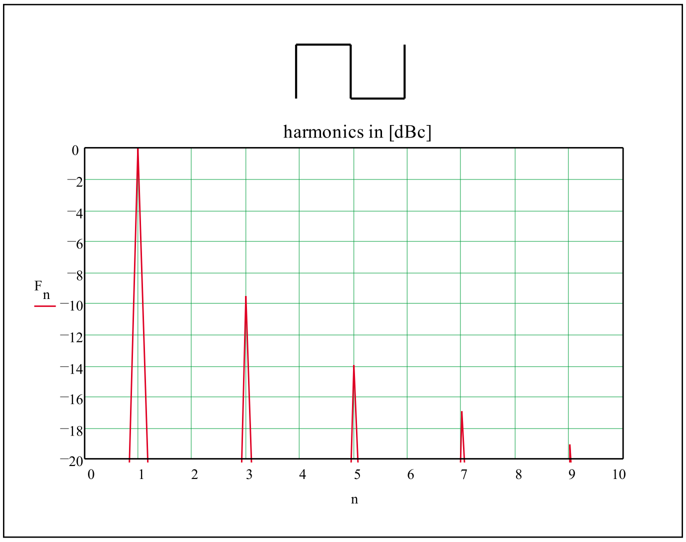
▲ **Figure 5. The spectrum for the shape from Figure 4a, with 61 percent cutting.**

'ACT74 types) were compared as they yield a wave of ideally one half duty cycle. The waveform from 'F74 is not very rectangular, which suggests a high level of even harmonics. They reach –25 dBc below the fundamental harmonic. Just the opposite, 'ACT74 gives nearly the ideal square wave, with spectrum close to that in Figure 6 and even harmonics as low as –50 dBc for fundamental frequencies of about 20 MHz. Other advantages of AC (ACT) series are its inherent wide operating temperature range and high output level, reaching supply voltage, which translates directly into obtainable harmonic power. Yet other CMOS logic series may be useful at lower frequencies, because of higher permissible supply voltage and therefore, higher possible output power when applied in a frequency multiplier configuration.

The most suitable situation for that kind of frequency tripling is when the wave to triple can be received from a divide-by-two stage. Such a divider, built on D or J-K flip-flops, can be simply steered by the original sinewave with help of a control amplifier giving high enough amplitude to drive the flip-flop safely. On the contrary, when the original sinewave is to be tripled directly, an ordinary logic gate such as 'ACT00 can be used to square the wave. Yet, in such a case, the triggering of the gate must be accomplished carefully, as the duty cycle of the output waveform (and the occurrence of undesired even harmonics) depends now on the AC and DC input levels. Thus, the gate should be driven with a rather high undistorted signal (~3 V_{pp}), with DC bias regulated to minimize the F2 and F4 harmonics at the output. Practically, the problem is not very serious, especially at higher frequencies, when the waveform produced is less ideal.

One more practical tip should be also emphasized. Digital integrated circuit chips include multiple flip-flops or gates, yet one should not employ more than one stage per chip because of internal crosstalk. For example, using an 'ACT163 4-bit synchronous counter as a divider from 80 MHz to 40 MHz one may observe plenty of harmonics in the output spectrum. With 5 MHz raster, they can be as high as –30 dBc below the fundamental, produced by the subsequent counter sections. Because no section in the 'ACT163 can be disabled then this type is unsuitable for the task. In case of an 'ACT74, with dual D flip-flops, one of them should always remain unused.

Now, assuming we have established an ideal generator of square wave voltage, let us check how it corresponds with practical results. Let it assume a 50 ohm standard filter, working into a 50 ohm load, is employed to filter out the third harmonic. How does one connect it to the source? It might seem justified to insert a 50 ohm resistance between such an assumed voltage source and the filter input to make a matched generator. Yet, we are not interested here in general matching properties, because now a particular filter is connected close to the signal output with the only demand to get the highest useful harmonic power in the load with the lowest amount of undesired harmonics. So after excluding that resistor, the output power increases a few dB and the undesired harmonics relative level decreases by the same amount, as the resistor practically does not influence undesired harmonics.



▲ **Figure 6. The spectrum of rectangular wave: F3 level of –9.5 dBc, F5 of –14 dBc.**

Accepting that we make a direct connection, one may ask why the square generator has to work with a 50 ohm filter instead of 5 or 500 ohm filter, for example. Although we typically require a 50 ohm load, the filter could be created as a transforming one, say from 5 to 50 ohms, so it would give an effective 5 ohm load for the source at the desired harmonic. In practice, such a modification would increase output power a little, with significant spectrum worsening because of difficult loading for the digital output stage. In the opposite case, when a 500 ohm to 50 ohm transforming filter is connected, then power transfer is far from optimum. So, working with 50 ohms is near the optimum conditions and as a standard, it enables simple analysis, measurement and choice of filters.

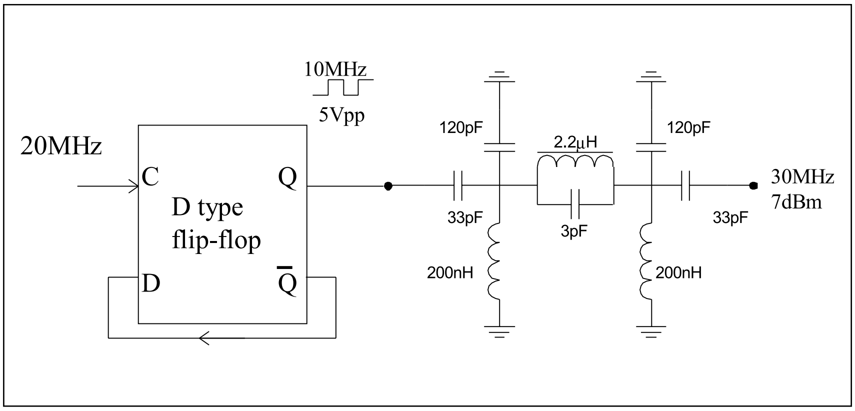
Now, let us try to determine the third harmonic power accessible after the multiplier filter. The theoretical formula for a square wave, corresponding to the spectrum of Figure 6, can be noted as a series:

$$f(a) = \sin a + \frac{1}{3}\sin 3a + \frac{1}{5}\sin 5a \ldots \qquad (3)$$

The square wave amplitude determined from this formula is related to the fundamental sine amplitude as 0.78 to 1. In our case, with a 5 volt logic ACT series, we obtain a 5 volt peak-to-peak square wave quite precisely, so its amplitude amounts to 2.5 volts. The fundamental sinewave is 2.5 volts/0.78 = 3.2 volts. The above equation indicates the third harmonic as 3 times lower, so it will be 1.07 volts. This amplitude delivered to a 50 ohm load would give power of 10.6 dBm. In practice, with filters of about 2 dB loss, one can reach about 7 dBm, so the real output stage influence is below 2 dB.

The CMOS output circuit consists of a MOS FET complementary push-pull pair. For output voltages closer than 1 volt to "1" or "0" states, the output stage behaves like the MOS FET r_{ON} resistance connected to UDD or ground respectively. For intermediate output voltages, the circuit output behaves more like a current source rather than a resistance. For AC (ACT) the r_{ON} values are about 10 ohms, so one could try to optimize the described application by inserting a matching resistor <40 ohms between the digital output and the 50 ohm filter. However, abandoning it prompts the best results.

To illustrate the overall spectrum prediction, a complete example with a simple, real filter is given in Figure 7, while Table 1 presents: a) the output square waveform spectrum without filtering, with the 'ACT74 working into a 510 ohm/51 ohm divider, b) filter characteristics, and c) the resultant, filtered output spectrum.



▲ **Figure 7. The frequency tripler 10 to 30 MHz example, with the ideal, input 10 MHz square-wave generated by a 74ACT74 implemented as a divide-by-two.**

	Harmonics F1	F2	F3	F4	F5
a - square-wave spectrum [dBc]	0	-47	-9	-52	-14
b - filter characteristic[dB]	-63	-38	-2	-32	-47
c - output spectrum[dBc]	-59	-75	0	-78	-56

▲ **Table 1. Measured values for the example in Figure 7: a) output square-wave spectrum without filtering, normalized to fundamental 10 MHz, b) filter characteristic, c) resultant output spectrum normalized to filtered 30 MHz harmonic.**

The 3 pF capacitor in the filter in Figure 7 serves to increase attenuation above the passband, about 10 dB at F5, yet such a tip may sometimes be improper, as it may increase the spurs at UHF to –40 dBc and more.

The example is to illustrate that the tripler output spectrum can be directly calculated simply by composing the square wave spectrum with the filter characteristic and therefore normalizing the result to the dominant harmonic. More strictly, that would be the case if the matching resistor were inserted between the IC and the filter to give the nominal source impedance. Without it, the circuit output is up to 6 dB higher power and the undesired harmonics' relative levels are lower by the same amount.

Although it is really a low frequency example, the properties are similar when going higher, with a little worse characteristic at twice higher frequencies. At four times higher, the most noticeable difference is with the F2 and F4 harmonics, reaching –50 dBc. Measurements of the third harmonics throughout 30 to 120 MHz region indicate a significant impact of the circuit layout when reaching the highest frequencies, especially the feedback connection making the D flip-flop a divide-by-2.

With basic logic gates, the working range may be moved even higher, with 100 to 300 MHz triplers quite practical, although the symmetric wave is not inherently obtained. The ACT logic series is not the fastest one. It could be possible to expand such circuits to much higher frequencies with ECL logic. Yet ECL's lower voltage levels limit the efficiency dramatically. Nevertheless, it seems to be possible to move the method higher with any other squaring circuits.

The approach described above seems to sufficiently fulfill the requirements for a robust frequency multiplier as drawn out at the beginning. No tedious analysis is needed and simple calculations give results close to measurements. No experimental trimming is required either. In fact, such a circuit may be regarded as non-tuned because the filter acts as a separate pre-tuned block or as inserted as a complete device. The circuitry is quite insensitive to component tolerances. Connecting the multiplier stages is relatively simple, producing expected results. The output power level stability is evident as the ACT series has inherently wide operating temperature range and the output power is related directly to the system supply.

So, again, as with frequency doublers, it seems to be reasonable to stop in the middle when going through the three multiplying approaches.

The third approach, termed here as the harmonic redistribution approach, was actually not intended to become very well-known. It seems to be simple and efficient, with the theoretical efficiency limit of 100 percent for the ideal varactor multiplier and practical values of about 70 percent readily available. The advantages may not be obvious in a demanding system, though. At RF frequencies, that approach employs slightly biased transistors rather than varactors, with a high input signal supplied, enabling some conversion gain. However, to obtain steady working conditions, one should not seek high gain.

Conclusions

The theory and practice of low order RF frequency multipliers have been researched in a critical glance. The common opinion on frequency multipliers as inherently narrowband devices has been contradicted with the description of a category of apparently wideband circuits. Thus, there are three generic approaches to the division of microwave frequency synthesis multiplying techniques:

- analog function multipliers;
- wave-shaping multipliers; and
- harmonics (energy) redistribution multipliers.

Stopping in the middle with the second approach has been suggested as the optimal choice. ■

Author information

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