Linear and EM Simulation Cuts Design Time of a 3.8 GHz Amplifier

CAD design tools are valuable aids in circuit design and validation

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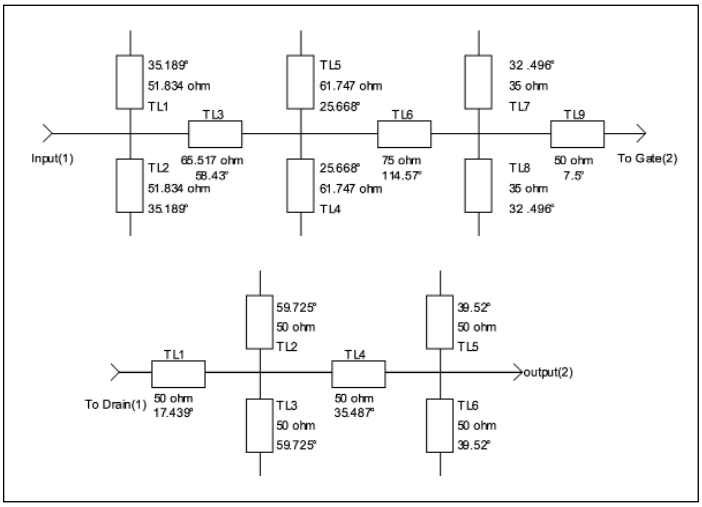
As the operating frequency goes beyond 3 GHz, the feasibility of lumped component matching networks diminishes due to component parasitics as well as tolerance in the component values. An alternative is to use distributed matching networks. However, this leads to another obstacle: discontinuities in these networks are not always modeled with sufficient accuracy in linear simulators.

To avoid the "garbage in, garbage out" pitfall, planar electromagnetic (EM) simulations of these networks are necessary. While most designers appreciate the utility of such a tool, many have limited or no access due to cost of the software. With the introduction of Sonnet Lite, a free planar EM simulator from Sonnet Software, any RF designer can now benefit from the accuracy of EM simulations. While there are limitations to this free program, there are also "tricks" to make it useful in "real" designs [1].

Although accurate, EM simulations consume considerably more CPU time. Random changes to the circuit and re-simulation to optimize a circuit, as often used in linear circuit simulators, would be inefficient if applied to EM simulations. Here is where the speed and flexibility of a linear simulator such as the one included in the GENESYS 7 software from Eagleware can help out. By combining the capabilities of both simulators, the circuit has a much better chance of being right the first time. Using a 3.4 to 4.2 GHz amplifier design, this article will demonstrate how the two programs can be used together to produce such a circuit.

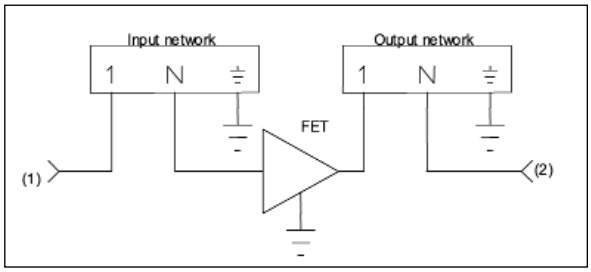


▲ **Figure 1. Synthesized matching networks from =MATCH=, with ideal transmission lines.**

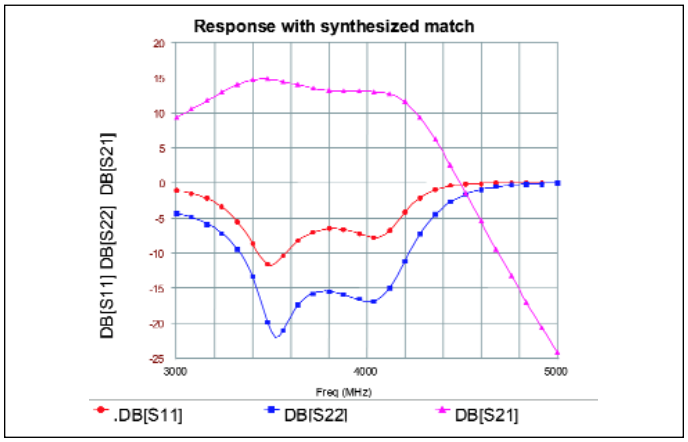
The basic performance requirements for the amplifier are:

- Frequency range: 3.4 to 4.2 GHz
- Gain: >12 dB
- Output Return Loss: < –15 dB

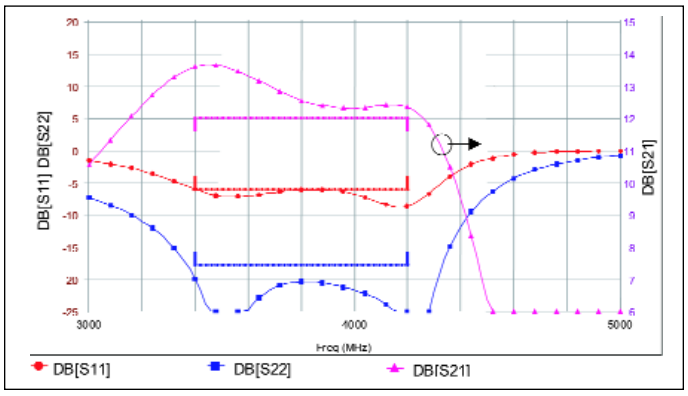
Once the active device has been selected, the



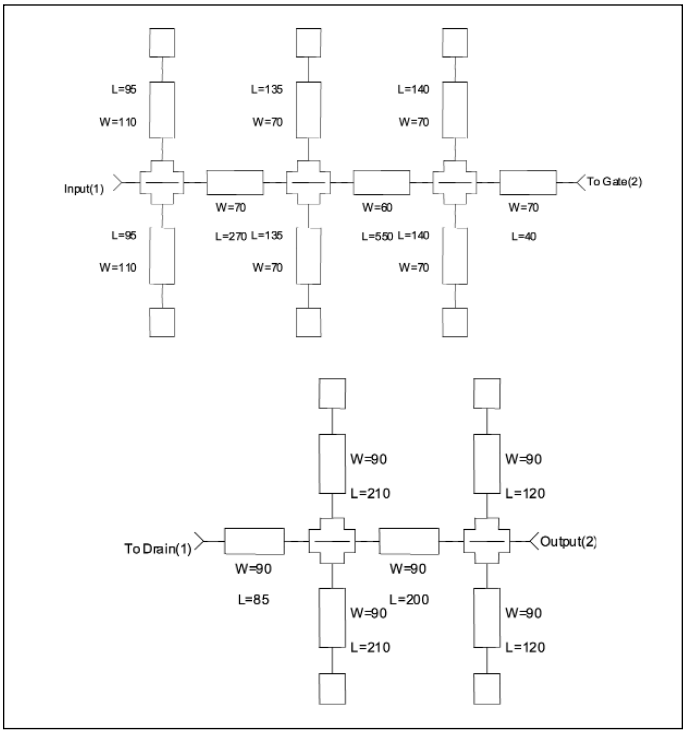
▲ **Figure 2. PA block diagram.**



▲ **Figure 3. PA response with synthesized matching networks from =MATCH=.**



▲ **Figure 5. PA response with microstrip elements as optimized in GENESYS 7.**



▲ **Figure 4. Matching networks as optimized by GENESYS 7 to include microstrip discontinuities.**

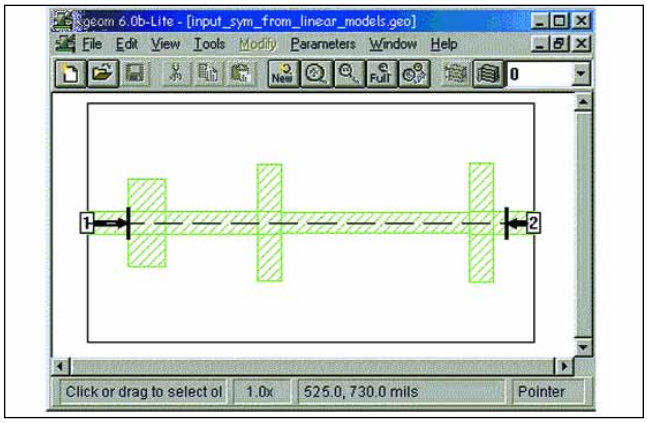
S-parameters will be used to generate the termination impedance for a "simultaneous conjugate match." This, in turn, is used in a synthesis program such as =MATCH= to generate a matching network.

Obtaining accurate *S*-parameters for the active device before starting the matching synthesis is very important. This means measuring the device even if there is published data. This will save time and frustration.

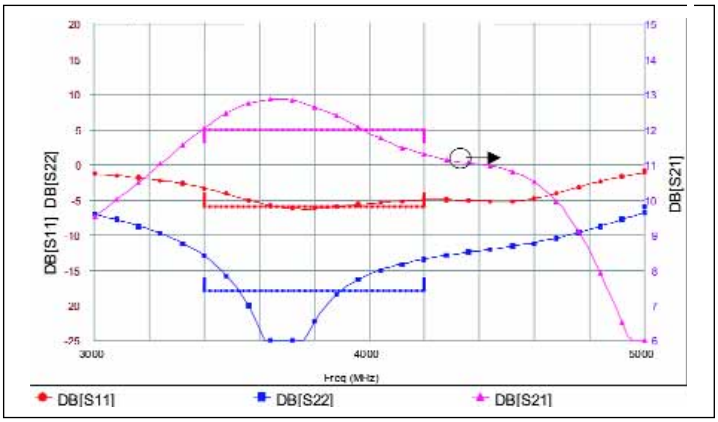
To move one step closer to a "real" circuit, the synthesized networks are transferred to GENESYS 7.0's linear simulator, where microstrip discontinuities are included in the simulations. To conserve memory usage in Sonnet Lite, the matching networks are made symmetric about the x-axis [1], as shown in Figure 1. The circuit parameters are then optimized to meet the design goals.

Necessity of EM simulations

The matching networks from GENESYS 7 are



▲ **Figure 6. Input network in Sonnet Lite using dimensions generated by GENESYS 7.**



▲ **Figure 7. PA response with EM simulations of the matching networks optimized by GENESYS 7.**

	Starting Value (mils)	After optimization to match Sonnet results (mils)	Error (mils)	Corrected value for Sonnet (mils) Starting Value + Error
L1	140	98	42	182
L2	135	90	45	180
L3	95	53.5	41.5	137
Lout1	210	147	63	273
Lout2	120	70	50	170

▲ **Table 1. Summary of matching network stub lengths.**

reproduced in Sonnet Lite, and the EM simulation results from Sonnet Lite are used for comparison. A screen shot of Sonnet Lite showing the input matching network is shown in Figure 6. The assumption here is that the EM results will be representative of the "real" results if the circuits were built. The simulation results are shown in Figure 7. The responses are significantly different from the desired response of Figure 5.

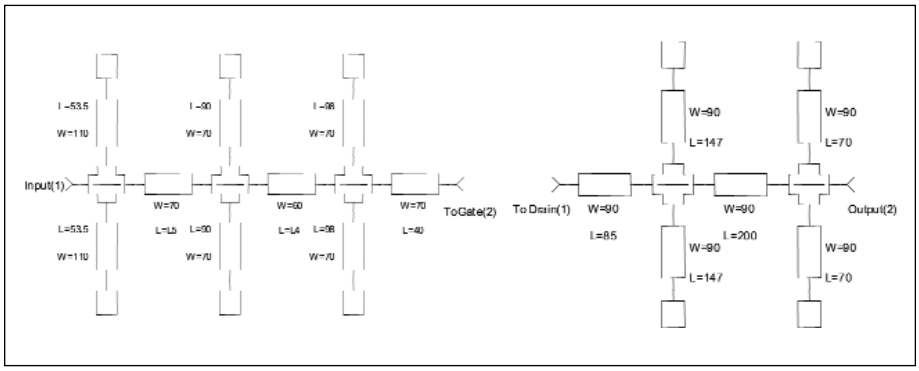
Circuit optimization

Figure 7 indicates that the matching networks need to be modified. To determine which element to change and by how much, we will first use the optimization feature of the linear circuit simulator (GENESYS 7, in this example) to modify the original networks to match the results of the first set of EM simulations. The differences in the dimensions are the "errors" and will be applied to the original circuit (generated by GENESYS 7). These new dimensions will then be incorporated into the Sonnet Lite simulations to check their effectiveness.

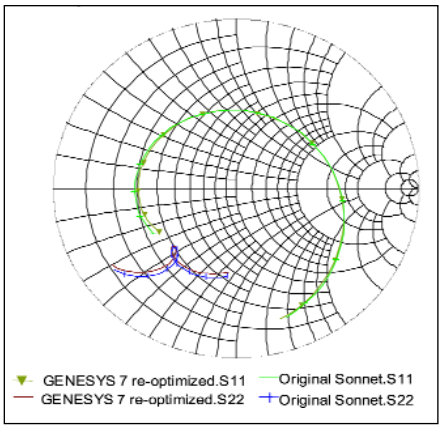
To keep things simple, only the lengths of the stubs will be varied in the optimization. If the results are not satisfactory, more parameters, such as line width and through-line length, can be made available to the optimizer. Figures 8 through 11 show the optimized dimensions and the resulting *S*-parameters. A summary of the stub lengths before and after "optimization" is given in Table 1. L1, L2, and L3 refer to the input network. Lout1 and Lout2 refer to the output network.

Even with relatively large correction factors (26 ~ 46%), the corrected dimensions from GENESYS 7 produced excellent results when re-simulated in Sonnet Lite. Using a 5-mil grid in Sonnet Lite, the dimensions in Table 1 are rounded off to the nearest increment.

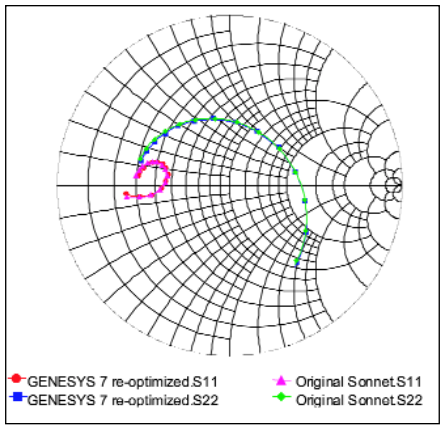
As shown in Figures 12 through 14, the corrected dimensions produced EM results that are quite close to the intended response. One final modification to the input network is needed before the design can be fabricated: the stubs closest to the FET gate need to be altered to clear the solder pad for the Source connection of the FET (SOT89). This is another situation where EM simulation is valuable, enabling arbitrary conductor shapes to be used when needed. The resulting layout is shown in Figure 16.



▲ **Figure 8. Matching networks "optimized" to match results from Sonnet Lite.**



▲ **Figure 9. *S*-parameters of the input network.**

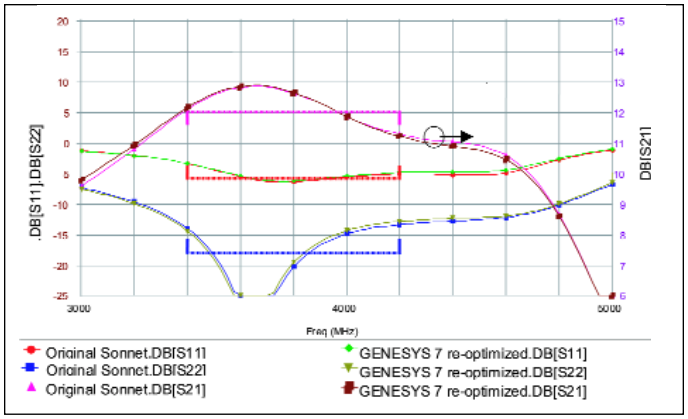


▲ **Figure 10. *S*-parameters of the output network.**

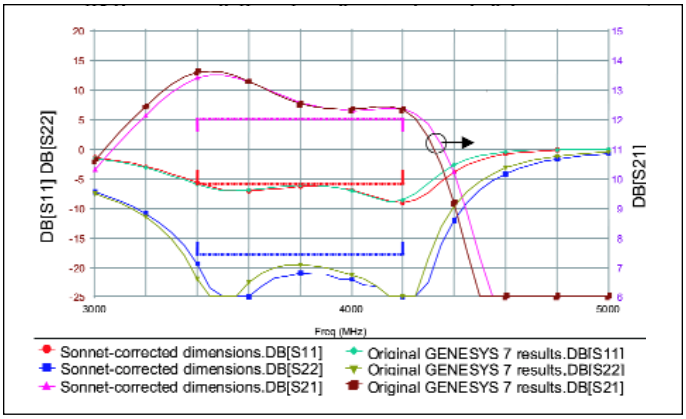
Measurements vs. simulations

The final test of any simulation is, of course, actual results from a real circuit. Figures 17 through 19 compare the simulation results with the network analyzer measurements.

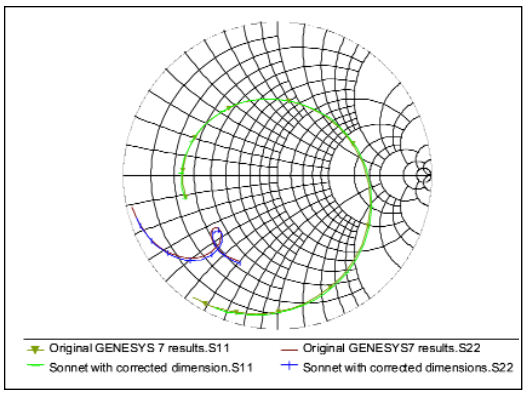
The measured results correlate well with the simulations. The frequency shift in the passband is related to the slight differences in the test jig that was used to measure the *S*-



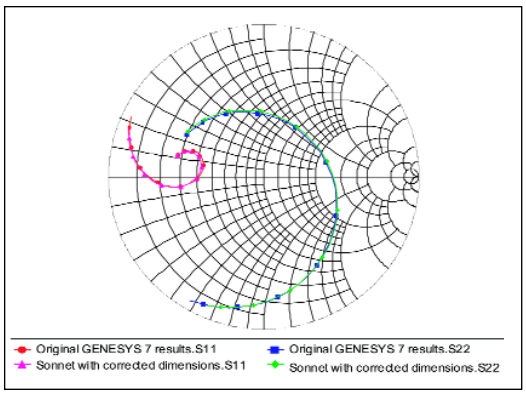
▲ **Figure 11. PA response with microstrip networks tuned to match Sonnet Lite results.**



▲ **Figure 14. PA response with Sonnet results using "corrected" dimensions.**



▲ **Figure 12. Sonnet results for input network with corrected dimensions.**



▲ **Figure 13. Sonnet results for output network with corrected dimensions.**

Practical design considerations

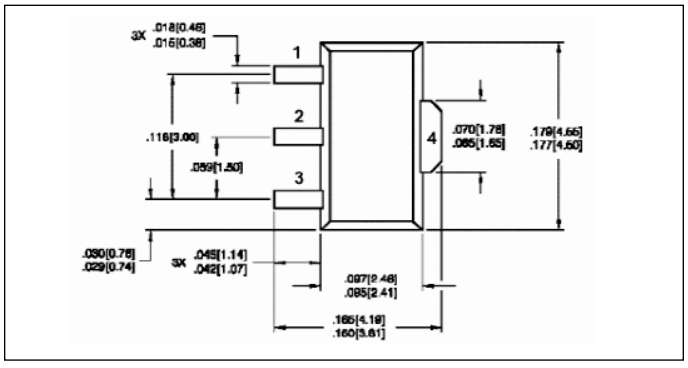
This article has thus far bypassed the biasing networks that would be needed to complete the design (the above results were obtained using the bias tees of the network analyzer). Now that the main concepts and results have been presented, some comments on the topic are appropriate.

Due to the moderate bandwidth requirement (~20%), $\lambda/4$ high impedance transmission lines or self-resonant chip inductors can be used to provide a DC bias path. The RF "short" at the end of the transmission line or inductor can be a chip capacitor that is at or near its series self-resonance. The effect of the bias networks on the overall circuit can be simulated by attaching it to the existing input and output ports of the PA.

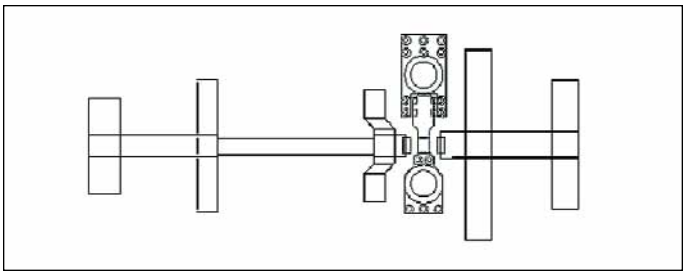
Another practical issue that arose for the above example is the length of the input matching network. To conserve space, the long section of transmission line can be folded into a "U," as shown in Figure 21. By

parameters of the FET and the actual layout of the PA. When the PCB for the PA was made, a new test jig was added that would mimic the grounding scheme of the actual layout (see Figure 16). With the new test jig, the *S*-parameters were re-measured. The results are shown in Figure 20.

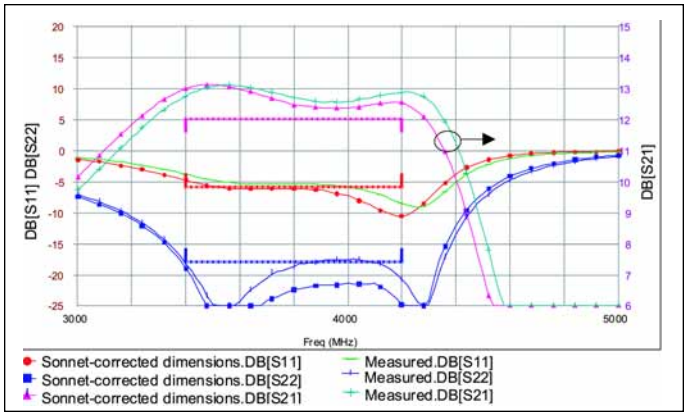
Besides showing improved correlation between simulation and measurements, the results in Figure 20 also illustrate the importance of accurate device S-parameters.



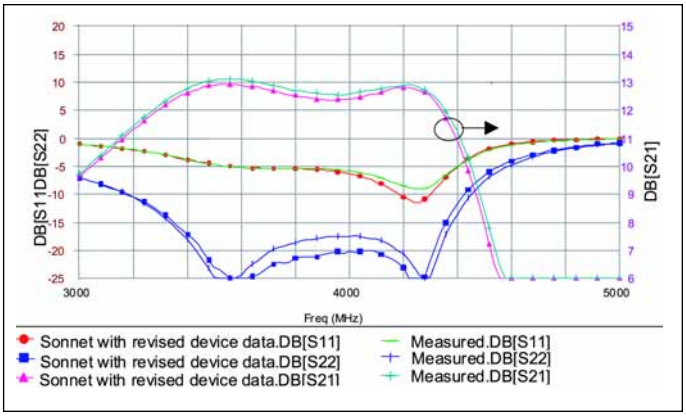
▲ **Figure 15. SOT89 package outline.**



▲ **Figure 16. Layout for PA with input network modified to clear the ground tab of the FET.**

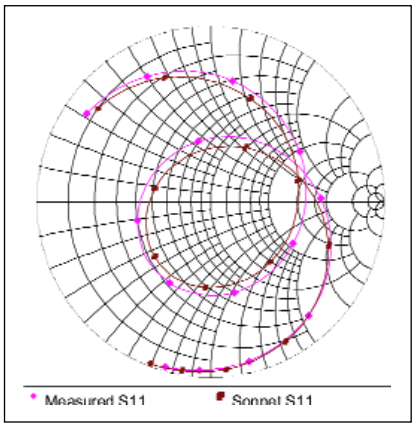


▲ **Figure 17. Measured results vs. simulation.**

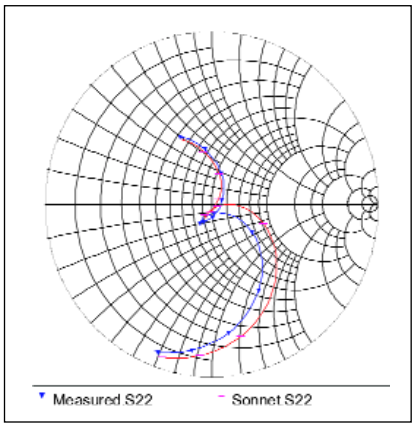


▲ **Figure 20. Measured results vs. simulation with revised *S*-parameters for the FET.**

introducing four bends, the dimensions of that section of transmission line need to be modified. Once the dimensions of the "U" have been optimized to match the results of the straight piece, the new network can be re-simulated. Instead of simulating the entire network, which would exceed the memory limit of Sonnet Lite, the network will need to be cut into three sections and their results recombined to get the overall response. A more detailed example of this partitioning trick is presented in [1].



▲ **Figure 18. Measured results vs. simulation: PA S_{11}.**



▲ **Figure 19. Measured results vs. simulation: PA S_{22}.**

PCB variations

PCB parameters such as dielectric constant, board thickness and etching variations can have a significant effect on circuit performance. Through Monte Carlo simulations, the speed of the linear circuit simulator can provide some assurance that the design will be repeatable in production. Small (less than grid size) changes in conductor dimensions are not easily handled in Sonnet Lite, and even then it would be difficult to determine the worst-case scenario for the different parameters.

Conclusions

Fast and accurate simulations need not always be expensive. By combining the efficiency of the optimizer in GENESYS 7 with the enhanced accuracy of Sonnet Lite, a wide band 3.8 GHz amplifier was able to meet design objectives in a single pass with minimal number of EM simulations. ■

Acknowledgements

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References

1. James C. Rautio, "Tips and Tricks for Using Sonnet Lite — Free EM software will radically change the way you do high frequency design," *Microwave Product Digest,* November 1999, pp. 30–34, 67–70.

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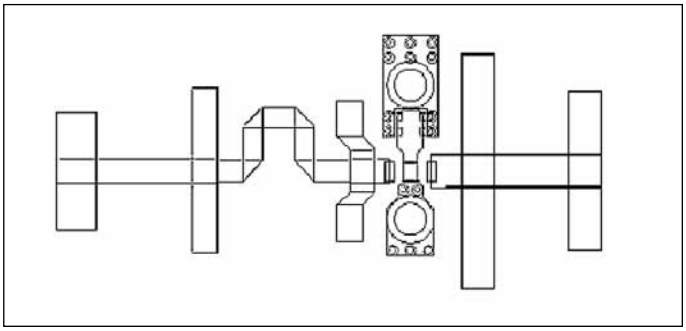

▲ **Figure 21. Input matching network with folded section.**