A VCO Design for WLAN Applications in the 2.4 to 2.5 GHz ISM Band

By Peter Shveshkeyev
Alpha Industries, Inc.

The increased demand for mobile network connections has lead to the establishment of RF interface standards for Wireless Local Area Networks (WLANs). The unlicensed ISM frequency band at 2.4 to 2.5 GHz has been designated for WLAN usage. Table 1 displays frequency allocations in different parts of the world for WLAN. In the US, IEEE 802.11 specifies two RF physical layer interfaces for WLAN, Direct Sequence Spread Spectrum (DSSS) and Frequency Hopped Spread Spectrum (FHSS).

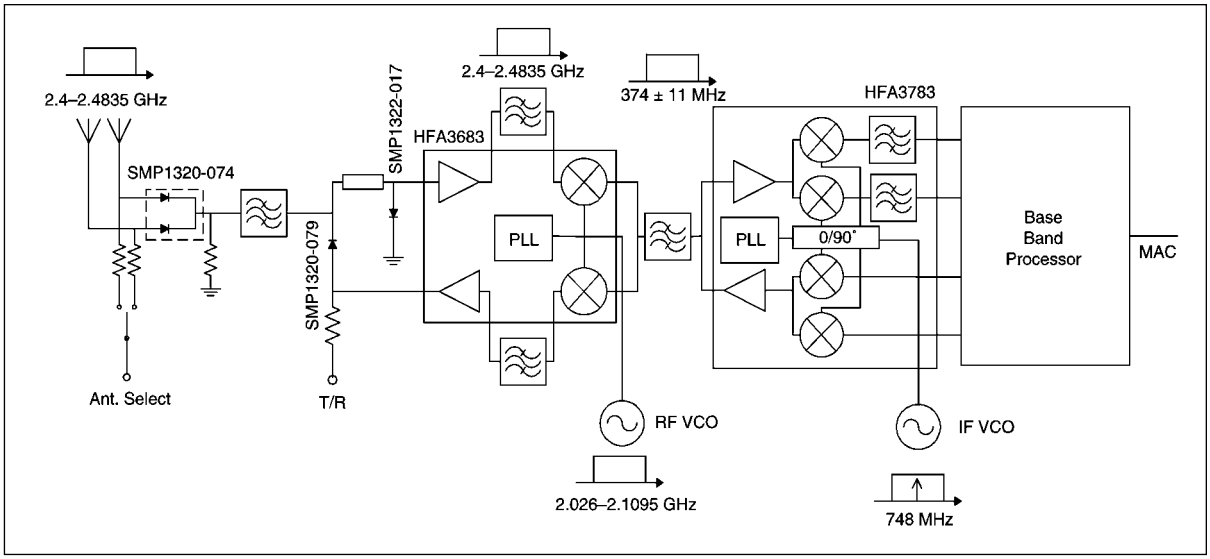
DSSS uses an 11-bit Barker code where each bit of information is spread within a single channel. The IEEE standard allocates 11 channels, each 22 MHz wide, with 5 MHz spacing between center frequencies in the 83.5 MHz band. This creates channels whose occupied frequencies overlap.

With FHSS, there are 75 channels, each 1 MHz wide. The transmitter and receiver follow a predetermined frequency-hopping sequence at least once every 400 ms. The frequency-hopping sequences have been arranged to spread the power evenly across the ISM band.

Region	Allocated Spectrum (GHz)
US, Europe	2.4–2.4835
Japan	2.471–2.497
France	2.4465–2.4835
Spain	2.445–2.475

▲ **Table 1. Global spectrum allocations for the 2.4 GHz band [1].**

In the typical DSSS interface architecture, shown in Figure 1, the RF signal passes through an antenna diversity switch (this switch may be



▲ **Figure 1. Typical WLAN RF interface architecture based on the Intersil Prism™ chip set [2].**

designed using Alpha's common cathode SMP1320-074 PIN diode). The signal passes through a bandpass filter and a T/R switch (this switch may be designed using Alpha's PIN diodes SMP1320-079 and SMP1322-0173). In the down/up converter IC, Intersil HFA3683, the RF signal is converted to an IF of 374 MHz. The IF signal enters a second down/up converter, Intersil HFA3783, and is further converted to/from the baseband IC input/output interface range. This architecture uses external VCOs for the RF and IF local oscillators. In the selected frequency plan, the RF VCO operational range is 2.06 to 2.1095 MHz and the IF VCO operates at 748 MHz fixed frequency.

This application note describes the design of RF and IF VCOs for a 2.4 to 2.4835 GHz WLAN application, based on the frequency plan described above. Although this design addresses a particular RF system outline, this example may be applied to most WLAN systems.

VCO specifications

In the frequency plan shown in Figure 1, the RF VCO frequency range is 2.026 to 2.1095 GHz. In reality, the tuning range of the specific VCO design should be stretched to accommodate conditions that would affect frequency. These factors include temperature variations, component value variations, aging, and humidity. Table 2 shows how the tuning range needs to be expanded to meet these conditions. We assume that the VCO has a +0.1%/10° C temperature sensitivity, which is typical for uncompensated RF VCO designs.

In this design, there is no frequency trimming allowed after mounting. Therefore, the tuning range will be extended to cover deviations resulting from component value variations. For inductors and capacitors with a ±5% tolerance the worst case of ±2.3% frequency variation may result. Including aging and other factors, a ±0.5% final tuning range will be from 1.969 to 2.184 GHz, or 215 MHz.

Similar considerations lead to an extension of the IF VCO range of 748 MHz ±3.2% (724–772 MHz), resulting in a 48 MHz tuning range.

The RF and IF VCO performance also depends on the characteristics of the specific RFIC chip-set used. Typical performance objectives for the RF and IF VCO are listed in Table 3.

Range Description	Margin %	Tuning Range (GHz) Min.	Max.
Operational		2.026	2.1095
Temperature (+15°C to + 85°C)	+0.7	2.026	2.1243
Component variations	±2.3	1.979	2.1732
Aging and other	±0.5	1.969	2.1841

▲ **Table 2. RF VCO tuning range margins.**

Parameter	Test Conditions	RF VCO	IF VCO
Frequency range (GHz)	VCTL		
	0.5 V	1.969	0.726
	2.5 V	2.184	0.770
Tuning sensitivity (MHz/V)		108	22
Supply voltage (V)		3	3
Supply current (mA)		15	10
Control voltage (V)	VCTL	0.5–2.5	0.5–2.5
Output power (dBm)	POUT	-3	-8
Pushing figure (MHz/V)		2	2
Pulling figure (MHz)	VSWR = 2	1	1
	For all phases		
Phase noise (dBc/Hz)	@ 10 kHz	-90	-90

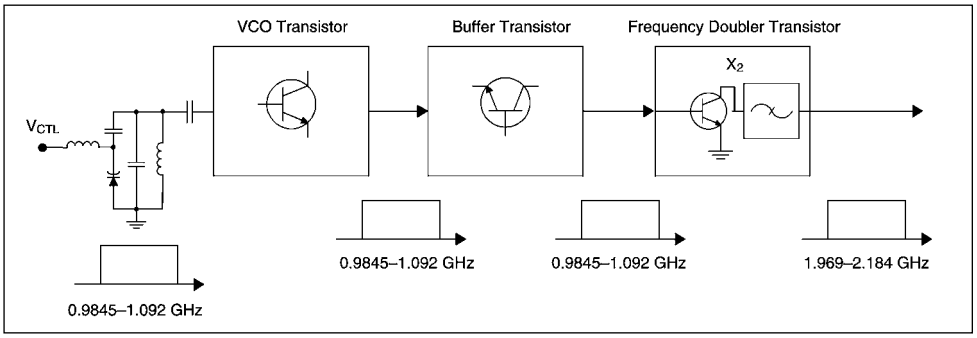
▲ **Table 3. Typical RF/IF VCO performance.**

VCO design considerations

An important consideration for the VCO and other RF components integrated on the same PCB is the ability to cover the frequency range with no trimming. Non-trimmed VCOs are particularly sensitive to variations of the component values and PCB material characteristics. In addition, VCOs operating at oscillation frequencies greater than 1 GHz are even more sensitive to these variations.

For this reason, this design employs a frequency-doubling scheme to achieve an RF VCO between 1.969 and 2.1841 GHz. The fundamental frequency of the RF VCO architecture in Figure 2 operates at 0.9845 to 1.092 GHz, half the output frequency. This signal is fed to a multiplier/buffer transistor, whose output circuit is tuned to the second harmonic, 1.969 to 2.184 GHz.

An important benefit of frequency doubling is its inherent high level of load isolation, reducing the VCO



▲ **Figure 2. RF VCO block diagram.**

buffer amplifier's complexity. However, the presence of the fundamental component in the output spectrum may require some filter circuitry at the multiplier output to prevent PLL counter errors.

The fundamental RF VCO was designed using traditional Colpitts circuit procedures. Similarly, the IF VCO is also a traditional design using a separate Colpitts VCO and buffer transistor, both operating in the same frequency range of 0.726 to 0.770 GHz.

Colpitts VCO fundamentals

The fundamental Colpitts VCO operation is illustrated in Figures 3a and 3b. Figure 3a shows a Colpitts VCO circuit the way it is usually implemented on a PCB. Figure 3b reconfigures the same circuit as a common-emitter amplifier with parallel feedback. The transistor junction and package capacitors, C_{EB}, C_{CB} and C_{CE}, are shown separated from the transistor parasitic components to demonstrate their direct effect on the VCO tank circuit.

In an actual low-noise VCO circuit, the capacitor we noted as C_{VAR} may have a more complicated structure. It would include series and parallel-connected discrete capacitors used to set the oscillation frequency and tuning sensitivity. The parallel resonator (or simply resonator) consists of the parallel connection of the resonator inductance, L_{RES}, and the varactor capacitive branch, C_{VAR}. A fundamental property of the parallel resonator in a Colpitts VCO is its inductive impedance at the oscillation frequency. This means that its parallel resonant frequency is always higher than the oscillation frequency.

At parallel resonance in the resonator branch, its impedance in the feedback loop is high, acting like a stop band filter. Thus, the closer the oscillation frequency to the parallel resonant frequency, the higher the loss introduced into the feedback path. However, since more reactive energy is stored in the parallel resonator closer to the resonant frequency, a higher Q-loaded (Q_L) will be achieved. Obviously, low-loss resonators, such as crystal or dielectric resonators, allow closer and lower loss oscillation buildup at parallel resonance in comparison to microstrip or discrete inductor-based resonators.

The proximity of the parallel resonance to the oscillation frequency may be effectively established by the C_{SER} capacitance value. Indeed, if the capacitance of the C_{SER} is reduced, the parallel resonator will have higher inductance to compensate for the increased capacitive reactance. This means that the oscillation frequency will move closer to parallel resonance resulting in higher Q_L and higher feedback loss.

The Leeson equation establishing connection between tank circuit Q_L and its losses states:

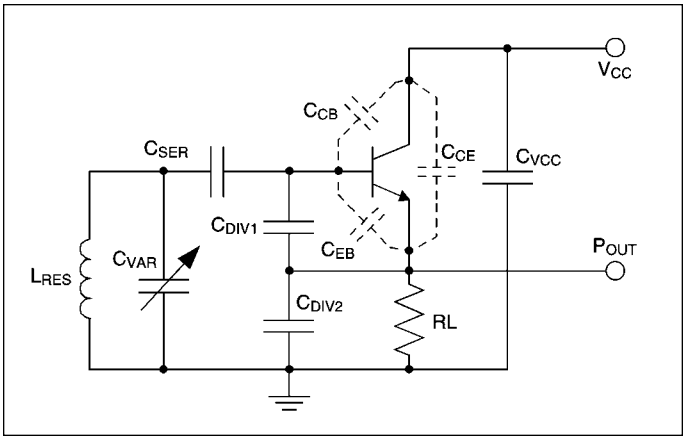
$$\xi(f_m) = \frac{FkT}{2P}\left(1 + \frac{f^2}{4Q_L^2 f_m^2}\right)$$

Where F is the large-signal noise figure of the amplifier, P is loop or feedback power (measured at the input of the transistor), and Q_L is loaded Q. These three parameters have significant consequence for phase noise in an actual low-noise RF VCO. In designing a low noise VCO, we need to define the condition for minimum F and maximum P and Q_L.

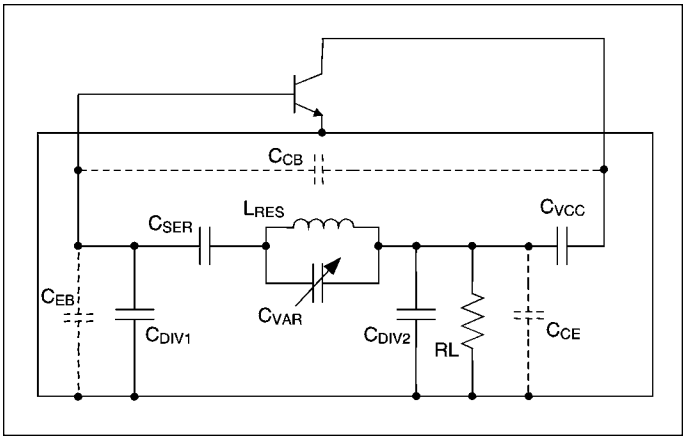
This discussion shows that loop power and Q_L are contradictory parameters. That is, an increase in Q_L leads to more loss in the feedback path resulting in lower loop power. The condition for optimum noise figure is also contrary to maximum loop power and largely depends on the specific transistor used. The best noise performance is usually achieved with a high gain transistor whose maximum gain coincides with minimum noise at large signals. Since there are no such specifications currently available for standard industry transistors, we can only base the choice of device on experience.

The RF VCO model

The RF VCO model is shown in Figures 4a and 4b. Some component values, defined as variables, are listed in the "Var_Eqn" column in Figure 4b. In the VCO resonator model, in Figure 4a, the SMV1763-079 varactor



▲ **Figure 3a. Basic Colpitts VCO configuration.**

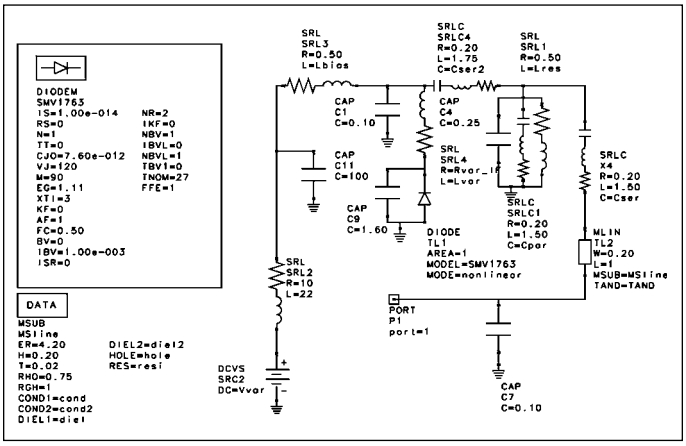


▲ **Figure 3b. Common emitter view of the Colpitts VCO.**

model is described as a resistor and inductor, SRL4, connected in series, and capacitor C_9 and diode SMV1763 are connected in parallel. The varactor choice was based on the VCO frequency coverage and the requirement for low phase noise. The resonator inductor, L_{RES}, is described as a series RL network SRL1 with parallel capacitor C_4. Parallel capacitor C_4 is modeled with its parasitic series inductance and resistance in the SRLC1 series network. Two series capacitors, C_{SER} and C_{SER2}, are also modeled as SRLC series networks, X_4 and XRLC4, respectively. Transmission line TL2 models the physical connection of the resonator with the base of the VCO transistor X_2 (Figure 4b).

In the RF VCO circuit model, shown in Figure 4b, transistors, X_2 and X_4, are connected in DC cascode sharing the base bias network consisting of R_4 (R_{DIV1}), R_1 (R_{DIV2}) and R_2. The bias resistor values were designed to evenly distribute the DC voltages between X_2 and X_4. The emitter bias resistor, RL1, was chosen at the low value of 100 ohms to minimize the DC voltage drop. The 60 nH inductance in series with RL1 in the network SRL1 enhances the RF-to-ground impedance at the emitter terminal. At RF frequencies, X_4 operates as a common-emitter amplifier with the emitter grounded through parallel capacitor network SRLC1–SRLC3. The efficiency of the circuit suppresses the fundamental component and enhances the second harmonic at the output of X_4 and is critical to the design of that network. The inductors L_3, L_2 and the parasitic inductances in SRLC1 and SRLC3 are crucial parts of the design.

The details of the SRLC1–SRLC3 network layout in the VCO design are shown in Figure 5. The circuit model values appearing in the model were optimized to fit the circuit's performance. Some inductors in the model look different from the layout and are attributed to the imperfection of the circuit component models.



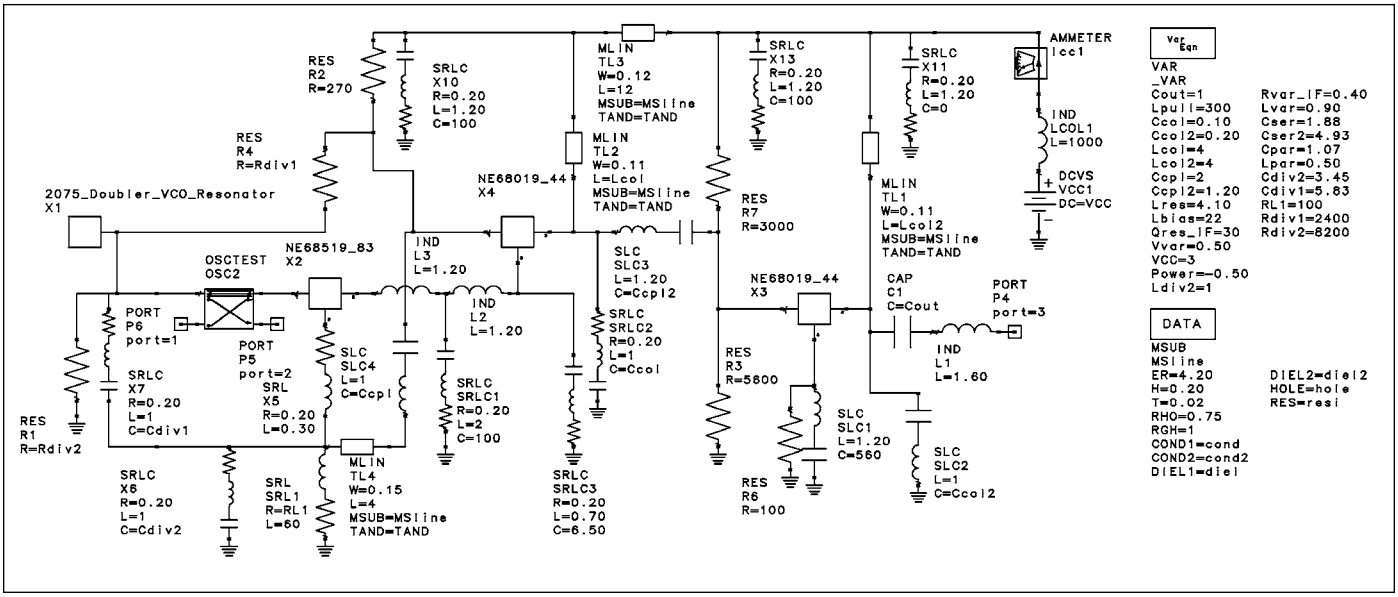
▲ **Figure 4a. The RF VCO resonator model.**

The output circuit of transistor, X_4, consists of transmission line TL2 and coupling capacitor SLC3. This output circuit is tuned to the second harmonic of the oscillation frequency. The buffer transistor X_3 operates at the second harmonic as an ordinary common-emitter amplifier with about 10 mA DC current for high gain.

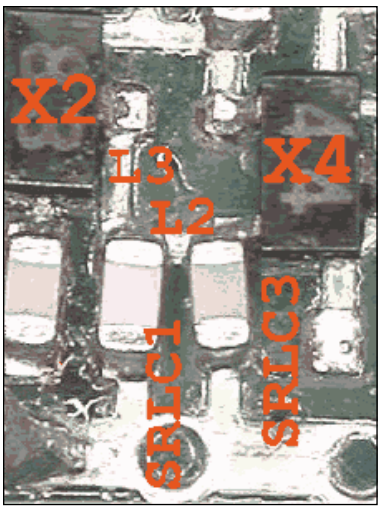
In the test bench in Figure 6 the loop gain Ku = V_{OUT}/V_{IN} is defined as the ratio of voltage phasors at the input and output ports of an OSCTEST component. Defining the oscillation point is a technique to balance the input (loop) power in order to provide zero gain for zero loop phase shift. Once the oscillation point is defined, the frequency and output power may be "measured." We do not recommend the use of the OSCTEST2 component for closed loop analysis, since it may not converge and does not allow clear insight to VCO behavior.

The IF VCO model

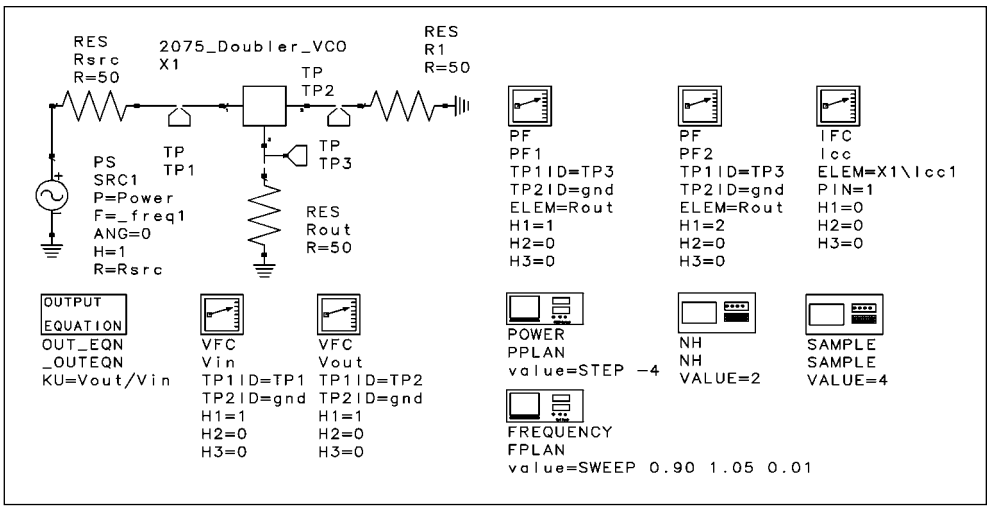
The IF VCO model is shown in Figures 7a and 7b.



▲ **Figure 4b. The RF VCO circuit model.**



▲ **Figure 5. SRLC1-SRLC3 network layout details.**

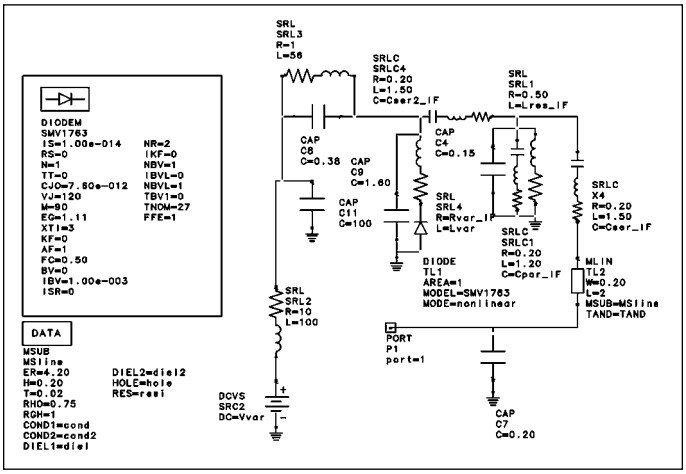


▲ **Figure 6. The RF VCO Test Bench for open loop oscillator analysis using the OSCTEST coupler from Libra IV library.**

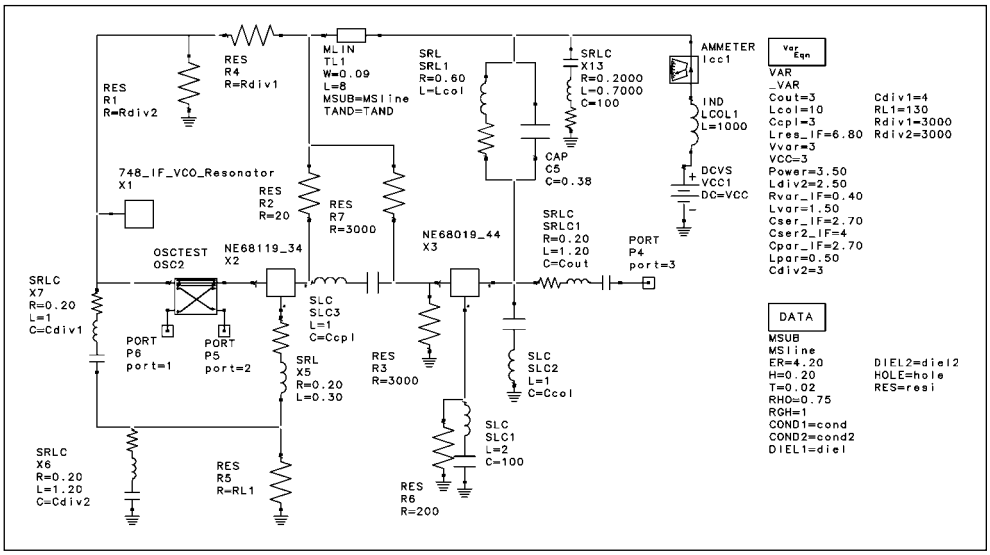
Some component values, defined as variables, are listed in the "Var_Eqn" column in Figure 7b. In the resonator model, Figure 7a, the SMV1763-079 varactor model is described with resistor and inductor, SRL4, connected in series, and capacitor C_9 and diode SMV1763 connected in parallel. For this narrow band application many varactors, abrupt and hyperabrupt, work well, however, the low resistance and the hyperabrupt characteristic of the SMV1763-079 helps improve tuning linearity and phase noise. The resonator inductor, L_{RES}, is described as a series RL network, SRL1, with parallel capacitor C_4. The parallel capacitor is modeled with its parasitic series inductance and resistance in the SRLC1 series network. Two series capacitors, C_{SER} and C_{SER2}, are also modeled as SRLC series networks, X_4 and XRLC4 respectively. Transmission line, TL2, models the physical connection of the resonator with the base of the VCO transistor, X_2, in Figure 7b.

In the IF VCO circuit model, in Figure 7b, transistors X_2 and X_4 are DC biased separately to independently optimize the performance of the VCO and buffer transistors. The emitter bias resistor, RL1, was chosen as low as 130 ohms to achieve current/performance balance in the VCO transistor. The overall current from the 3 VDC bias was set at approximately 10 mA, which is adequate to provide sufficient power with good phase noise performance.

The VCO output signal is fed from collector resistor R_2, shown in the base of common-



▲ **Figure 7a. IF VCO resonator model.**



▲ **Figure 7b. IF VCO circuit model.**

Parameter	Description	Unit	Default
IS	Saturation current (with N, determine the DC characteristics of the diode)	A	1e–14
R_S	Series resistance	W	0
N	Emission coefficient (with IS, determines the DC characteristics of the diode)	-	1
TT	Transit time	S	0
C_{JO}	Zero-bias junction capacitance (with V_J and M define nonlinear junction capacitance of the diode)	F	0
V_J	Junction potential (with V_J and M define nonlinear junction capacitance of the diode)	V	1
M	Grading coefficient (with V_J and M define nonlinear junction capacitance of the diode)	-	0.5
E_G	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E_G, helps define the dependence of IS on temperature)	-	3
KF	Flicker-noise coefficient	-	0
AF	Flicker-noise exponent	-	1
FC	Forward-bias depletion capacitance coefficient	-	0.5
B_V	Reverse breakdown voltage	V	Infinity
I_{BV}	Current at reverse breakdown voltage	A	1e–3
ISR	Recombination current parameter	A	0
NR	Emission coefficient for ISR	-	2
IKF	High-injection knee current	A	Infinity
NBV	Reverse breakdown ideality factor	-	1
I_{BVL}	Low level reverse breakdown knee current	A	0
NBVL	Low level reverse breakdown ideality factor	-	1
T_{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker-noise frequency exponent	-	1

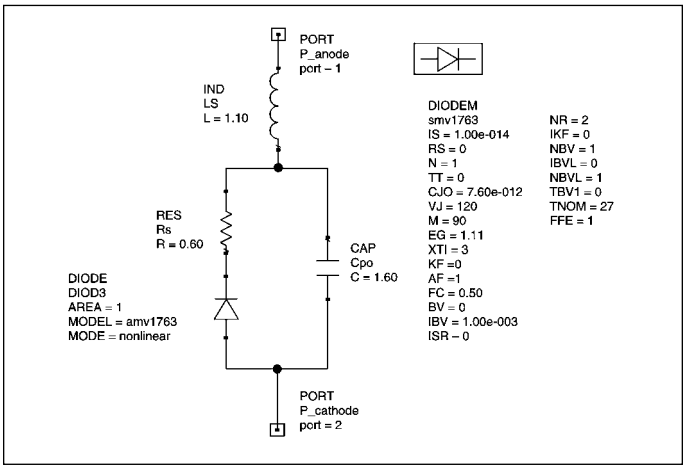
▲ **Table 4. Silicon diode default values in Libra IV.**

C_{JO} (pF)	M	V_J (V)	C_p (pF)	R_S (Ω)	L_S (nH)
7.6	90	120	1.6	0.6	1.1

▲ **Table 5. SPICE parameters for SMV1763-079.**

emitter amplifier buffer stage X_3. The output circuit of the buffer stage consists of parallel-connected inductor, SRL1, capacitor, SLC2, and coupling capacitor, SRLC1. The collector inductance is modeled as a lossy inductance with 0.6 ohm series resistance in parallel with parasitic capacitor, C_5.

Transmission line, TL1, is an essential contributor to VCO performance, as a part of the load/tank circuitry. Referring to Figure 3b, R_L (the VCO active load) shown as R_2 in Figure 7b, could be could be interpreted as



▲ **Figure 8. SMV1763-079 SPICE model for Libra IV.**

series impedance between the collector of the VCO transistor and capacitor C_{VCC}. Transmission line, TL1, in Figure 7b, may be considered an inductor in series with that load. The buffer input circuit then becomes parallel to both R_2 and TL1 (in Figure 7b). The effective inductance of TL1 improves the input match of the buffer stage and increases the output power level; however, this will also increase the load on the VCO feedback power, which may lead to phase noise degradation.

The test bench was identical to Figure 6 (RF VCO), which was defined for open loop analysis with the OSCTEST component above.

SMV1763-079 SPICE model

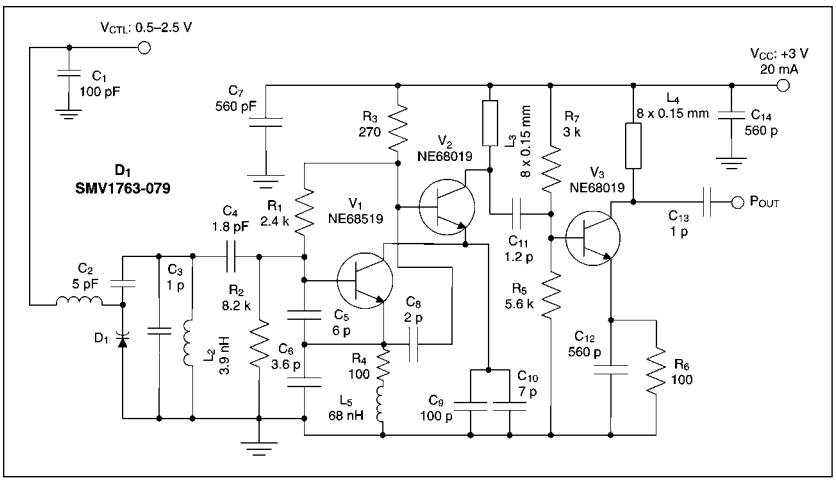
SMV1763-079 is a low series resistance, hyperabrupt junction varactor diode. It is packaged in the small footprint, SC-79 plastic package with a body size of 47 × 31 × 24 mils (total length with leads is 62 mils).

The SPICE model for the SMV1763-079 varactor diode, defined for the Libra IV environment, is shown in Figure 8 with a description of the parameters employed.

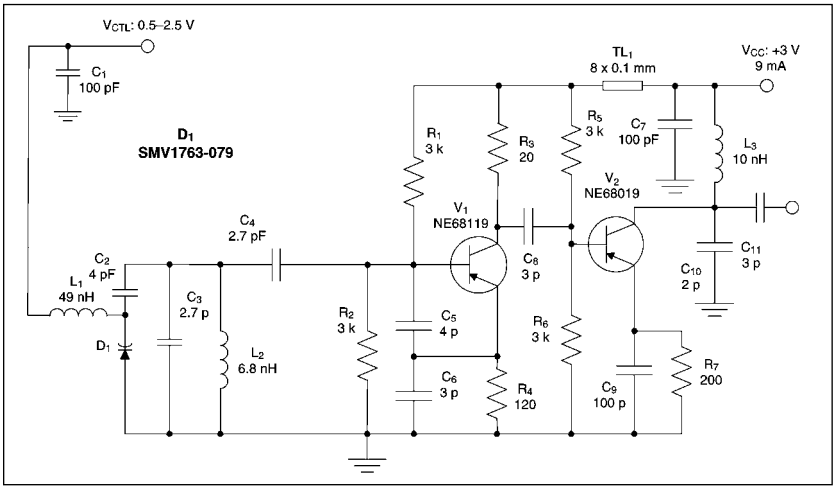
Table 4 describes the model parameters. It shows default values appropriate for silicon varactor diodes that may be used by the Libra IV simulator.

According to the SPICE model, the varactor capacitor, C_V, is a function of the applied reverse DC voltage, V_R, and may be expressed as follows:

$$C_V = \frac{C_{JO}}{\left(1 + \frac{V_R}{V_J}\right)^M} + C_P$$



▲ **Figure 9. RF VCO schematic.**



▲ **Figure 11. IF VCO schematic.**

This equation is a mathematical expression of the capacitance characteristic. The model is most accurate for abrupt junction varactors (like Alpha's SMV1408). For hyperabrupt junction varactors, the model is less accurate because the coefficients are dependent on the applied voltage. To make this equation work better for hyperabrupt varactors the coefficients were optimized for the best capacitance vs. voltage fit as shown in Table 5.

Note that in the Libra model in Figure 8, CP is given in picofarads, while C_{GO} is given in farads to comply with the default unit system used in Libra.

RF VCO design, materials and layout

The RF VCO circuit diagram is shown in Figure 9. The circuit is powered by a 3-volt source. The I_{CC} current was established near 20 mA. The RF output signal is coupled from the VCO through capacitor C13 (1 pF).

The PCB layout is shown in Figure 10. The board is made of standard 10 mil thick FR4 material. The passive components on the board have 0402 footprints.

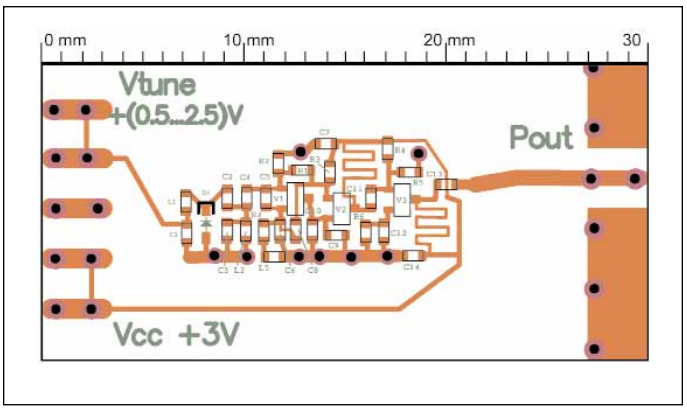
IF VCO design, materials and layout

The IF VCO circuit diagram is shown in Figure 11. This circuit is also powered by a 3-volt source. The I_{CC} current was established near 9 mA. The RF output signal is coupled from the VCO through capacitor C_{11} (3 pF).

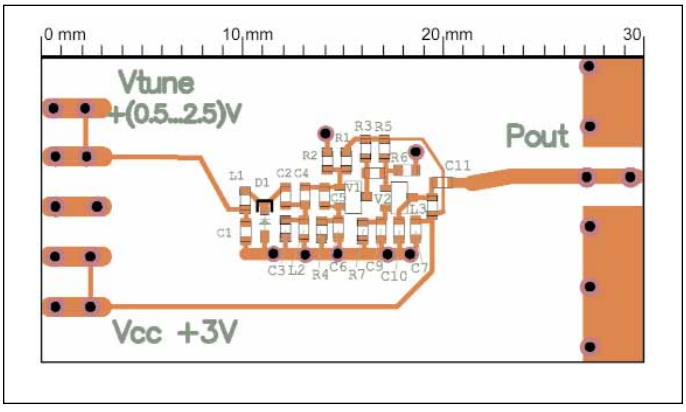
The PCB layout is shown in Figure 12. The board is made using standard 10 mil thick FR4 material. Passive components on the board have 0402 footprints. A bill of materials for each VCO is included in the version of this Application Note that is published on the Alpha Industries Web site: www.alphaind.com.

RF VCO: Measurements and simulation

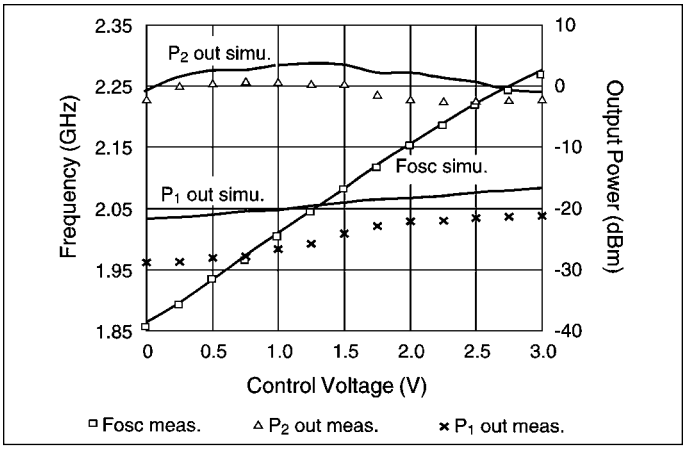
The measured performance of this circuit and the simulated results from the model are shown in Figures 13 and 14. Phase noise measurements are shown in Figure 15, showing performance better than –91 dBc/Hz at 10 kHz offset and better than –111 dBc/Hz at 100 kHz offset. This 20 dB/decade slope is constant to below 10 MHz.



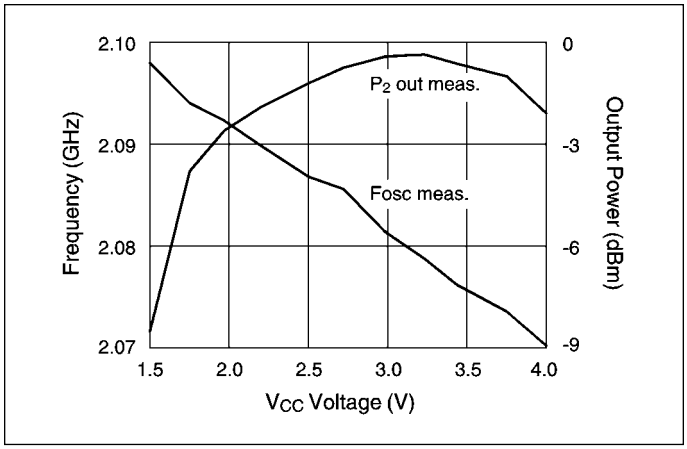
▲ **Figure 10. RF VCO PCB.**



▲ **Figure 12. IF VCO PCB.**



▲ **Figure 13. RF VCO tuning response.**



▲ **Figure 14. RF VCO pushing response.**

Because of frequency doubling, phase noise at the fundamental frequency should be 6 dB better at the far offset. The doubled frequency phase response, shown in Figure 15, gradually diverges from the fundamental frequency as the offset frequency increases with the phase noise difference close to the ideal value of 6 dB. The measurements were performed using an Aeroflex PN9000 Phase Noise Test Set with a 100 ns delay-line.

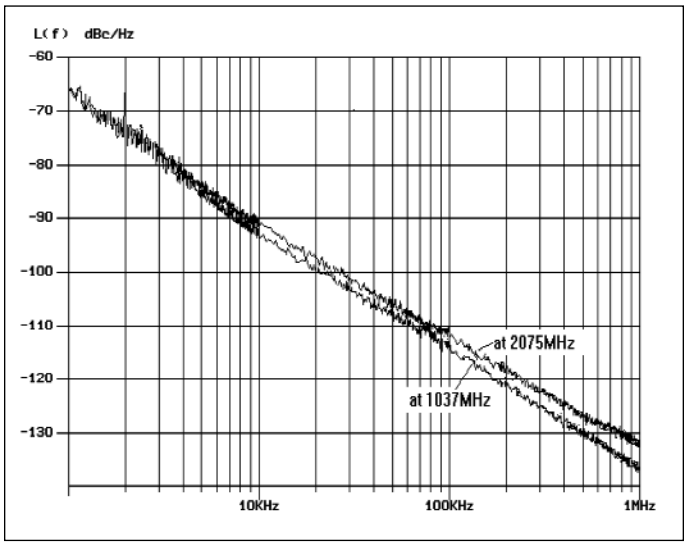
The measured frequency tuning response, in Figure 13, shows near linear, 145 MHz/V, tuning sensitivity in the 0.5 to 2.5 V range typical for battery applications. The simulated frequency tuning response is similar to the measured response. The VCO output power vs. tuning voltage shows a 2 to 4 dB divergence between measurement and simulation. This may be attributed to an inaccuracy in the VCO model parameters, especially to the transistor model parameters. These models are derived for small-signal amplifier applications and may not accurately reflect the higher degree of nonlinearity of a VCO.

The DC supply pushing response is shown in Figure 14. It shows a distinct change of frequency vs. supply voltage, which is probably a result of the dominant VCO emitter-base capacitance. Table 6 summarizes the data measured for RF and IF VCOs.

IF VCO: Measurements and simulation

The measured performance and simulated results of the IF VCO are shown in Figures 16 and 17. Phase noise measurements, shown in Figure 18, demonstrate better than –94 dBc/Hz at 10 kHz offset and better than –114 dBc/Hz at 100 kHz offset. This 20 dB/decade slope is constant to below 10 MHz. As with the RF VCO, these measurements were performed with the Aeroflex PN9000 Phase Noise Test Set.

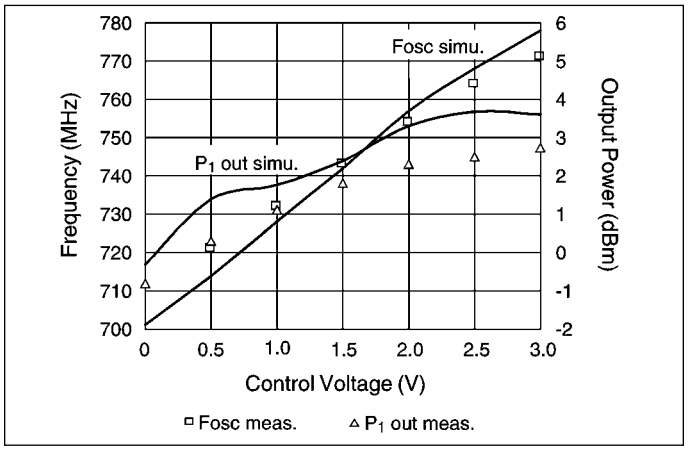
The measured frequency tuning response, in Figure 16, shows 22 MHz/V tuning sensitivity in the 0.5 to 2.5 V range, typical for battery applications. The simulated frequency tuning response shows a higher tuning range



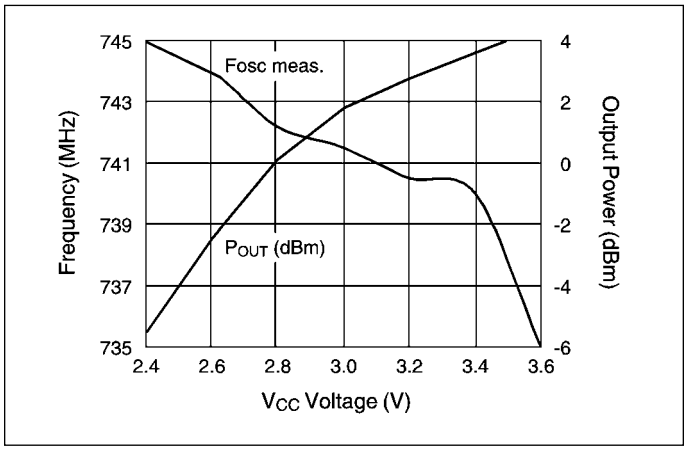
▲ **Figure 15. RF VCO phase noise plot at V_{CTL} = 1.5 V and V_{CC} = 3 V.**

Parameter	Test Conditions	RF VCO	IF VCO
Frequency range (GHz)	V_{CTL}		
	0.5 V	1.93	0.720
	2.5 V	2.22	0.765
Tuning sensitivity (MHz/V)		145	22
Supply voltage (V)		3	3
Supply current (mA)		20	10
Control voltage (V)	V_{CTL}	0.5–2.5	0.5–2.5
Output power (dBm)	P_{OUT}	0 ±2	–8
Pushing figure (MHz/V)		10	5
Pulling figure (MHz)	VSWR = 2		
	at all phases	-	-
Phase noise (dBc/Hz)	@ 10 kHz	–91	–94

▲ **Table 6. Measured RF/IF VCO performances.**



▲ **Figure 16. IF VCO tuning response.**



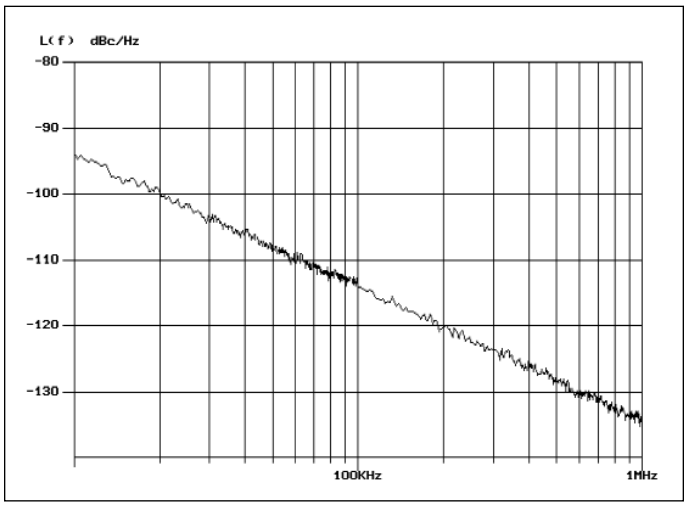
▲ **Figure 17. IF VCO pushing response.**

because the transmission line (TL1 in Figure 7b) significantly affects VCO performance. Another reason for the divergence of the simulation and measurement data is the effect of higher harmonics. A far more complicated circuit model than the one described in Figure 7b is required to account for higher harmonics.

The model used, however, was quite successful in achieving the design goals at the first attempt (directly from simulation to physical design) and in understanding phenomena such as the influence of TL1.

Summary

In this application note, two VCO designs applicable for 2.4 to 2.5 GHz WLAN transceiver functions were demonstrated. It was shown that an RF VCO with a large tuning sensitivity (about 150 MHz/V) could be achieved with low phase noise (<–91 dBc/Hz at 10 kHz offset) using Alpha Industries' low resistance hyperabrupt varactor SMV1763-079. This varactor was also shown to suit a lower frequency IF VCO, providing good tuning range and low phase noise. VCO models were developed that were able to accurately predict performance, and were confirmed by a comparison of simulated and measured performance. ■



▲ **Figure 18. IF VCO phase noise plot at V_{CTL} = 1.5 V and V_{CC} = 3 V.**

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Author information

Dr. Peter Shveshkeyev is Principal Applications Engineer at Alpha Industries, Inc., 20 Sylvan Road, Woburn, MA 01801. He may be reached by telephone at 617-824-4366, by fax at 617-824-4579 or by e-mail at pshveshkeyev@alphaind.com. Additional information about Alpha Industries is available at the company Web site: www.alphaind.com.