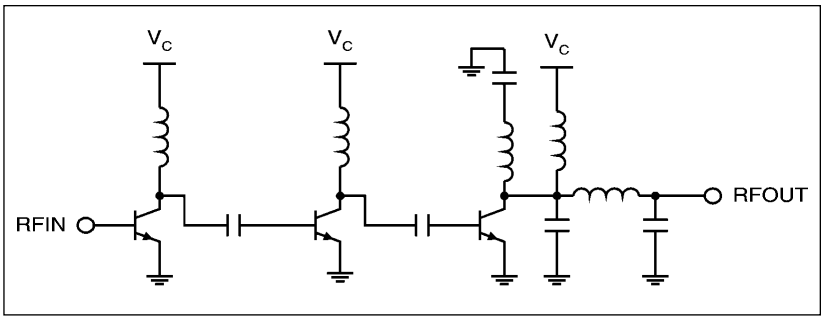
Design of a 3-volt HBT Power Amplifier for DCS

Design techniques and performance data is presented for a new PA RFIC operating at 1.7 to 1.8 GHz

By Bruce Schmukler and Jon Jorgenson
RF Micro Devices

The design of an HBT power amplifier IC intended for 3-volt DCS applications is presented in this article. The impact on the isolation of transistor self-biasing under a large signal drive is investigated using SPICE, and a design improvement is made to eliminate the impact of transistor self-biasing on isolation. Excellent power and efficiency are obtained. For V_{cc} = 3.2 volts, a peak output power of 32.7 dBm is obtained with a peak efficiency of 50.6 percent. For a V_{cc} = 2.7 volts, a peak output power of 31.4 dBm is obtained with a peak efficiency of 51.3 percent. Small, innovative, cost effective packaging for the power amplifier is also described. The performance, size, and cost of this PA are all well suited for high volume cellular phone applications.



▲ **Figure 1. Simplified circuit diagram of a three-stage power amplifier.**

PA design considerations

Consumer demand for wireless communication is ever increasing worldwide, placing a burden on the existing cellular infrastructure. In Europe, the increased demand led regulators to create the DCS cellular telephone band. DCS utilizes GSM baseband technology at carrier frequencies near 1.8 GHz. The handset receiver operates between 1805 MHz and 1880 MHz, while the handset transmitter operates at 1710 MHz to 1785 MHz.

Also in response to consumer demand, cellular telephone manufacturers have been striving to reduce the size and weight of their phones. With the introduction of DCS, and the creation of dual band GSM/DCS phones, the quest for ever smaller components has intensified. A significant way to reduce the size and weight of a phone is to use a 3 volt battery. This can either be a single lithium ion cell, which has the highest energy density of the presently available rechargeable batteries, or it can be three NiMH cells. Each provides about the same voltage.

Manufacturers place many requirements on the DCS transmitter power amplifier. Some of the most important parameters to manufacturers are low voltage operation, power, efficiency, size and power control. Many manufacturers specify that the DCS PA must be capable of operating down to 2.7 volts, with a nominal voltage near 3.2 volts. This allows full utilization of the battery charge to maximize talk time while complying with DCS standards.

These factors have led to the design and development of 3-volt GaAs/AlGaAs HBT power amplifier integrated circuits to address the DCS market by RF Micro Devices. These power amplifier ICs, offered as the RF2140 and RF2174, provide excellent power and efficiency at low voltages: typically 32.5 dBm at 3.2 volts

and 31 dBm at 2.7 volts with an efficiency of 50 percent or more achievable. In addition, the small, innovative packaging used for the PAs is described. With a measurement of just 4 mm on a side, power, efficiency and small size are combined all in one.

Electrical design

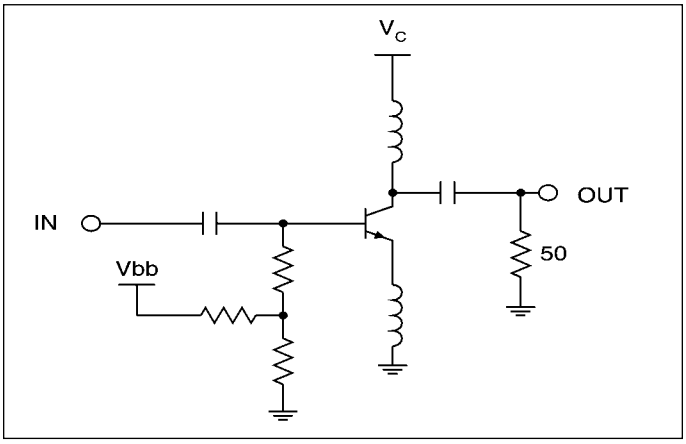
The key design parameters are battery voltage, frequency of operation, power, and gain. High efficiency is also very desirable and should be optimized, given the other constraints. The nominal voltage of operation is chosen to be 3.2 volts in order to be compatible with 3 volt battery operation and to compensate for internal battery and PCB trace resistances. The PA must also produce acceptable power at 2.7 volts. Furthermore, under charging conditions, the PA must be able to survive 4.5 volts to 5.5 volts.

The frequency of operation is 1710 MHz to 1785 MHz, the DCS handset transmit band. The target power is 32 dBm or greater at the nominal voltage of 3.2 volts. This provides power overhead to the manufacturers to compensate for path losses between the PA and the antenna. The input drive power range is 6 dBm to 10 dBm, requiring the amplifier to have at least 26 dB of power gain. High efficiency is always desirable. Factors that effect efficiency are output losses, gain, load impedance and bias conditions.

The general design strategy is to pick the device technology, select the circuit topology, choose the package, determine the number of amplifier stages, size the stages appropriately to abide by current density and thermal dissipation rules, design the matching networks, and then add power control. The device technology is GaAs/AlGaAs HBT for its high breakdown voltage, gain, available power, efficiency, and single supply operation. In order to supply the required power and gain at DCS frequencies, three common emitter stages are needed. The general topology of the circuit is shown in Figure 1, and corresponds to a classic 3-stage bipolar PA design. The first stage is sized for a peak output power of 18 dBm and the second stage is designed for peak power of 25 dBm. This ensures that the output stage will have enough drive power to work in deep class AB operation while simultaneously providing the desired output power.

Deep class AB bias allows the PA to operate very efficiently. It uses the ability of a bipolar device to self-bias under drive power, significantly reducing the quiescent current while enhancing efficiency. Nonlinearity of the amplifier is not an issue for GSM based systems, since they use a constant envelope modulation. The amplifier can operate at peak saturated power without distorting the modulated signal.

The matching networks are generally reactive in order to avoid losses that would degrade efficiency. The output match is composed of two LC sections to transform a 50 ohm load to a 2.4 ohm load line at the output stage collector. In addition, a series resonant 2nd harmonic trap is placed at the output collector. This enhances efficiency by reducing the harmonic distortion in the peak-to-peak voltage swing. Interstage matching is accomplished with a series capacitor and shunt inductor, which is composed of on-wafer, bondwire, package and external inductances. The parasitic components have to be estimated from the package. New, small packaging is utilized for the PA and is described in more detail in a later section.

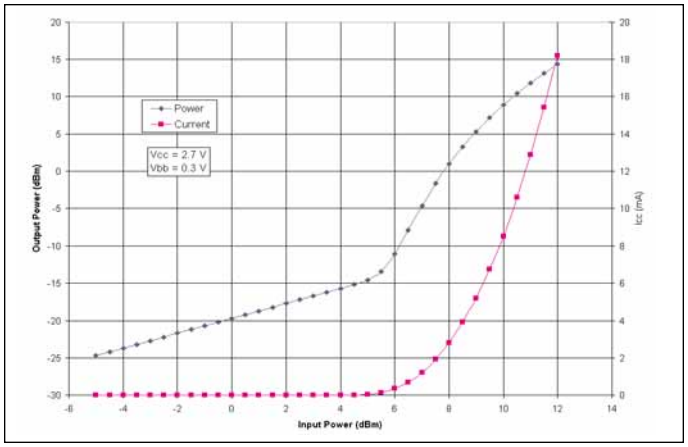


▲ **Figure 2. Single-stage amplifier circuit used for analysis of self-biasing.**

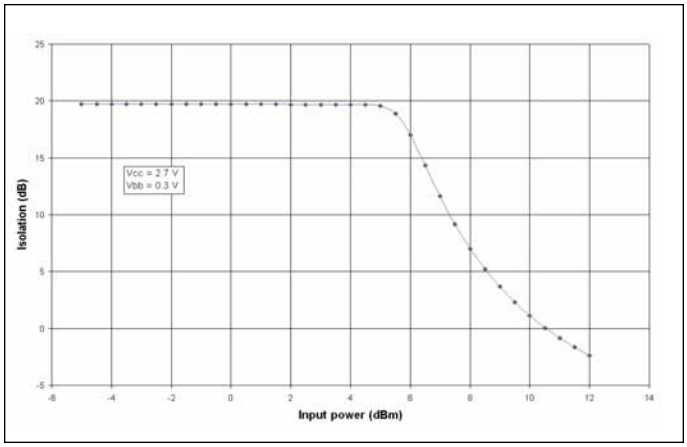
An isolation problem is found

The initial results from the first iteration of die were very encouraging. Target power of 32 dBm at 3.2 volts was surpassed with power-added efficiency approaching 50 percent. Power at 2.7 volts was also very good. All in all, the amplifier met manufacturer specifications except for one deficiency: poor isolation when power control voltage, V_{apc}, is set low. The VCO that drives the PA is generally activated before the PA is turned on and can have a drive power of 6 dBm to 10 dBm. System specifications call for the antenna output power to be below –48 dBm when the phone is not transmitting. Under a worst case condition with an input power of 10 dBm, the PA output power must be –30 dBm or less with V_{apc} = 0.3 volts, the lowest guaranteed power control voltage. The measured isolation for input power from 6 dBm to 8 dBm was acceptable, however, at maximum input power and maximum frequency, the output power was –16 dBm, 14 dB higher than specification. This led to an investigation into the cause of the nonlinear degradation of isolation.

Isolation is characterized as a function of input drive level and V_{apc}, leading to the discovery of two separate mechanisms limiting isolation. One mechanism is the small-signal isolation, which behaves as expected. In the small-signal regime, a 1 dB increase in input power cor-



▲ **Figure 3. Power output and collector current vs. power input at V_{CC} = 2.7 volts.**



▲ **Figure 4. Isolation as a function of input power, showing the rapid degradation above 6 dBm input.**

responds with a 1 dB increase in output power. The effective isolation, defined as input power minus output power, stays constant with drive level. For input levels below 8 dBm, this is the mechanism that affects isolation. At high input drive levels of 10 dBm, it was discovered that the isolation is significantly degraded from the small-signal limit due to self-biasing of the transistors. They should be deactivated, but are partially turned on by the input power. Self-biasing is good for achieving high efficiency, but in this self-bias regime, the isolation is not constant with input drive power, degrading significantly as input power increases. This effect is demonstrated with SPICE simulations in the next section.

Isolation and self-biasing

In this section, the concept of self-biasing and its impact on isolation are explored using transient SPICE simulations of a single-stage HBT amplifier. Figure 2 shows the single-stage amplifier used to simulate the self-bias effect on isolation. For the most part, the circuit mimics the first stage of a 3-stage DCS power amplifier.

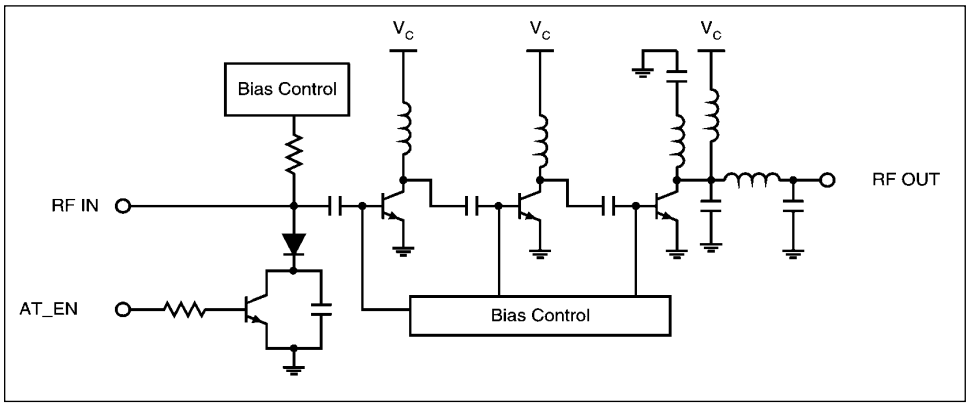
Transient SPICE simulations on the circuit of Figure 2 are run with input power as a parameter. Transient simulations are required since the self-bias effect is a large signal effect. AC simulations would not show this effect. Figure 3 shows the resulting output power and collector current as a function of input power for a V_{cc} = 2.7 volts and V_{bb} = 0.3 volts, which nominally shuts off the transistor. The transistor stays off until input power reaches 6 dBm, after which the collector current starts to increase with input drive power. The transistor self-biases, turning itself on when it should be off. For input power less than 6 dBm, the output power tracks one-to-one with the input power, representing the small-signal isolation regime. Above 6 dBm input, the output power increases more rapidly than the input power. This corresponds exactly to where the transistor self-biases.

Figure 4 shows the resulting isolation as a function of input power for the circuit of Figure 2. The isolation for this single ideal stage is about 20 dB for input power below 6 dBm. The isolation degrades rapidly as input power increases, and actually turns into gain above the 10 dBm level. The smoking gun has been found, the next section describes a solution to the problem.

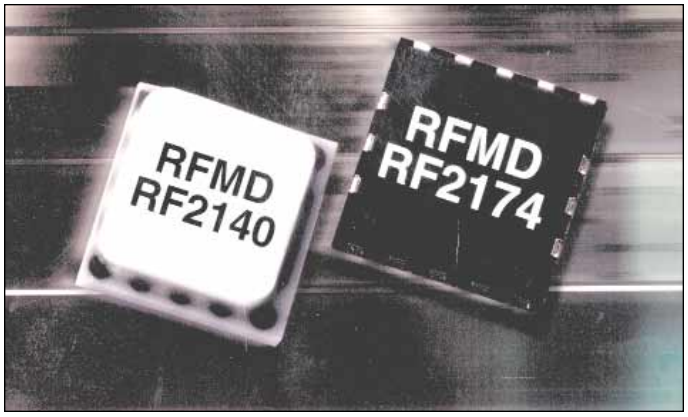
Improved design

Achieving the required isolation is essential for the manufacturer to obtain approval for the handset. There are different ways to solve this from a system view, including complex timing to activate the driver VCO just before the PA or a second isolation switch to provide another 18 to 20 dB of isolation. These are not desirable because they add complexity, components, loss or cost. It would be best for the self-biasing effect to be eliminated.

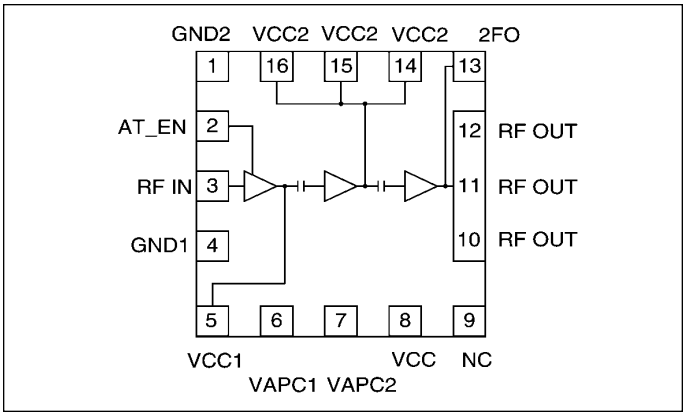
In order to eliminate the effect, we cannot allow the first stage to see an input drive level of



▲ **Figure 5. Circuit of the improved amplifier with a PIN diode attenuator.**



▲ **Figure 6. Photo of the packaged amplifiers.**



▲ **Figure 7. Pinout diagram of the RF2140/2174.**

10 dBm when V_{apc} = 0.3 volts. In addition, when V_{apc} is at full value, we want the first stage to see the full input power level in order to obtain maximum output power and high efficiency. When V_{apc} is low, we want to shunt away power from the first stage, but when it is high, we don't want to add loss to the RF path. Another constraint is that when the PA is dormant, all currents must be nearly zero so that the battery is not constantly drained.

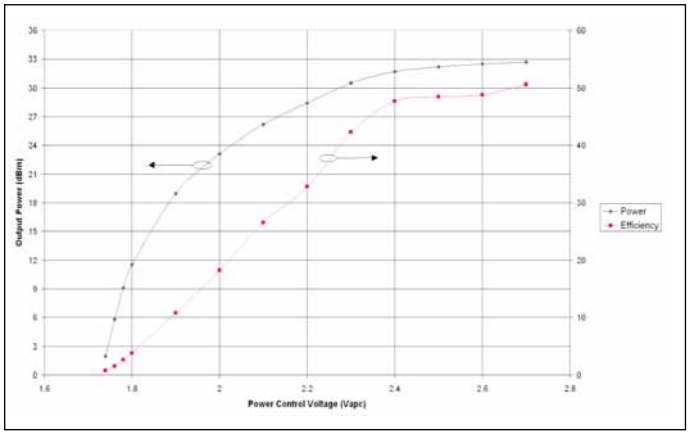
The solution is to add a PIN diode in front of the first stage. The diode is turned on when V_{apc} is low, to shunt power away from the first stage, and turned off when V_{apc} is high, so that there is no RF path loss under normal amplifier operation. Figure 5 shows the revised circuit incorporating the PIN diode. The bias control circuit adjusts the diode current to supply current to the diode when V_{apc} is low and to taper the current as V_{apc} is increased. The PIN diode at high V_{apc} is turned off and looks like an open circuit. At low V_{apc}, it looks like a resistor, attenuating the RF path. An added benefit of the PIN diode is that it reduces the input VSWR at low V_{apc}, eliminating the need for extra matching components.

An extra enable pin, AT_EN, must be added to turn off the PIN diode current when the entire transmitter is off. AT_EN is usually tied to the VCO/transmitter enable. Without this extra enable, the PIN diode would constantly draw current and drain the battery even when the phone is off. All in all, the new design achieves what it is intended to do. Before presenting the results, a description of the packaging for the PA is in order.

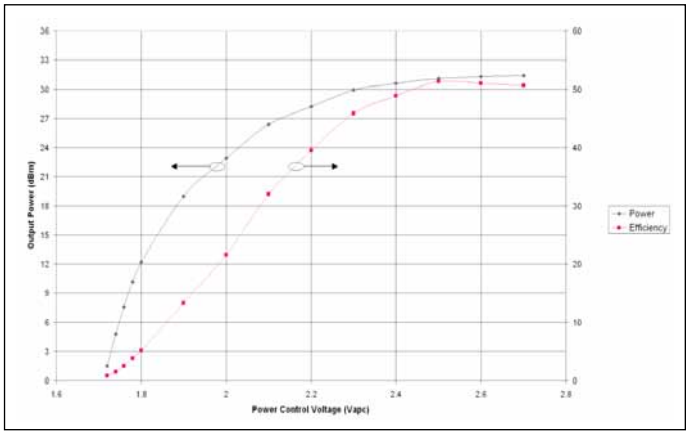
Packaging

Packaging for power amplifier ICs has an importance on par with the electrical design. The package must protect the IC, have low lead inductance, have good thermal performance, be suitable for high volume automated production and be inexpensive. As commercial wireless frequencies continue to climb, packaging of RFICs will grow in importance.

These needs led to the utilization of small, leadless ceramic and plastic packages. The overall dimensions of the packages are 4 mm by 4 mm. They have 16 pins around the circumference spaced 0.8 mm apart and a grounded die flag for low output-stage-emitter inductance. In the ceramic version, three of the leads are fused together to lower the parasitic output inductance, simplifying output matching at higher frequencies. The result is 14 independent I/Os and a backside ground. For



▲ **Figure 8. Measured output power and power-added efficiency (PAE) for V_{CC} = 3.2 V.**



▲ **Figure 9. Measured output power and power-added efficiency (PAE) for V_{CC} = 2.7 V.**

both of these ceramic and plastic packages, pin-to-pin mutual inductance is reduced due to the small size and positioning of pins at 90 degree angles instead of in two rows. These packages are small and leadless, reducing parasitic inductance by at least a factor of two, and up to a factor of four, compared to other available leaded, exposed-die-flag packages.

The packages are manufactured using high volume, low cost, ceramic and plastic technology. For the ceramic package, encapsulation is completed with an air cavity lid. The plastic package is injection molded. The result is robust, small, cost-effective packaging well suited for high frequency RFIC applications. A picture of the final product in ceramic packaging is shown in Figure 6.

Results

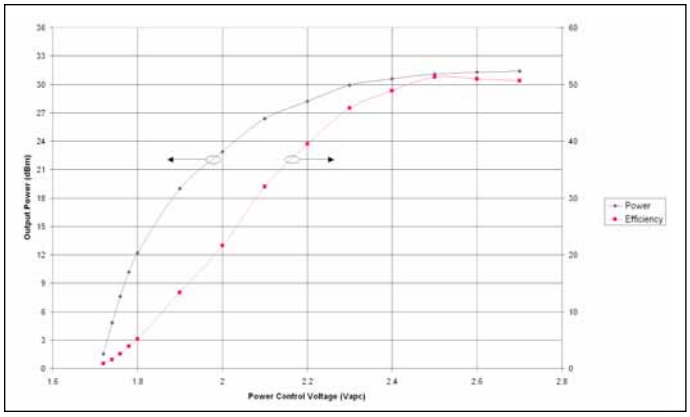
A pin connection diagram of the final amplifier is shown in Figure 7. RF IN and RF OUT represent the input and output respectively. The pins VAPC1 and VAPC2 receive the same power control voltage, but require separate bypassing to prevent interstage crosstalk. AT_EN is the enable for the PIN diode attenuator. The harmonic trap uses pin 2FO. Various ground and voltage-supply pins are utilized for different amplifier stages.

Excellent power and efficiency are achieved. Figure 8 shows a measured plot of output power and associated power-added efficiency (PAE) as a function of power control voltage for V_{cc} = 3.2 volts. A peak power of 32.7 dBm for V_{apc} = 2.7 volts is measured, and a peak PAE of 50.6 percent is achieved. Excellent power and efficiency are also measured with V_{cc} = 2.7 volts, as shown in Figure 9. A peak power of 31.4 dBm is measured; the peak PAE is measured at 51.3 percent. Most manufacturers were impressed with the available power and efficiency from this HBT DCS power amplifier IC.

Isolation is recharacterized with the PIN diode enabled. With a maximum input drive of 10 dBm, isolation is measured to be 43.5 dB to 45 dB over the 1710 MHz to 1785 MHz band, surpassing the target of 40 dB. In addition, the self-biasing effect on isolation is eliminated, proving that the PIN diode circuit works as designed.

The final plot in Figure 10 shows the input VSWR as a function of power control voltage. The nominal VSWR is approximately 2:1 when the PA is operating. When V_{apc} is low, and the PA is off, the input VSWR is well under the 4:1 objective of most manufacturers, without the need for external matching components.

These results show that excellent performance is obtained from the final product. The front-end PIN diode design was verified to eliminate self-bias isolation degradation over the target input power range for



▲ **Figure 10. VSWR vs. power control voltage.**

6 dBm to 10 dBm, and to reduce the input VSWR at low V_{apc}. A patent on this technique has been applied for.

Conclusions

The design of a GaAs/AlGaAs HBT DCS power amplifier IC has been presented. The effect of self-biasing under large signal drive on isolation was demonstrated using SPICE simulations and a solution using a PIN diode to shunt away input power at low power control voltage was successfully implemented, achieving greater than 40 dB of isolation Excellent power in the DCS band is demonstrated with power-added efficiency surpassing 50 percent for a supply voltage down to 2.7 volts using GaAs/AlGaAs HBT technology from RF Micro Devices and small, innovative, cost effective packaging.

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For more information, contact:

RF Micro Devices
7625 Thorndike Road
Greensboro, NC 27409-9421
Tel: 336-931-1233
Fax: 336-931-7454
Internet: www.rfmd.com

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