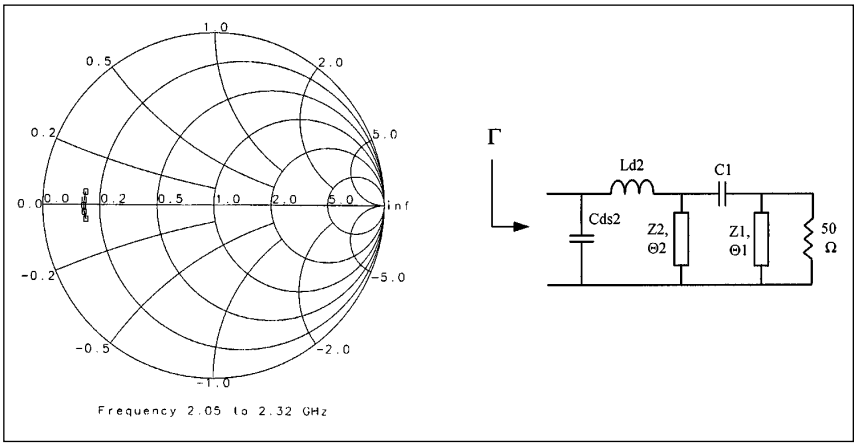
High Efficiency Two Stage Power Amplifiers with Nearly Constant Saturated Output Power

By Brian K. Kormanyos, Boeing Defense and Space Group,
Joe A. Pusl, IBM Wireless Design Center,
John R. Grebliunas and **Andrew W. Fong**, Hughes Space and Communications

Multi-carrier personal communications systems often require power amplifiers with approximately constant 1 dB gain compression point and saturated output power across the frequency range of use. For portable or satellite applications it is also desirable to have high gain, high efficiency and uniform temperature coefficient over the frequency range. A design procedure for a two stage GaAs FET amplifier based on control of the load line over frequency and proper selection of FET size ratio between the stages has been developed to achieve the desired characteristics. The resulting circuits are compact and do not require feedback. The method has resulted in consistently successful design of both hybrid MIC and monolithic MMIC amplifiers at L-band (1.414 GHz) and S-band (2.12 GHz) for both geosynchronous earth orbit (GEO) and medium earth orbit (MEO) satellite to mobile telephone applications. Over a 10 percent operating bandwidth in this frequency range, typical 3-watt single ended designs provide 26 dB small signal gain, 60 percent power added efficiency (PAE) in saturation and 0.5 dB flatness in saturated output power level.



▲ **Figure 1. Desired impedance locus for output matching of the second stage with de-embedded parasitic elements Cds_2 and Ld_2.**

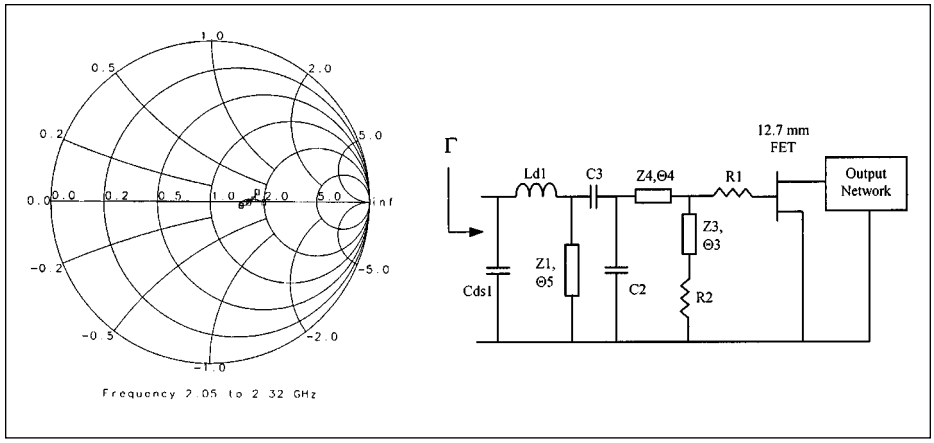
Design procedure

The following procedure illustrates the design of a 3-watt amplifier, but the technique can also be used to design amplifiers at higher or lower power levels. The design begins with the second stage output matching network and proceeds toward the first stage input network.

The load line resistance for the second stage is determined from the DC bias condition of the GaAs FET [1]. The de-embedded parasitic inductance and capacitance, Cds_2 and Ld_2, from the device model are artificially moved outside the reflection coefficient reference plane and absorbed into the matching network design. A nearly constant saturated output power over the frequency range is achieved with an output impedance locus that can maintain a constant real part fixed at the load line value and minimize the imaginary part when viewed from the artificially defined reflection coefficient plane. The desired situation is shown by the typical locus in Figure 1. This matching network is kept lossless for high efficiency operation and simple

to keep the size of the unit to a minimum. A three element high pass matching network is used and the drain bias is inserted through the first element.

Resistive loading is applied to the input of the second stage to achieve stable operation after the output has been matched. We have found that it is not always necessary to increase the *K* factor of this stage to 1.0 or above. A value of 0.7 or 0.8 is often sufficient and can improve efficiency. The stability of the overall two stage should be verified with the *S* probe technique described in [2]. Series and shunt resistive loading is used and the gate bias voltage is applied through the shunt stability resistor.



▲ **Figure 2. Desired impedance locus for wide band interstage matching with de-embedded first stage parasitic elements Cds_1 and Ld_1.**

The interstage network is designed to transform the input of the partially stabilized second stage to the load line impedance desired for the first stage. Cds_1 and Ld_1 are de-embedded and pushed out into the network as before, creating a similar artificially defined reflection coefficient plane. The magnitude of the impedance transformation is rather large due to the high device size ratio and a wide band transformation is desired to maintain the constant gain compression characteristics over bandwidth. Again we seek an impedance locus concentrated at the correct real value with a minimized imaginary part. This goal is not achieved as precisely for this stage as it was for the final output stage but it is also less critical here. The network consists of a high pass L network through which the first stage drain voltage is inserted, and a low pass L network (Figure 2).

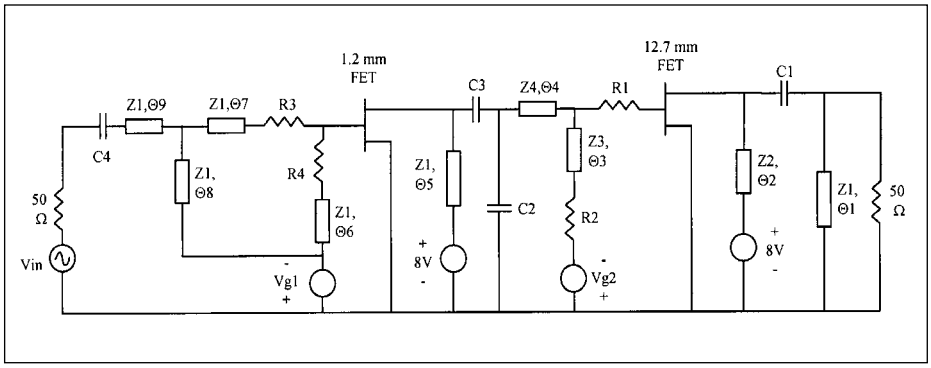
With the completion of the interstage network, all that remains is to apply resistive loading to the input of the first stage to achieve the required level of overall stability, and impedance match the input. A combination of series and shunt resistive loading is used. The first stage input match is accomplished with a band pass type network and the bias is inserted through one of the shunt inductive elements. The complete design is shown in Figure 3.

Device size ratio (fan-out)

The second stage device is sized to meet the power requirements of the design at hand. The size of the first stage device is selected to minimize its DC power requirement while continuing operation in a linear mode so that its contribution to overall gain compression is minimized. The gate current and change in drain current drawn by the first stage as the two stage amplifier is brought into saturation can be used to monitor the level of gain compression of the stage. Ideally, the first stage will not draw any significant gate current or show change in drain current until the second stage is about 1 dB into gain compression.

If an accurate non-linear model [3, 4] or a sufficient design history is available, it is possible to estimate the device size ratio by performing single stage power amplifier designs with devices of many different sizes. Different multi-stage cascades of the single stage blocks can then be considered, and interpolation between device sizes can be used.

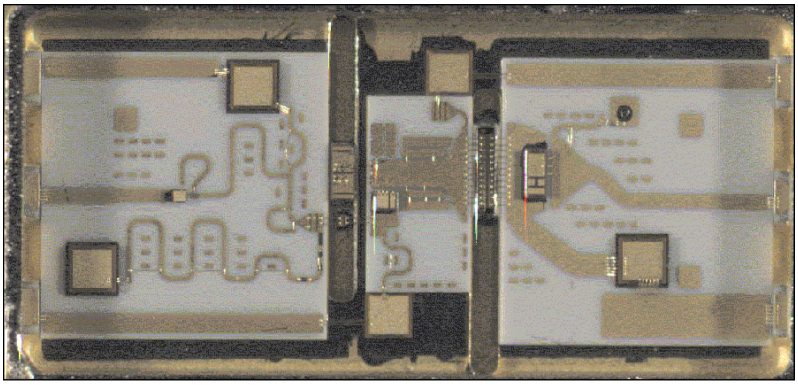
Each trial design is load-line matched on the output, resistively loaded for stability on the input, and its input is reflection matched. Pick a device size for the final that delivers the required saturated output power assuming an appropriate 0.2 to 0.4 dB output network loss. The required input power to saturate the final is known from the non-linear simulation or prior design experience. Pick a first stage device that delivers the required drive power with 1 dB of gain compression or less. The output network loss of this stage can be ignored because it can



▲ **Figure 3. Complete amplifier topology showing the high pass output matching network, combination interstage network, stability network and bandpass input matching network.**

be absorbed into the stability loading at the input of the final. The return loss associated with any driver stage output being matched to its load line, not S_{22} conjugate, is transferred through the interstage networks with the same effect on overall gain because the reflection matched input of any stage downstream looks like a 50 ohm load. It is not necessary to maintain 50 ohms for any device input associated with an interstage in the final design because the reflection loss associated with load line matching will remain constant [5].

We have found empirically that a ratio of second stage to first stage gate periphery near 10 to 1 works well for L- and S-band amplifiers using high performance GaAs MESFETs.



▲ **Figure 4. Photograph of the hybrid MIC S-band amplifier with 26 dB small signal gain, 60 percent power-added efficiency and 0.5 dB gain flatness over a 10 percent bandwidth.**

Results

A hybrid MIC amplifier designed according to the described procedure is shown in Figure 4. The measured small signal gain response is shown in Figure 5. The 1 dB gain compression point and saturated power level across the range of frequency use and temperature are shown in Table 1. Although the amplifier shows excellent performance by itself, the data in Table 1 is taken with a unit including an external gate bias temperature compensation circuit as it is used in the final application. This design has recently been produced for use in an S-band MEO mobile telephony program. This same design technique has also been utilized for an L-band GEO mobile telephony program.

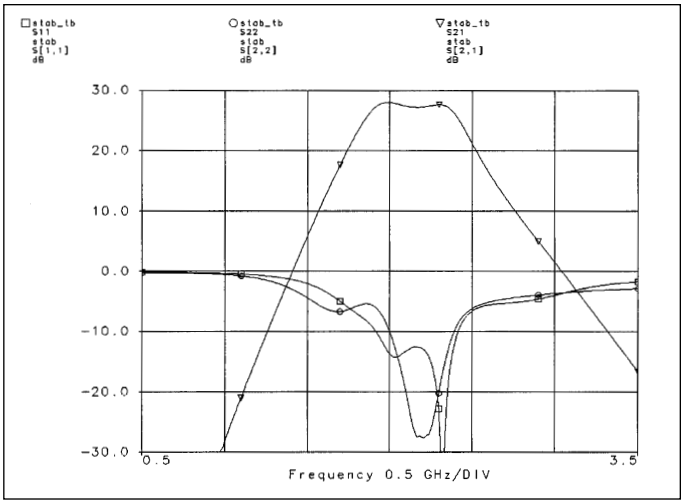
Temp (deg C)	Frequency (GHz) 2.170	2.185	2.200	Frequency (GHz) 2.170	2.185	2.200
	P_{1dB} (dBm)			PAE @ P_{1dB} (%)		
5.0	32.7	32.5	32.4	45.7	46.6	45.6
35.0	32.8	32.7	32.5	45.8	46.8	45.8
65.0	32.7	32.6	32.4	43.9	45.1	43.9
DELTA	0.1	0.2	0.1	–1.8	–1.5	–1.7
	P_{sat} (dBm)			PAE @ P_{sat} (%)		
5.0	34.8	34.7	34.6	61.9	64.5	63.3
35.0	34.8	34.7	34.6	60.4	63.2	62.1
65.0	34.6	34.5	34.4	57.8	60.9	59.9
DELTA	–0.2	–0.2	–0.2	–4.1	–3.6	–3.4

▲ **Table 1. Measured performance of the S-band amplifier showing 1 dB gain compression and saturated output power flatness with gate bias temperature compensation.**

Discussion

The flat band pass type gain response of the two stage is primarily a consequence of the interstage network. The second stage has a slight negative gain slope with frequency on its own and its output matching cannot be compromised without degrading efficiency. Since it is usually a requirement to match the first stage input across the usable frequency range it is difficult to control the gain with this network. The movement of the interstage matching networks true impedance locus (without pushing out Cds_1 and Ld_1) relative to S_{22}* of the first stage is responsible for the characteristic gain flatness across the band of use. The reversing loop causes the impedance locus to move back toward S_{22}* and maintain the overall gain where it would otherwise be rolling off. This wide band small signal gain response with simultaneous large signal load line control is the reason for the improved temperature stability relative to other commercial designs we have examined.

These other designs sacrificed bandwidth to achieve similar performance resulting in a narrow gain peak



▲ **Figure 5. Measured small signal *S* parameters for the S-band two-stage amplifier, showing the typical bandpass gain obtained with this method.**

that tended to walk out of band with temperature change. The overall band pass type gain response obtained with our approach also provides improved stability when used in larger cascaded amplifier chains since there is very little gain at low frequencies where stability problems sometimes occur.

This design procedure has consistently yielded stable high gain amplifiers with remarkably high efficiency considering that no special consideration was taken of the GaAs FET terminations at the second or third harmonic frequencies [6]. Another feature of this design technique is that it provides excellent performance repeatability which is essential for meeting the amplitude and phase tracking requirements of phased array antenna applications.

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Author information

Brian K. Kormanyos received a 1989 BS degree in electrical engineering from the University of Washington, and MS and Ph.D. degrees in experimental electromagnetics in 1991 and 1994, respectively, from the University of Michigan. His research activity was in the area of quasi-optical millimeter wave mixers, oscillators, and power combining arrays. Previously, he was with Hughes Space and Communications Company, where he worked on non-linear microwave components for satellite applications. Since April 1996, he has been with The Boeing Space and Defense Company, working on power amplifier MMICs and unique microwave transitions for phased array antennas and terrestrial LMDS wireless systems. He may be reached by e-mail at L.kormanyos@att.net.

Joe A. Pusl received a 1990 BS degree and a 1992 MS degree in Electrical Engineering, both from the University of California at Santa Barbara. His graduate emphasis was on microwave circuit design and solid state physics and modeling. While pursuing his MS degree, he worked on broadband millimeter-wave MMIC designs and on millimeter-wave network analysis technologies. From July 1992 to April 1998, he was with Hughes Space and Communications Company in Los Angeles, CA, where he worked on device development and the design of MICs and MMICs for low-noise and power applications. He is now with the IBM Wireless Design Center in Encinitas, CA, designing RFICs for cellular handsets.

John R. Grebliunas received a 1982 BSEE degree from the University of Illinois and a 1985 MSEE degree from the University of Southern California. He has 18 years of experience in the design, development, manufacture and test of communication electronics for satellite payloads. He has developed RF electronics for Broadcast Satellite Service, Fixed Satellite Service, Mobile Telephony Phased Array Satellite Service and Broadband Wireless Connectivity Satellite Service applications. He has been with Hughes Space and Communications Company since 1982 and is currently project manager for development of K-band active phased array RF modules.

Andrew W. Fong received a 1995 BSEE degree from the University of Illinois and a 1998 MSEE from the University of Southern California. Since 1995, he has been a Staff Engineer with the Hughes Space and Communications Channel Electronics Group, specializing in microwave circuit design. His work is concentrated in the area of high efficiency solid state power amplifiers, low noise amplifiers and linearizers.