A High IIP_3 Low Noise Amplifier for 1900 MHz Applications Using the SiGe BFP620 Transistor

This application note describes the design of a practical LNA

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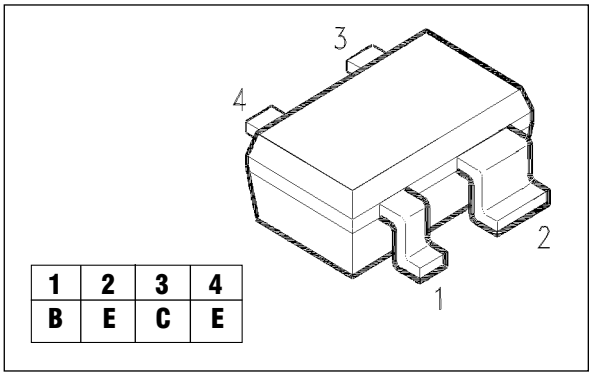
Infineon's BFP620 is a high-performance, low-cost silicon germanium bipolar transistor housed in a 4-lead ultra miniature SOT-343 surface mount package. With a transition frequency (f_T) in excess of 70 GHz, this device is ideal for high performance applications, including Low Noise Amplifiers in portable telephones and other battery operated wireless communications devices. The BFP620 offers exceptionally low noise figure, high gain and high linearity at low power consumption levels. The BFP620 rivals more expensive GaAs MESFET and PHEMT devices in performance without requiring a negative supply voltage.

This application note describes a low noise figure, high 3rd-order intercept PCS band LNA targeted for 1900 MHz CDMA applications, and also provides general guidelines for improving 3rd-order intercept performance in amplifiers using Infineon transistors.



▲ **Package and pin assignments for the BFP620.**

Overview of 1900 MHz high-linearity LNA

The schematic diagram for the 1930 to 1990 MHz low noise amplifier (LNA) is shown in Figure 1. The amplifier is intended for use in low-cost battery powered applications such as those found in PCS band or TriMode CDMA cellular handsets. Design goals include a gain of 15 dB, unconditional stability, a noise figure under 1.1 dB, an input 3rd order intercept Point (IIP_3) of +10 dBm, reduced parts count and a low PCB area requirement. Input and output return loss values of better than 10 dB were sought in order to ease integration with a duplexer and image-stripping filter.

Measurement results are summarized in Table 1. These are mean values taken from a sample lot of ten applications boards. The insertion losses of the connectors and microstriplines are not backed out for these results. If the (input) transmission line and connector losses

Parameter	Symbol	Value
Gain	dB [S_{21}]	14.7 dB
Noise figure	NF	1.04 dB
Input 3rd order intercept point	IIP_3	+10.3 dBm
Output 3rd order intercept point	OIP_3	+25.0 dBm
Output 1 dB compression	OP_{1dB}	+ 5.8 dBm
Input return loss	dB [S_{11}]	13.3 dB
Output return loss	dB [S_{22}]	14.6 dB
Collector-emitter voltage	V_{CE}	2.1 V
Supply current	I	8.9 mA
LNA PC board area	—	~45 mm^2
Number of external SMT components*	—	12

* Includes bias resistors and DC blocks

▲ **Table 1. Typical performance for BFP620 application at 1960 MHz, T = 25 °C, V = 3.0 V.**

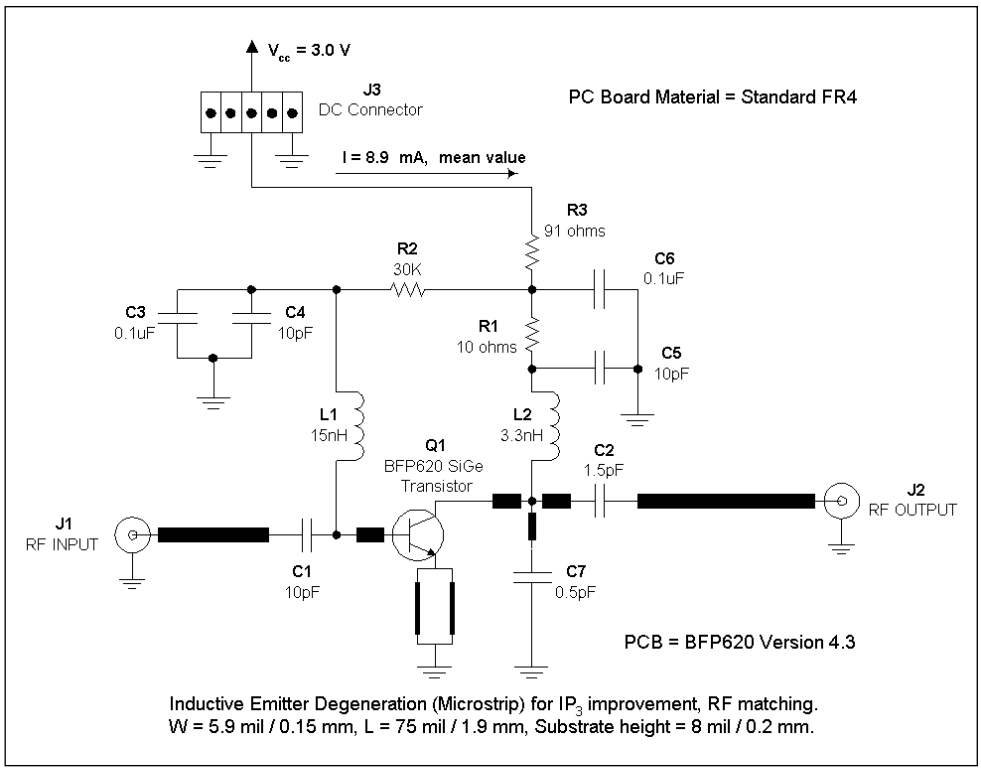
were subtracted, the noise figure result would be about 0.2 dB lower.

Figure 2 is the PC board cross section. The board material is standard FR4. Note that spacing from the top layer RF traces to the internal ground plane is 0.008 inch (0.20 mm).

Low noise amplifier design considerations

In subsequent sections, the various design considerations and trade-offs for this particular LNA will be described. These factors include:

1. Linearity
2. Stability
3. Noise figure
4. Input/output match
5. DC bias



▲ **Figure 1. Schematic diagram for the PCS LNA, printed circuit board Version 4.3.**

1. Linearity

The primary design goal for this low noise amplifier (LNA) was to achieve an input 3rd-order intercept point of +10 dBm, while consuming less than 10 mA of DC current. To this end, two techniques were employed: inductive emitter degeneration, and use of additional charge storage across the base-emitter junction of the transistor.

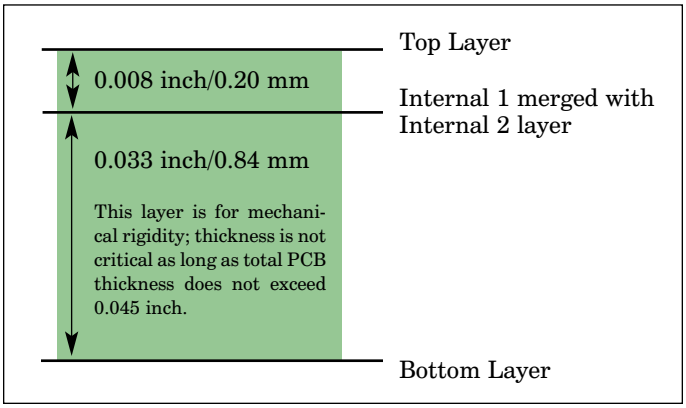
The usual method employed for measuring 3rd-order intercept point (IP_3) involves injecting two equal amplitude sinusoidal signals at frequencies f_1 and f_2 into the amplifier input, and observing the relative levels of the test signals f_1, f_2 and third-order products $2f_2 - f_1$ and $2f_1 - f_2$ at the amplifier output. The third-order products, as well as all other signals present at the amplifier output besides f_1 and f_2, constitute distortion and are the result of nonlinear behavior within the transistor, most notably across the base-emitter junction. For the testing done on this particular LNA, each input test tone power level (P_{IN}, input power for both f_1 and f_2) is set to –20 dBm, and the spacing between the tones is nominally 1 MHz. The input 3rd-order intercept point (IIP_3) is calculated as follows:

$$IIP_3 = P_{IN} + \frac{\Delta IM_3}{2}$$

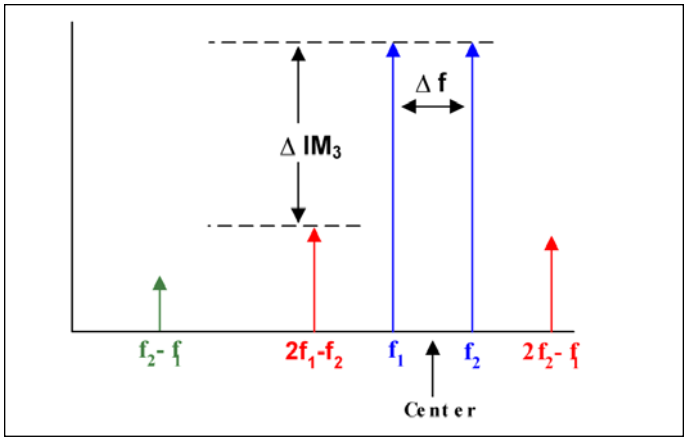
where ΔIM_3 = the *difference* in amplitude between one of the two equal amplitude test tones present at the amplifier output, and the level of the highest 3rd-order distortion product (Figure 3).

Inductive emitter degeneration

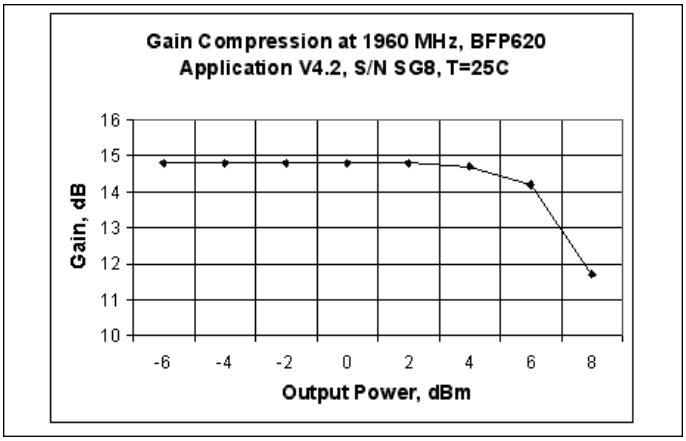
The process of intentionally inserting additional inductance between device emitter connections and RF ground is a commonly employed method used for influencing device input/output match, noise match, stability and linearity. Inductive degeneration does not seriously impact noise figure performance, as resistive degeneration does. In this design, two microstriplines, each with dimensions of 0.15 mm × 1.9 mm, serve as inductors between each device emitter lead and PCB ground plane. This additional inductance provides "series-series" negative feedback, improving amplifier 3rd-order intercept and gain compression points, at the cost of reduced gain. For this LNA, approximately 1.5 to 2 dB of gain is traded to attain improved linearity. In other



▲ **Figure 2. PC board cross section.**



▲ **Figure 3. Partial representation of output spectrum of the LNA, showing 3rd order and low-frequency products.**



▲ **Figure 4. Typical gain compression curve of the LNA at 1960 MHz, T = 25 °C, V = 3.0 V.**

words, typical gain in a similar applications board with direct emitter grounding was 16 to 16.5 dB, and this gain was reduced to 14.7 dB by the use of inductive emitter degeneration.

Effect of adding additional charge-storage across the base-emitter junction

One of the spectral lines generated by device nonlinearities during a two-tone test is a low frequency product, $(f_2 - f_1)$. For the case of a test tone spacing of 1 MHz, this 1 MHz product modulates the base-emitter and collector-emitter voltages of the LNA at a 1 MHz rate. Recalling that for a bipolar transistor, emitter current is an *exponential* function of the base-emitter voltage,

$$I_e \approx I_{es} e^{\left(\frac{qV_{BE}}{kT}\right)}$$

one can imagine this low frequency AC signal present at the device terminals varying the operating point of the transistor at the rate $(f_2 - f_1)$, thus adversely impacting distortion product levels.

If a relatively large value capacitor is placed across the base-emitter junction to bypass this low frequency product $(f_2 - f_1)$, the voltage fluctuation seen by the base-emitter junction of the transistor can be reduced, and the levels of the 3rd order products minimized (Figure 1). Capacitor C3, 0.1 μF, performs the low-frequency bypass function described here. An improvement in third-order intercept point of approximately 5 to 10 dB can be expected by using this "trick." The same effect may be seen by using extra charge storage on the collector, but the results are usually not nearly as dramatic.

The closer together the two input test tones f_1 and f_2 are in frequency, the lower frequency the product or beat note $(f_2 - f_1)$ is. Therefore, as input test tones f_1 and f_2 come closer together, more capacitance is needed to achieve best possible bypassing of the low frequency product $(f_2 - f_1)$. For a test tone separation of 1 MHz, 0.1 μF was found to be more than adequate in this particular application circuit. A good physical or gut-level feeling for the efficacy of this trick can be determined by testing the LNA with and without C3 in place, and by experimenting with different test tone spacing and capacitor values for C3.

For best results, the transistor should see a nice, low-impedance path at low frequencies between this additional charge storage and its terminals. For this reason, a coil rather than a high-value resistor is used to bring in the base bias voltage and isolate the RF from the DC bias network. The 15 nH inductor used on the base to bring in the DC bias has negligible impedance up to tens of megahertz, but provides enough impedance at 1.9 GHz to nearly isolate the base of the transistor from the bias network within the LNA's normal operating frequency range. For applications requiring operation over wide temperature ranges, the effect of temperature on capacitor dielectric and capacitor performance should be investigated.

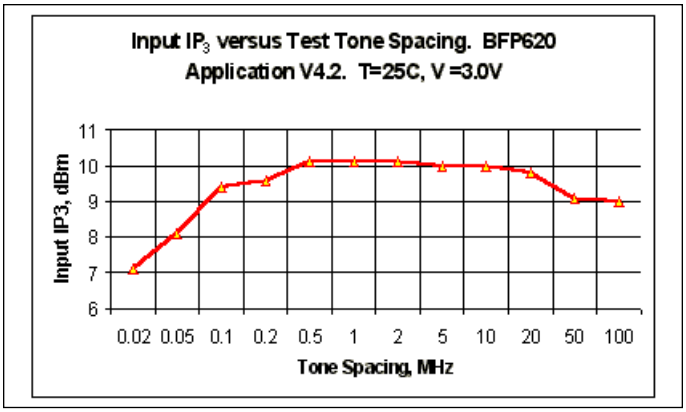
It is important to note that bypassing the $(f_2 - f_1)$ product as described here does not affect the compression level of the amplifier — only the third-order intercept point. As a result, if this bypassing technique is used, the general rule of thumb stating that there is approximately a 10 dB difference between third-order intercept and 1 dB compression points is no longer valid. In this application, the input IP_3 is +10 dBm, and the input P_{1dB} is typically –7.9 dBm, with a difference of 17.9 dB between these two points. A typical gain compression curve is shown in Figure 4.

Test tone spacing vs. IIP_3

The reader may wonder what happens to third-order product distortion levels as the two input test tones are separated in frequency. A BFP620 V4.2 Applications

f_1 (MHz)	f_2 (MHz)	Δf	IIP_3 (dBm)
1959.990	1960.010	20 kHz	+7.1
1959.975	1960.025	50 kHz	+8.1
1959.950	1960.050	100 kHz	+9.4
1959.900	1960.100	200 kHz	+9.6
1959.750	1960.250	500 kHz	+10.1
1959.500	1960.500	1 MHz	+10.1
1959.000	1961.000	2 MHz	+10.1
1957.500	1962.500	5 MHz	+10.0
1955.000	1965.000	10 MHz	+10.0
1950.000	1970.000	20 MHz	+9.8
1935.000	1985.000	50 MHz	+9.1

▲ **Table 2. Input 3rd order intercept versus test tone spacing for a BFP620 V4.2 Application Board.**



▲ **Figure 5. Input IP_3 versus test tone spacing, BFP620 Application Board V4.2; V = 3.0 volts, center frequency = 1960 MHz, T=25 °C.**

Board was tested for input IP_3 over a range of test tone spacing, from 20 kHz to 100 MHz. In each case the midpoint frequency $(f_1 + f_2)/2$ was 1960 MHz. Results are tabulated in Table 2 and plotted in Figure 5.

As previously mentioned, one limiting factor at close tone spacing is the available charge storage (e.g., value of C3), or "how good of a low frequency ground" one has across the base-emitter junction (and also, to a lesser degree, at the collector). At wider tone spacing, the product $(f_2 - f_1)$ rises in frequency, and the impedance of the RF chokes that isolate the DC bias circuit from the transistor begin to play a role — and this undesired impedance begins to roll off or degrade IP_3 performance.

Of course, the selectivity of the matching circuits at LNA input and output also have some influence, particularly as the test tones are separated more widely and begin to fall out of the normal operating frequency range of the amplifier.

Linearity summary

For this LNA application, two methods are used to improve third-order intercept performance: inductive emitter degeneration, and low-frequency bypassing of the $(f_2 - f_1)$ product at the base-emitter (and collector) junction.

Inductive emitter degeneration achieves linearity improvement at the cost of reduced gain. Other methods may be employed to achieve further reduction of third-order distortion levels, but these two simple methods are less likely to be influenced by temperature and LNA termination impedance than some of the more exotic techniques reported in the literature [1].

2. Stability considerations

In general, for a linear two-port device characterized by *S*-parameters, the two necessary and sufficient conditions to guarantee unconditional stability (e.g., no possibility of oscillation when the input and output of the device are both terminated in any passive real impedance) are

a) $K>1$, and b) $|\Delta|<1$, where

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$$

$$|\Delta| = |S_{11}\cdot S_{22} - S_{12}\cdot S_{21}|$$

In the literature one may encounter an alternative form for these two conditions as

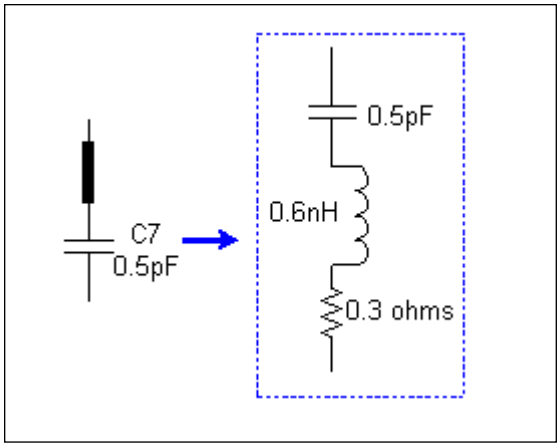
a) $K>1$, and b) $B_1>0$, where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

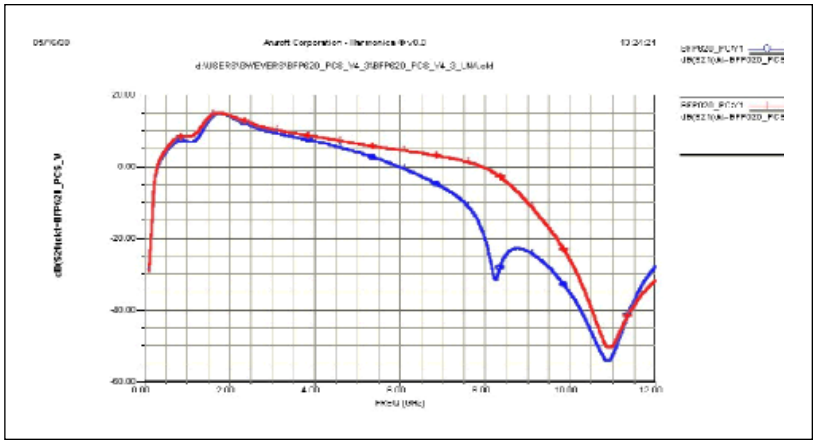
A simulation tool is of great help when trying to optimize an amplifier for stability. The Ansoft Serenade® design environment was used for simulations in this LNA design, including evaluating the stability factors K and B_1 up to 6 GHz.

Stability below 6 GHz

At the time of this writing *S*-parameters were available for the BFP620 from 10 MHz to 6 GHz. Initial simulations looked at stability factors K and B_1. The use of inductive emitter degeneration for the purposes of linearity improvement also had a major impact on the stability of the amplifier. In brief: a small amount of emitter degeneration improves stability at lower frequencies, but as the amount of emitter inductance is increased, stability at higher frequencies — that is, in the range of 5 to 12 GHz — is compromised. In simulations, and later confirmed with measurements, output resistive loading



▲ **Figure 6. Approximate lumped-element model for Capacitor C7 in 0402 package.**



▲ **Figure 7. Simulated plot of LNA gain showing effect of capacitor C7 on high frequency gain of LNA.**

(see schematic, R1, 10 ohms) in conjunction with the additional emitter inductance helped to bring *K* to a value greater than 1, particularly in the range of 800 to 1200 MHz. The RF bypass capacitor C5, 10 pF, has less of an effect at lower frequencies as compared to at 2 GHz. Hence, the LNA output "sees" this lossy 10 ohm resistor below band, improving stability in that region. Having some stability margin in this range is especially important given that PCS band duplexers typically look very reflective in the 800 to 1200 MHz range.

Stability above 6 GHz

As stated previously, a small amount of additional emitter inductance can help stabilize the BFP620 at lower frequencies, but larger amounts of added emitter inductance can jeopardize stability at higher frequencies — for this particular amplifier, in the region above about 8 GHz. As the BFP620 is a very high gain device with an extremely high transition frequency, the potential for high frequency instability exists, and thus great care must be exercised.

A large amount of inductive emitter degeneration was required in order to meet the linearity requirement target of an input IP_3 of +10 dBm with less than 10 mA of current. Due to this large amount of required emitter inductance, it was found that the LNA could oscillate at 10 GHz if both LNA input and output were left open-circuited. The 10 GHz oscillation could be observed on a spectrum analyzer if the area near the LNA were "sniffed" with an RF probe while amplifier input and output were left open-circuited.

[Note: A cable with a PC Board mount SMA connector inserted into one end may be used as a makeshift

RF probe, with the center pin of the SMA connector used as an "antenna." Be sure to include a DC block at the spectrum analyzer input!]

Another observable symptom of the 10 GHz oscillation was a shift in DC operating current. As the input and output of the LNA is changed from a 50 ohm termination to an open circuit, the DC current increases by 0.5 to 1.5 mA.

In a real application (e.g., with a duplexer at LNA input and a ceramic image-stripping filter at LNA output), the LNA would not see a perfect open circuit at all frequencies, and a problem might not exist. Nevertheless, this situation of marginal stability with input and output open-circuited is undesirable. As *S*-parameters were only available to 6 GHz, a careful analysis of K and B_1 was not possible at 10 GHz. A more empirical approach was taken to eliminate the potential 10 GHz oscillation.

If it were possible to kill the gain of the LNA above 8 GHz or so, while leaving PCS band gain largely unaffected, it might be possible to eliminate the potential 10 GHz instability. To this end, a simple, crude, but effective fix was employed.

In Figure 1, note the 0.5 pF capacitor C7. An approximate lumped-element model for this capacitor is shown in Figure 6, including the short microstrip track leading to the capacitor and the chip capacitor's self-inductance and equivalent series resistance (ESR). In general, for best simulation accuracy, it is a good idea to try to model parasitic reactance in circuit elements, e.g., modeling the parasitic capacitance/self-resonant frequency of chip coils, or parasitic inductance and equivalent series resistance (ESR) of chip capacitors.

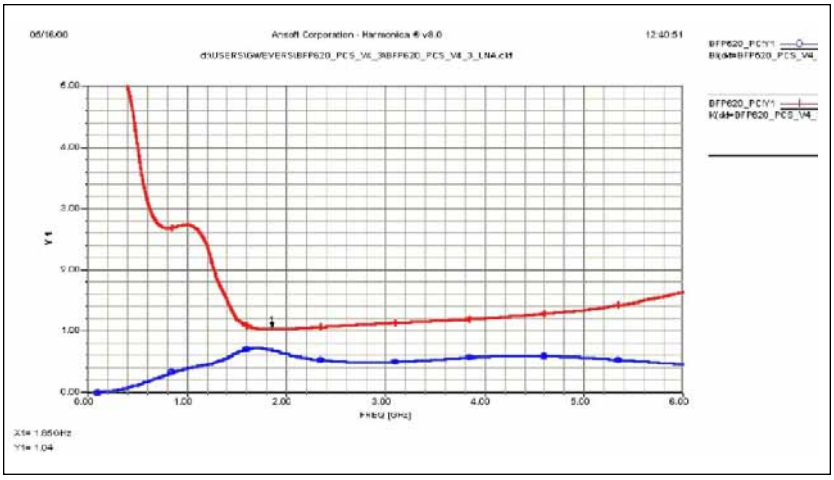
The 0.5 pF 0402-size chip capacitor C7 has its in-circuit self-resonance at approximately 9 GHz, given by

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

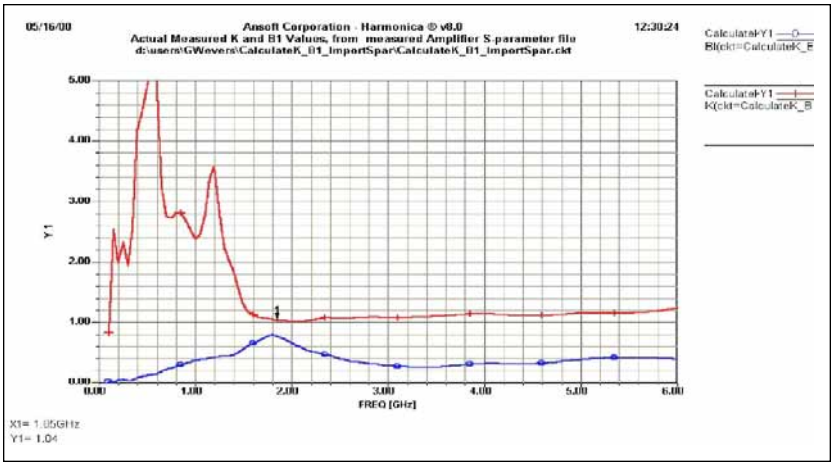
As a series resonance, C7 tends toward a short-circuit condition near 9 GHz. The main idea of this technique is that LNA gain in the vicinity of 8 to 11 GHz is reduced by "shorting out" the LNA output in this frequency range with C7, hence killing the potential oscillation. The effect on gain in the 1900 MHz PCS band was minimal, with a loss in gain of around 0.2 dB. Despite *S*-parameters being available only to 6 GHz, the simulation plot in Figure 7 gives a good qualitative idea of how

this element affects the amplifier with respect to gain above 5 or 6 GHz. (The simulator extrapolates *S*-parameters above 6 GHz.) In each case for the simulation, with and without C7, the output is re-matched for optimum amplifier gain and return loss. Note the reduction in gain above about 6 GHz when C7 is added to the LNA output. This above-band gain reduction helped eliminate the potential 10 GHz oscillation.

Simulated and measured plots of the stability factors K and B_1 for up to 6 GHz appear in Figures 8 and 9 for a BFP620 Version 4.3 PC board. For Figure 9, measured *S*-parameter data taken from an actual BFP620 board is imported into the circuit simulator, which then calculates and plots K and B_1.



▲ **Figure 8. Simulated plot of stability factors K and B_1 up to 6 GHz. Note K>1 and B_1>0 for entire region. The minimum K value is 1.04 at 1850 MHz.**



▲ **Figure 9. Measured stability factors K and B_1 vs. frequency for a V4.3 BFP620 Applications Board. Compare to simulated results in Figure 8.**

3. Noise figure

The BFP620 is capable of excellent noise figure performance up to 6 GHz, and offers noise figure values comparable to more expensive PHEMT and GaAs MESFET devices.

Near 2 GHz, the bias current for minimum noise figure is about 5 mA. However, the +10 dBm Input IP_3 requirement could not be met with only 5 mA of current, and for this particular application a minimum current of approximately 8 mA is required.

Table 3 gives noise parameters for the BFP620 at 1.8 GHz and a V_{CE} of 2.0 volts at 5, 8 and 10 mA collector current. This should help the reader understand how bias current influenced noise figure in this design. If the +10 dBm IIP_3 requirement were dropped (as would be the case in a "low-desense requirement" LNA design), less current (and less emitter degeneration) could be used, and noise figure values of just under 1.0 dB in an application circuit should be possible.

The emitter degeneration used for linearity improvement also had the pleasant side-effect of moving the optimum noise match and return loss match a bit closer together in terms of impedance. A plot of noise figure for a BFP620 V4.2 Application Board is given in Figure 10.

I_c (mA)	F_{MIN} (dB)	Γ_{opt} (mag)	Γ_{opt} (ang)	$R_n/50$
5	0.65	0.16	71	0.14
8	0.71	0.09	97	0.08
10	0.76	0.06	111	0.11

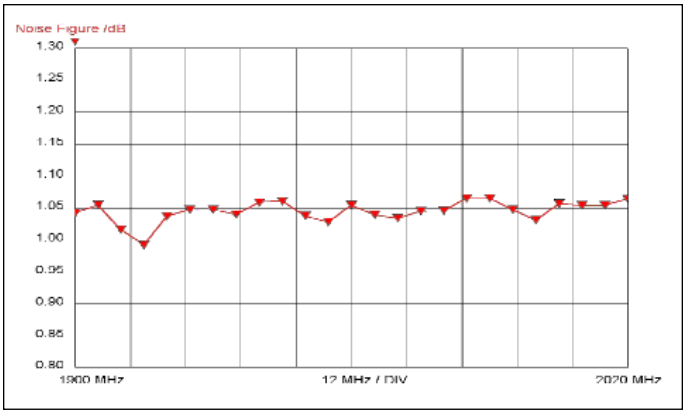
▲ **Table 3. BFP620 noise parameters at 1.8 GHz for V_{CE} = 2.0 volts.**

4. Input/output match

As stated in the previous section, the use of added emitter inductance helped to move the optimum noise match and optimum return-loss match closer together in terms of impedance.

The output matching circuit is a high-pass network consisting of L2 and C2. Due to the non-zero S_{12} of the device, the output matching circuit was used to favorably influence the input return loss.

The influence of the output matching circuit on the input return loss together with the positive effect of the added emitter inductance for both return loss and noise matching enabled the elimination of any RF matching elements at the device input. Only a 10 pF DC blocking capacitor (C1) and a coil to bring in DC bias voltage to the base (L1) were required at the input. This elimina-



▲ **Figure 10. Plot of noise figure vs. frequency for a BFP620 V4.2 Application Board. Span is 1900 to 2010 MHz. Temperature = 25° C.**

tion of input tuning elements also permits optimizing the design for a balance of input return loss and noise figure with fewer iterations. A good linear RF simulation tool is very helpful in gaining insight into circuit behavior and trends in this regard.

At the input, L1 presents a relatively high impedance at the 1900 MHz PCS band, and as such has minimal influence on the input match of the circuit. This coil has a minimum self-resonant frequency of 2300 MHz, which lies above the LNA's nominal frequency range.

The input and output return loss for a typical BFP620 Version 4.3 Application at the low, middle and upper edge of the PCS band is shown in Table 4.

Frequency (MHz)	dB (S_{11})	dB (S_{22})
1930	12.2	19.5
1960	13.3	15.9
1990	14.9	13.7

▲ **Table 4. Input and output return loss for the BFP620 V4.3 Application Board S/N MS6.**

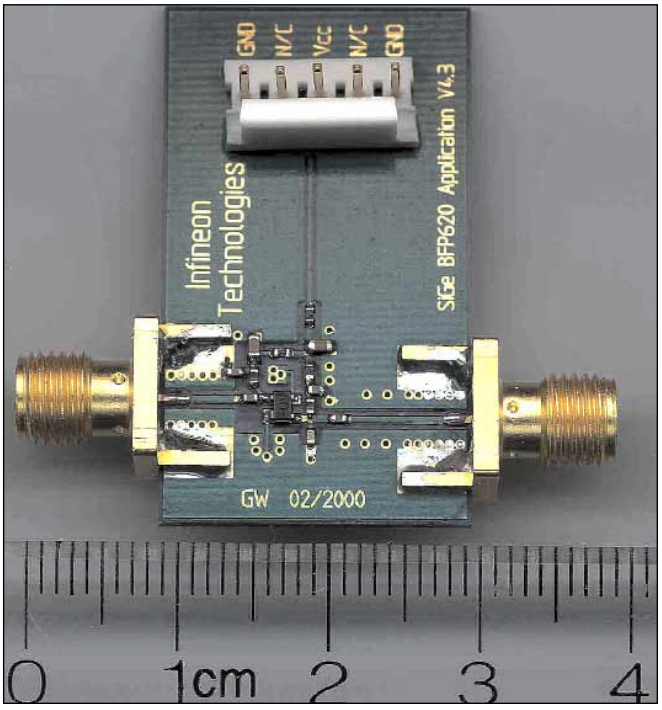
Temperature (° C)	Total Current (mA)
–40	8.3
+25	8.9
+85	9.4

▲ **Table 5. Bias current variation from –40 to +85 °C in a BFP620 Application Board V4.1.**

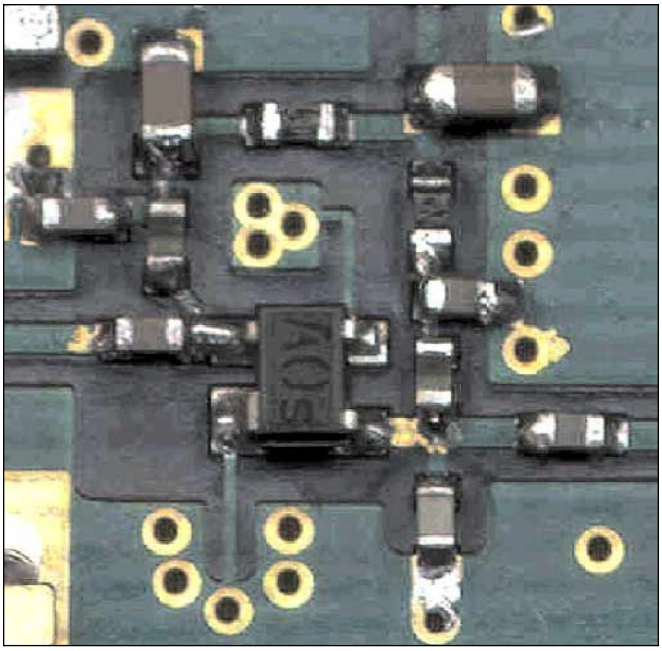
5. DC bias

In terms of the chosen DC bias setting, a compromise of the various specification targets — gain, linearity, noise figure and power consumption — had to be made. Higher current improves linearity and gain, but as shown in an earlier section, noise figure increases with

Appendix A. Images of the BFP620 Application Board.



▲ **View of Version 4.3 evaluation circuit printed circuit board.**



▲ **Close-in shot of application PCB showing parts placement. Microstriplines used for inductive emitter degeneration are visible between each of the two emitter leads and ground vias.**

higher current levels. Linearity is also improved with increased collector-emitter voltage (more voltage swing available at the amplifier output) but as one nears the collector-emitter breakdown voltage (BV_{CEO}) noise figure can begin to degrade due to the onset of voltage breakdown effects.

The BFP620's worst-case collector-emitter breakdown voltage (BV_{CEO}) is 2.3 volts, but typically is higher. Balancing and trading off the various target specification goals resulted in a nominal bias point of 2.1 volts for the collector-emitter voltage and 8.9 mA device current.

In Figure 1, resistor R3 drops the supply voltage down from 3.0 volts to approximately 2.1 volts. R2 supplies bias to the base of the transistor. R1 is present for LNA stability improvement, not for DC bias purposes.

This simple bias circuit offers a low to moderate amount of negative feedback to compensate for DC beta variation from device to device and over temperature. If the device current increases due to temperature or device-to-device variation in DC beta, the voltage drop across R3 increases, reducing the voltage seen by the base, thereby providing negative feedback. The DC current shift over the –40 to +85 °C range for a BFP620 applications board is shown in Table 5. If a more stable bias scheme is required, an active bias circuit using either a PNP transistor or the Infineon BCR400W active bias controller is recommended [2, 3].

Summary and conclusions

Infineon's silicon germanium BFP620 bipolar transistor offers a very high performance, power-efficient and cost-effective solution for high frequency low noise amplifier (LNA) designs.

This application note describes a high-linearity LNA design for 1900 MHz PCS band applications. The BFP620 is also a good solution for low-noise amplifiers operating in the European and Asian UMTS/WCDMA frequency ranges. Evaluation boards for the LNA application depicted in this application note are available from Infineon Technologies. The company's Web site is www.infineon.com. ■

References

1. Vladimir Aparin, Charles Persico, "Effect of Out-of-Band Terminations on Intermodulation Distortion in Common-Emitter Circuits."

2. "Application Considerations for the Integrated Bias Control Circuits BCR400R and BCR400," *Application Note No. 014*, Infineon Technologies, Silicon Discretes Group.

3. Peter Vizmuller, *RF Design Guide, Systems, Circuits, and Equations,* Artech House, 1995. (Pages 76-78 show active biasing of an RF bipolar transistor.)

Author information

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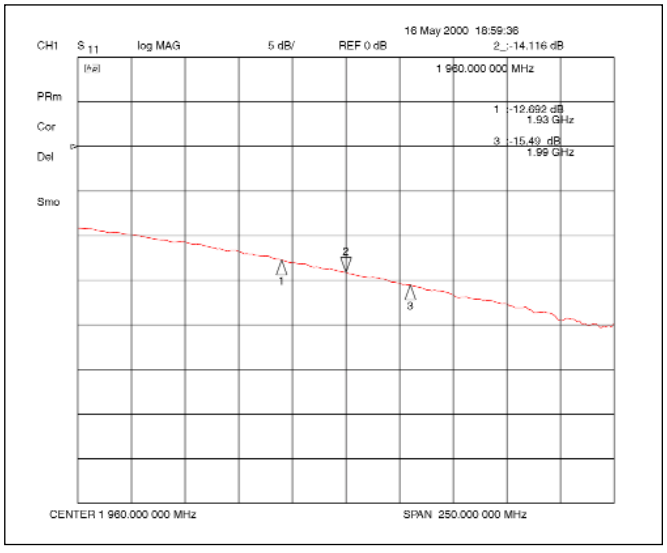
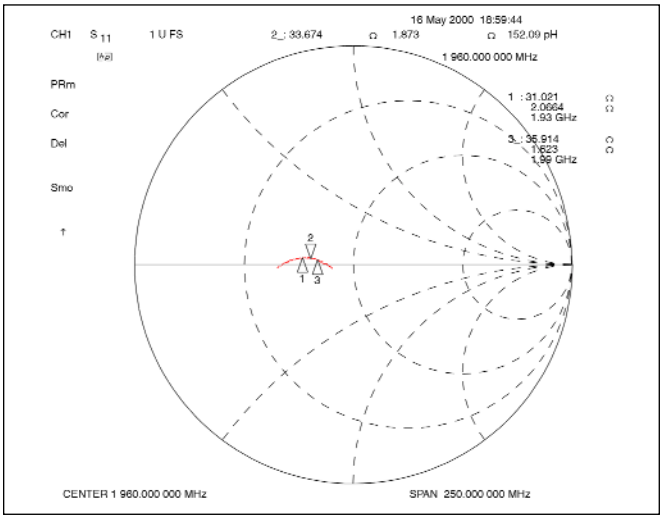
Appendix B. Data Plots for a BFP620 Version 4.3 Applications Board (S.N. MS5)

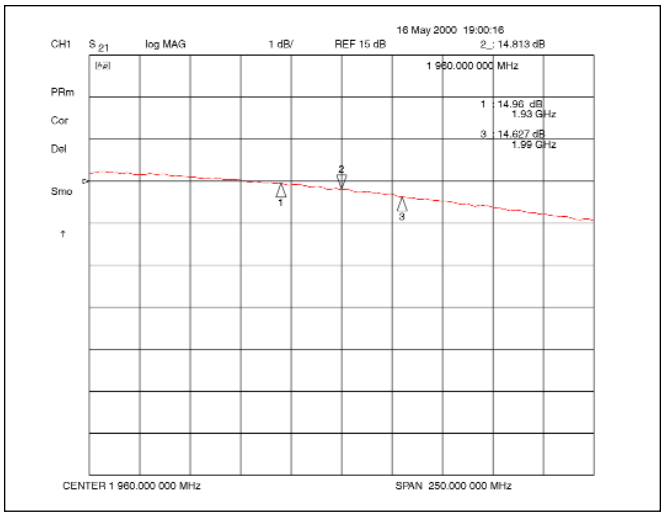
(continued on the following page)



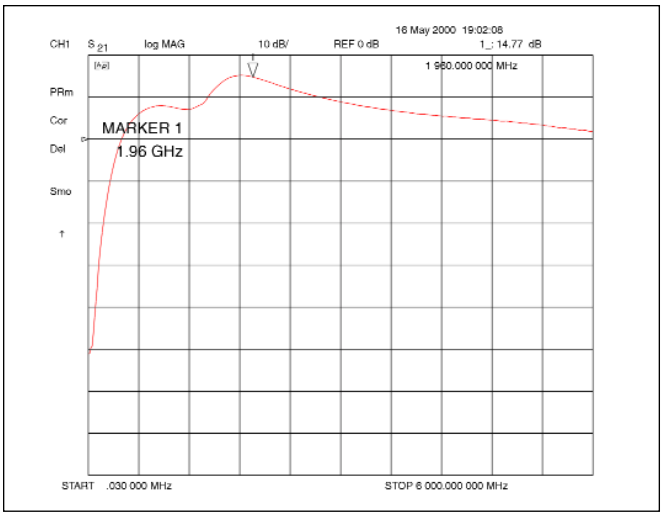
▲ **Input return loss (Log Mag).**



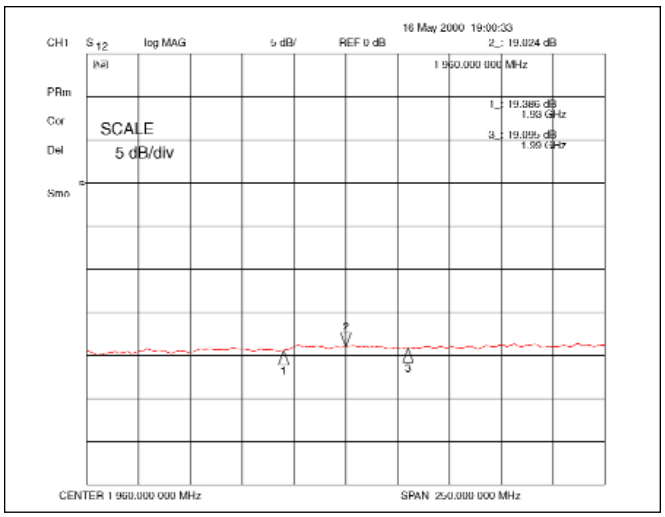
▲ **Input return loss (Smith chart). The reference plane is normalized to the PC board input RF connector.**



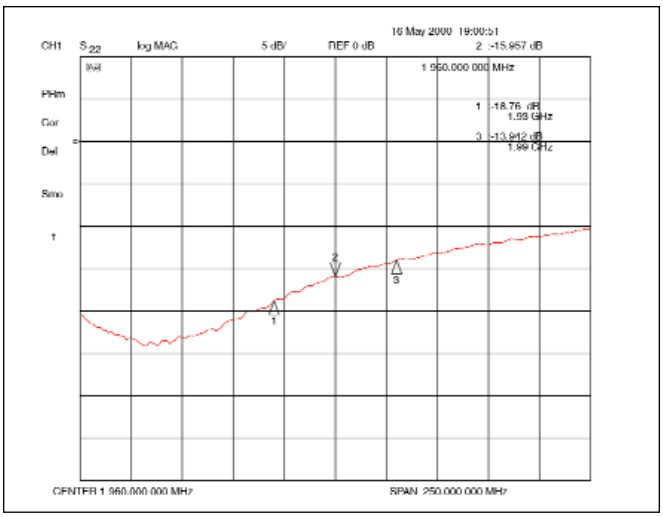
▲ **Forward gain, 1960 MHz ±125 MHz.**



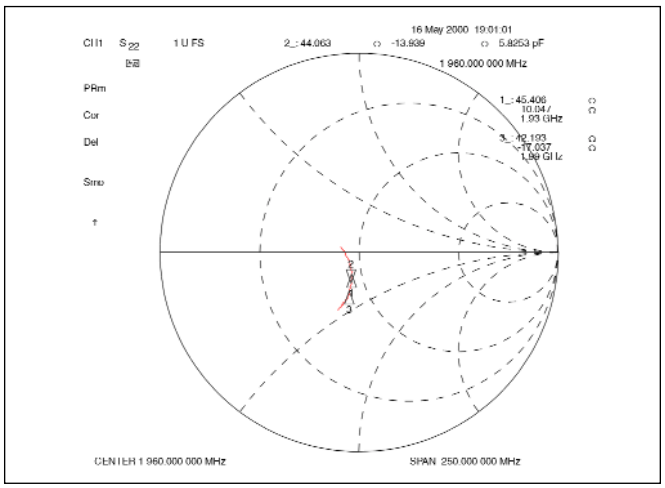
▲ **Forward gain, wide span (30 kHz to 6 GHz).**



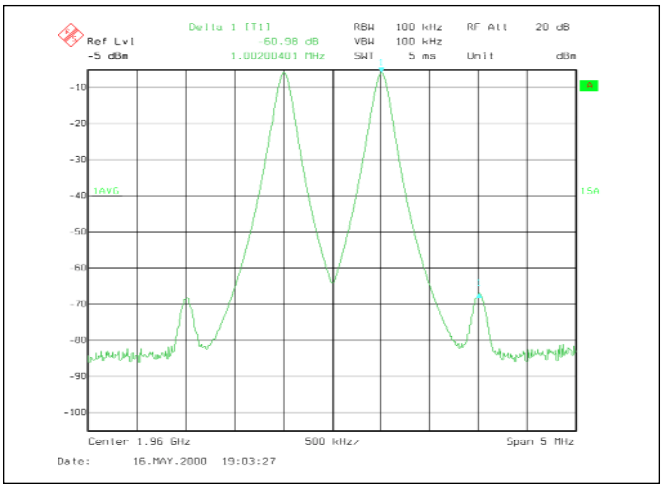
▲ **Reverse isolation.**



▲ **Output return loss (Log Mag).**



▲ **Output return loss (Smith chart). Note that reference plane is at the PC board RF output connector.**



▲ **Output response of the LNA with two-tones at f_1 = 1959.5 MHz. and f_2 = 1960.5 MHz, –20 dBm each tone.**