*Friedrich Krug, DJ 3 RV*

# A 10 MHz Timebase Clock for Frequency Counters, complete with a PLL for DCF77

**If one attempts to measure the frequency of a RF-signal exactly using a number of different frequency counters, one will experience that a number of different measured values will be obtained due to the fact that the timebase clocks usually differ from the nominal frequency. For this reason, the author developed a 10 MHz standard for testing and aligning the timebase clocks of frequency counters. The frequency is coupled to the 6.2 MHz signal from the DCF77 receiver, described in Edition 2/84 of VHF COMMUNICATIONS (1), with the aid of a phase-locked loop. This provides a sufficiently accurate standard.**

The clock oscillator of a digital frequency counter should oscillate exactly at the nominal frequency, and possess a good long-term stability, since any deviation will cause a correspondingly large relative error of the readout. For this reason, a high-quality oscillator is required such as a temperature-compensated crystal oscillator (TCXO), or even better an oven-controlled crystal oscillator (OCXO).

In order to compensate for the long-term drift of the frequency due to aging, it is advisable to use a control circuit that is derived from a standard frequency.

When using the DCF77 receiver described in (1), a reference signal will be available with which such a frequency control can be made with relatively simple means.

The described module uses an available oscillator, i.e. a temperature-compensated 10 MHz crystal oscillator (TCXO), with a capacitive fine frequency alignment. This oscillator represents a good clock even when it is not controlled. This means, that it provides a very accurate frequency standard even if the DCF77 transmitter should go off the air.

The frequency control is made via a phase-locked loop (PLL). Either the 6.2 MHz signal, or the 3.1 MHz signal from the DCF77 receiver is used as reference signal.

Since the module is to be used as a clock for digital circuits, the 10 MHz output signal provided at the output is at TTL-level. It can be divided down to 1 Hz using decade dividers. Any decade frequencies from 10 MHz to 1 Hz, and intermediate values of 5 MHz, 500 kHz, etc. down to 5 Hz are available by using ÷5 and ÷2-dividers. This makes the clock also suitable for other applications.

Due to the possibility of resetting the six lower frequency divider decades, it is easily possible to generate the required switching and control signals for a digital counter.

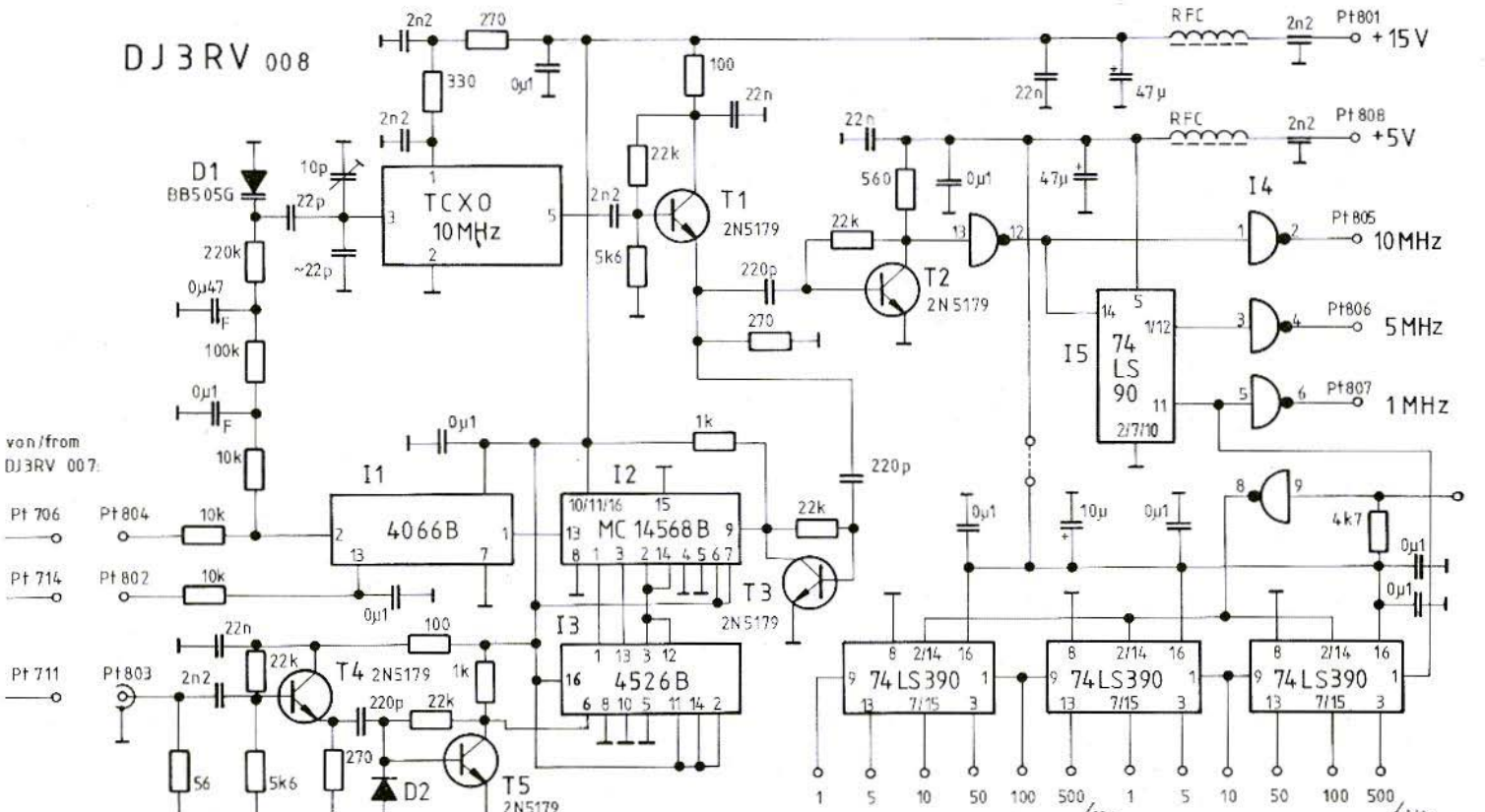


**Fig. 1: Circuit diagram of the 10 MHz oscillator module with programming of the divider for a reference signal of 6.2 MHz**

## 1. CIRCUIT DESCRIPTION

As can be seen in the circuit diagram given in **Figure 1**, a temperature-compensated crystal oscillator (TCXO) provides the required 10 MHz-signal whose frequency can be pulled using a variable capacitance. According to the manufacturer, this capacitance of 27 pF comprises a fixed capacitance, a 10 pF-trimmer for fine alignment, and the varactor diode D 1 for frequency control.

The frequency control using the phase comparator I 2 is similar to that used in module DJ3RV 007 (1). The 10 MHz output signal of the TCXO is fed via buffer amplifier T 1 and an impedance converter to level converter T 3 (CMOS-level), and then divided in I 2. The frequency division factor amounts to 100, which is programmed by connecting pins 10 and 11 to "high".

The 6.2 MHz reference signal from module DJ3RV 007 is fed to connection Pt803, and amplified to CMOS-level in T 4 and T 5. Integrated circuit I 3 and the second programmable divider in I 2 divide this signal by 62 and feed it to the phase comparator.

Unfortunately, it was found that not all CMOS-dividers operated well at 6.2 MHz. For this reason, the next section is to study the possibility of injecting a 3.1 MHz signal, and to divide this by 31.

The phase comparator operates at 100 kHz; the control signal is available at the tri-state output I 2/pin 13. With the aid of switch I 1, it is possible for this signal to be switched off when DCF77 is not transmitting. The switching voltage is fed to Pt802, and is also supplied by module DJ3RV 007. In this case, a very stable voltage of 5 V will be present at diode D 1 which is fed to Pt804 also from the DJ3RV 007-module.

The 10 MHz signal is amplified in T 1 and T 2 and is coupled out at TTL-level at Pt805. The divider I 5 divides by 2 and 5 so that a 5 MHz-signal is available at Pt806, and a 1 MHz-signal at Pt807.

A further divider chain is available on the board that comprises six decadic dividers, which means that signals down to 1 Hz are available. This divider chain can be reset, frozen, and started in a defined manner. It is thus possible for the control signals to be generated for a frequency counter.

## 2. CONSTRUCTION

The circuit is accomodated on a single-coated PC-board (DJ3RV 008), which is enclosed in a metal box of 74 x 148 x 50 mm (see **Figure 2**).

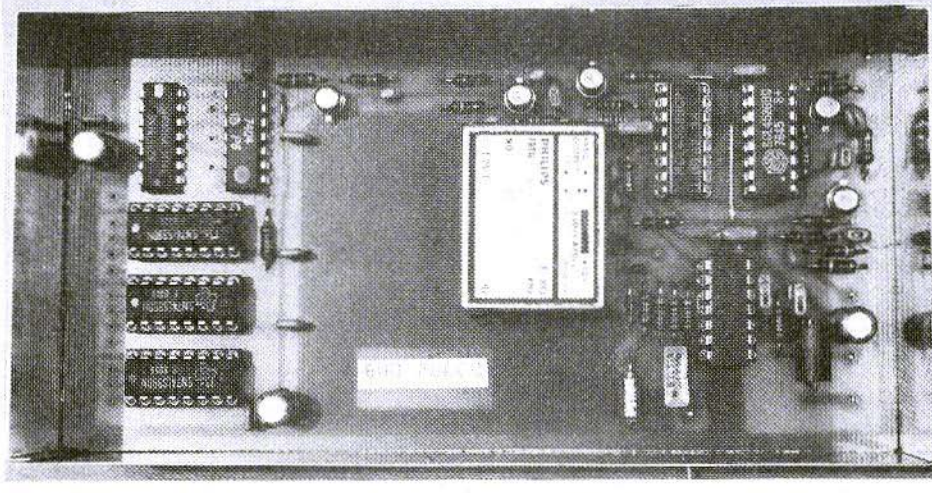

**Fig. 2: Photograph of the author's prototype oscillator module DJ 3 RV 008 The ICs in the PLL should be soldered into place.**

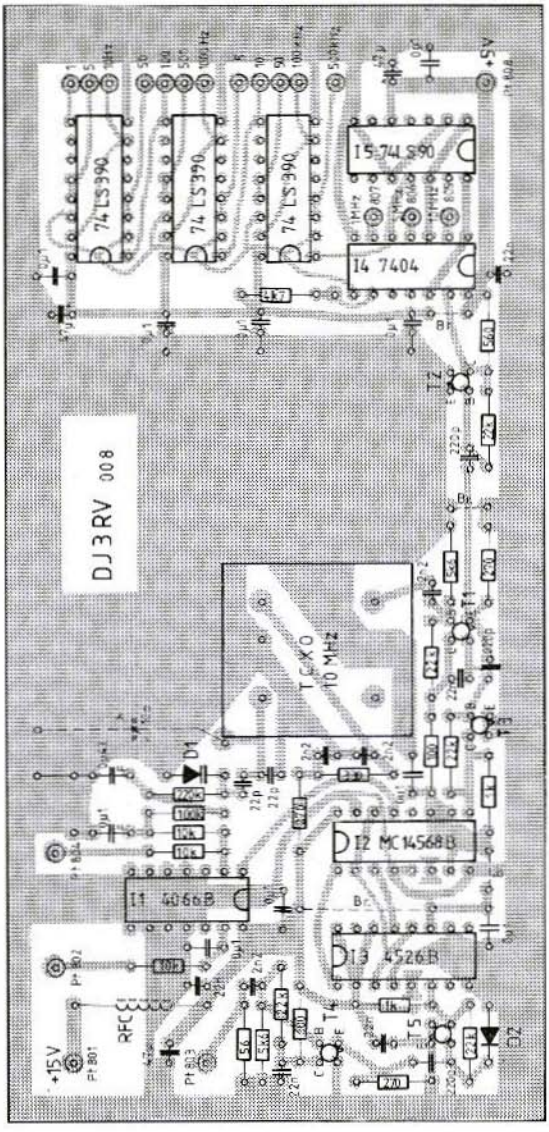


Fig. 3: Component location plan for the single-coated board DJ 3 RV 008

The location of the components can be seen in the component location plan given in **Figure 3**. The special components are given in the following components list:

**Components List for DJ3RV 008**

T 1 to T 5: 2N5179 (RCA) or similar UHF-transistor, e.g. BFX 89, BFY 90

I 1: 4066 B (RCA etc.)

I 2: MC 14568 B (Motorola)
I 3: MC 14526 B (Motorola etc.)
I 4: 7404 (TI etc.)
I 5: 74LS90 (TI etc.)
I 6 to I 8: 74LS390 (TI etc.)
D 1: BB 505 G (Siemens etc.)
D 2: 1N 4151 or similar
TCXO: Temperature-compensated crystal oscillator TEKO 10.000 kHz, Philips, Order-No. 4322 191 00001
Trimmer: 10 pF air-spaced trimmer, Johanson, type 5200

Some CMOS-circuits I 2 and I 3 will not be able to divide the 6.2 MHz signal by 62, which means that it is necessary to use a reference frequency of 3.1 MHz. In order to do this, it is necessary for diodes D 4 and D 5, as well as the filter comprising L 2 and the capacitor of 100 pF to be removed from the PC-board DJ3RV 007, as shown in **Figure 4a**, and be replaced by a wire bridge. The output signal at Pt 711 is then no longer sinewave, but slightly limited.

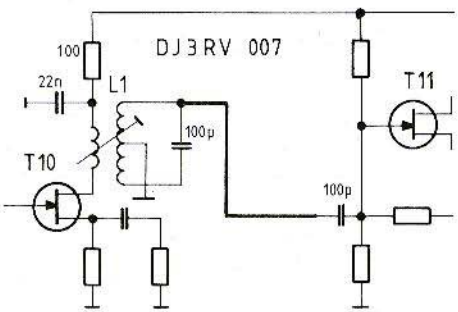


**Fig. 4a: Modification of the circuit DJ 3 RV 007 to obtain a 3.1 MHz reference signal**

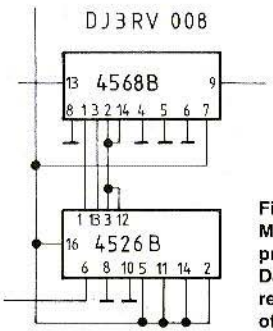


**Fig. 4b: Modification of the programming of board DJ3RV 008 for a reference frequency of 3.1 MHz**

It is now necessary for the dividers in I 2 and I 3 on PC-board DJ3RV 008 to be programmed to 31, as shown in **Figure 4b**.

The two dividers are connected in series and are binary coded. The lower four bits are set on I 3, and the upper four bits on I 2.

00011111 ≙ 31
00111110 ≙ 62

As can be seen with the given binary numbers, only two positions are changed. These are pin 5 of I 3 and pin 6 of I 2. These pins are still not wired on the board and must be programmed using the bridges!

Dividing by 62:
As given in circuit diagram Fig. 1:
Pin 5/I 3 to ground, and pin 6/I 2 to − 15 V

Dividing by 31:
Pin 5/I 3 to + 15 V, and pin 6/I 2 to ground.

In principle, it is possible for the divider circuit to be programmed for other reference frequencies, or division ratios if the conductor lanes on the PC-boards are modified as required. It is important that the reference frequency should be an even multiple of 100 kHz (at least 16 times), otherwise the divider in I 2 cannot be programmed when using the given circuit.

When using the module as a clock for a frequency counter, it is more favorable to increase the loop gain in the frequency control circuit of module DJ3RV 007. The modifications to the circuit are shown in **Figure 5**. Varactor diode D 2 is connec-

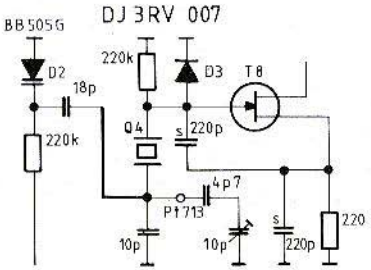


**Fig. 5: Increasing the pulling range of the crystal oscillator on DJ3RV 007**

ted to the hot end of crystal Q 4 via the 18 pF capacitor, and the series capacitor is reduced to 10 pF. The pulling range of the crystal will then be greater, however, the stability and noise behaviour will be slightly inferior. Holes and lines are provided on the PC-board for this modification.

## 3. CONNECTION AND ALIGNMENT

Connect the well stabilized operating voltages to Pt 801 and Pt 808. This is followed by connecting a 10 MHz TTL-signal to PT 805. The values given for the current drain are for orientation. With the control circuit switched off (Pt 802 to ground), the frequency of the TCXO should be aligned to exactly 10 MHz with the aid of the 10 pF trimmer. After switching on the control circuit, the frequency should remain phase-locked to the reference signal. The control can be checked at pin 2/l 1, if the frequency of the TCXO is temporarily shifted by touching pin 3.

The transcient behaviour of the control circuit is determined by the time constant of the filter links previous to diode D 1. In practical operation, a capacitor having a value of between 0.22 µF and 2.2 µF has been found suitable. The value of 0.47 µF given in the circuit diagram provides good results.

## 4. REFERENCES

1) F. Krug, DJ 3 RV
A Receiver for the VLF Time and Frequency Standard Transmissions from DCF 77
VHF COMMUNICATIONS 16, Edition 2/1984, Pages 96–114