7. Open-collector outputs are required whenever logic outputs are connected to a common point.

8. Several improved TTL families are available and continue to be introduced each year, providing decreased power consumption and decreased propagation delay.

9. The CMOS family uses complementary metal oxide semiconductor transistors instead of the bipolar transistors used in TTL ICs. Traditionally, the CMOS family consumed less power but was slower than TTL. However, recent advances in both technologies have narrowed the differences.

10. The BiCMOS family combines the best characteristics of bipolar technology and CMOS technology to provide logic functions that are optimized for the high-speed, low-power characteristics required in microprocessor systems.

11. Emitter-coupled logic provides the highest-speed ICs. Its drawback is its very high power consumption.

12. A figure of merit of IC families is the product of their propagation delay and power consumption, called the speed–power product (the lower, the better).

13. When interfacing logic families, several considerations must be made. The output voltage level of one family must be high and low enough to meet the input requirements of the receiving family. Also, the output current capability of the driving gate must be high enough for the input draw of the receiving gate or gates.

Glossary

BiCMOS: A logic family that is fabricated from a combination of bipolar transistors and complementary MOSFETs. It is an extremely fast low-power family.

Bipolar Transistor: Three-layer *N–P–N* or *P–N–P* junction transistor.

Buffer: A device placed between two other devices that provides isolation and current amplification. The input logic level is equal to the output logic level.

CMOS: Complementary metal oxide semiconductor.

Decoupling: A method of isolating voltage irregularities on the V_{CC} power supply line from an IC V_{CC} input.

Differential Amplifier: An amplifier that basically compares two inputs and provides an output signal based on the *difference* between the two input signals.

ECL: Emitter-coupled logic.

EMI: Electromagnetic interference. Undesirable radiated energy from a digital system caused by magnetic fields induced by high-speed switching.

Fall Time: The time required for a digital pulse to fall from 90% down to 10% of its maximum voltage level.

Fan-Out: The number of logic gate inputs that can be driven from a single gate output of the same subfamily.

Level Shifter: A device that provides an interface between two logic families having different power supply voltages.

MOSFET: Metal oxide semiconductor field-effect transistor.

NMOS: A family of ICs fabricated with *N*-channel MOSFETs.

Noise Margin: The voltage difference between the guaranteed output voltage level and the required input voltage level of a logic gate.

Open-Collector Output: A special output stage of the TTL family that has the upper transistor of a totem-pole configuration removed.

PMOS: A family of ICs fabricated with *P*-channel MOSFETs.

Power Dissipation: The electrical power (watts) that is consumed by a device and given off (dissipated) in the form of heat.

Propagation Delay: The time required for a change in logic level to travel from the input to the output of a logic gate.

Pull-Up Resistor: A resistor with one end connected to V_{CC} and the other end connected to a point in a logic circuit that needs to be raised to a voltage level closer to V_{CC}.

Rise Time: The time required for a digital pulse to rise from 10% up to 90% of its maximum voltage level.

Sink Current: Current entering the output or input of a logic gate.

Source Current: Current leaving the output or input of a logic gate.

Substrate: The silicon supporting structure or framework of an integrated circuit.

Totem-Pole Output: The output stage of the TTL family having two opposite-acting transistors, one above the other.

TTL: Transistor–transistor logic.

Wired-AND: The AND function that results from connecting several open-collector outputs together.

Problems

Section 9–1

9–1. What is the purpose of diodes D_1 and D_2 in Figure 9–1?

9–2. In Figure 9–1, when input *A* is connected to ground (0 V), calculate the approximate value of emitter current in Q_1.

9–3. In Figure 9–1, when the output is HIGH, how do you account for the output voltage being only about 3.4 V instead of 5.0 V?

9–4. In Figure 9–1, describe the state (ON or OFF) of Q_3 and Q_4 for

(a) Both inputs *A* and *B* LOW

(b) Both inputs *A* and *B* HIGH

Section 9–2

9–5. What does the negative sign in the rating of source current (e.g., $I_{OH} = -400\ \mu A$) signify?

9–6. For TTL outputs, which is higher, the source current or the sink current?

9–7. (a) Find V_a and I_a in the circuits of Figure P9–7 using the following specifications:

$I_{IL} = -1.6$ mA	$I_{IH} = 40\ \mu$A
$V_{IL} = 0.8$ V max	$V_{IH} = 2.0$ V min
$I_{OL} = 16$ mA	$I_{OH} = -400\ \mu$A
$V_{OL} = 0.2$ V typ	$V_{OH} = 3.4$ V typ

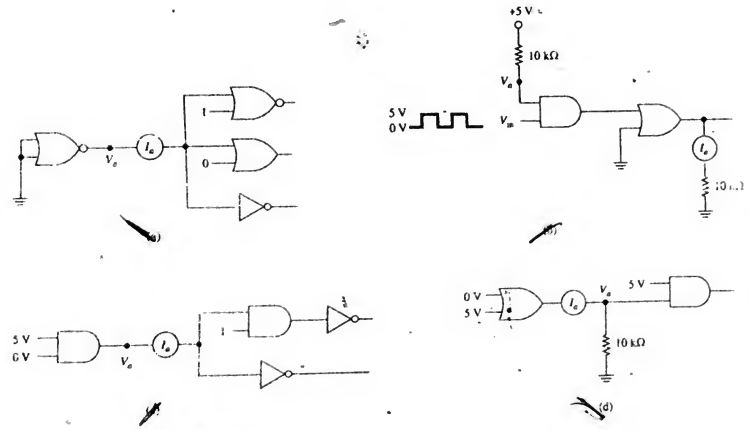

Figure P9–7

(b) Repeat part (a) using input/output specifications that you gather from a TTL data book, assuming that all gates are 74LSXX series.

Section 9–3

9–8. The input and output waveforms to an OR gate are given in Figure P9–8. Determine:

(a) The period and frequency of V_{in}

(b) The rise and fall times (t_r, t_f) of V_{in}

(c) The propagation delay times of (t_{PLH}, t_{PHL}) of the OR gate

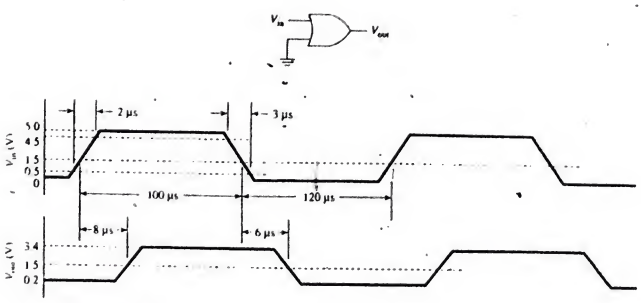

Figure P9–8

9–9. The propagation delay times for a 74LS08 AND gate (Figure P9–9) are $t_{PLH} = 15$ ns, $t_{PHL} = 20$ ns, and for a 7402 NOR gate, they are $t_{PLH} = 22$ ns, $t_{PHL} = 15$ ns. Sketch V_{out1} and V_{out2} showing the effects of propagation delay. (Assume 0 ns for the rise and fall times.)

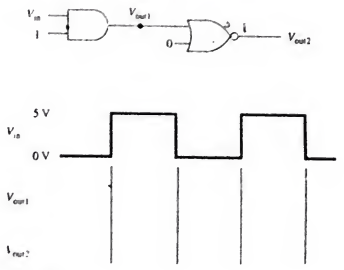

Figure P9–9

9–10. (a) Repeat Problem 9–9 for the circuit of Figure P9–10(a).

(b) Repeat Problem 9–9 for V_a, V_b, V_c, and V_d in Figure P9–10(b). (Use a TTL data book to determine the propagation delay times.)

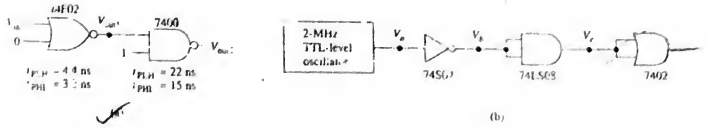

Figure P9–10

9–11. Refer to a TTL data book or the data sheets in Appendix B. Use the total supply current (I_{CCL}, I_{CCH}) to compare the power dissipation of a 7400 versus a 74LS00.

9–12. Refer to a TTL data sheet to compare the typical LOW-level output voltage (V_{OL}) at maximum output current for a 7400 versus a 74LS00.

9–13. (a) Refer to a TTL data sheet to determine the noise margins for the HIGH and LOW states of both the 7400 and 74LS00.

(b) Which has better noise margins, the 7400 or 74LS00?

9–14. (a) Refer to a TTL data sheet (or Appendix B) to determine which can sink more current at its output, the commercial 74LS00 or the military 54LS00.

(b) Which has a wider range of recommended V_{CC} supply voltage, the 7400 or the 5400?

9–15. Why is a pull-up resistor required at the output of an open-collector gate to achieve a HIGH-level output?

9–16. The wired-AND circuits in Figure P9–16 use all open-collector gates. Write the simplified Boolean equations at X and Y.

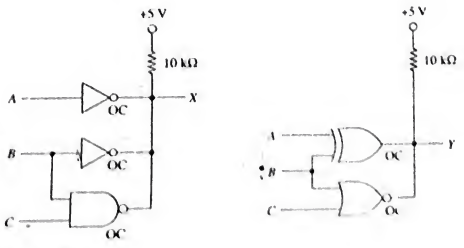

Figure P9–16

Sections 9–4 and 9–5

9–17. Make a general comparison of both the switching speed and power dissipation of the 7400 TTL series versus the 4000B CMOS series.

9–18. Which type of transistor, bipolar or field effect, is used in TTL ICs? In CMOS ICs?

9–19. Why is it important to store MOS ICs in antistatic conductive foam?

Sections 9–6 and 9–7

9–20. What is the principal reason that ECL ICs reach such high switching speeds?

9–21. Table 9–3 shows that the speed–power product of the 74ALS family is much better than the 100K ECL family. Why, then, are some large mainframe computers based on ECL technology?

9–22. The graph in Figure 9–24 shows the 4000B CMOS family in the opposite corner from the 100K ECL family. What is the significance of this?

9–23. Referring to Figure 9–25, which logic family dissipates less power at low frequencies, the 74LS or 74HC?

Section 9–8

9–24. (a) Using the data in Table 9–4, draw a graph of input and output specifications similar to Figure 9–26 for the 74HCMOS and the 74ALSTTL IC series.

(b) From your graphs of the two IC series, compare the HIGH- and LOW-level noise margins.

(c) From your graphs, can you see a problem in *directly* interfacing:

(1) The 74HCMOS to the 74ALSTTL?

(2) The 74ALSTTL to the 74HCMOS?

9–25. Refer to Table 9–4 to determine which of the following interfacing situations (driving gate-to-gate load) will require a pull-up resistor, and why?

(a) 74TTL to 74ALSTTL

(b) 74HCMOS to 74TTL

(c) 74TTL to 74HCMOS

(d) 74LSTTL to 74HCTMOS

(e) 74LSTTL to 4000B CMOS

9–26. Of the interfacing situations given in Problem 9–25, will any of the driving gates have trouble sinking or sourcing current to a single connected gate load?

9–27. From Table 9–4, determine:

(a) How many 74LSTTL loads can be driven by a single 74HCTMOS gate?

(b) How many 74HCTMOS loads can be driven by a single 74LSTTL gate?

Schematic Interpretation Problems

See Appendix G for the schematic diagrams.

9–28. Assume that the inverter U4-A in the Watchdog Timer schematic has the following propagation delay times: $t_{PHL} = 7.0$ nS, $t_{PLH} = 9.0$ nS. Also assume that WATCHDOG_CLK is a 10-MHz square wave. Sketch the waveforms at WATCHDOG_CLK and the input labeled CLK on U11-M on the same time axis.

9–29. Repeat Problem 9–28 with a 7404 used in place of the 74HC04. Assume that the 7404 has the following propagation delay times: $t_{PHL} = 15.0$ nS, $t_{PLH} = 22.0$ nS.