# Circuit Circus

# IC Logic Gates and Inverters

CHARLES D. RAKES

Over the years here at the *Circus*, we've shared a large number of circuits using the *C*omplementary *M*etal-*O*xide *S*emiconductor (CMOS) and *T*ransistor-*T*ransistor-*L*ogic (TTL, or T²L) line of integrated circuit logic gates. We've built oscillators, low-powered RF transmitters, speed-control circuits, light dimmers, stepper-motor controllers, and many other circuits using these versatile devices—but I don't recall ever taking the time to go over the basic functions and characteristics of these devices. Understanding just how each of the gates operates can make the job of troubleshooting much easier and make designing your own circuitry a real possibility. In this month's column, we'll take a look at the 7400 line of TTL logic gates and inverters and the 4000 family of CMOS gates and inverters, and we'll leave the newer series of gates for a later date.

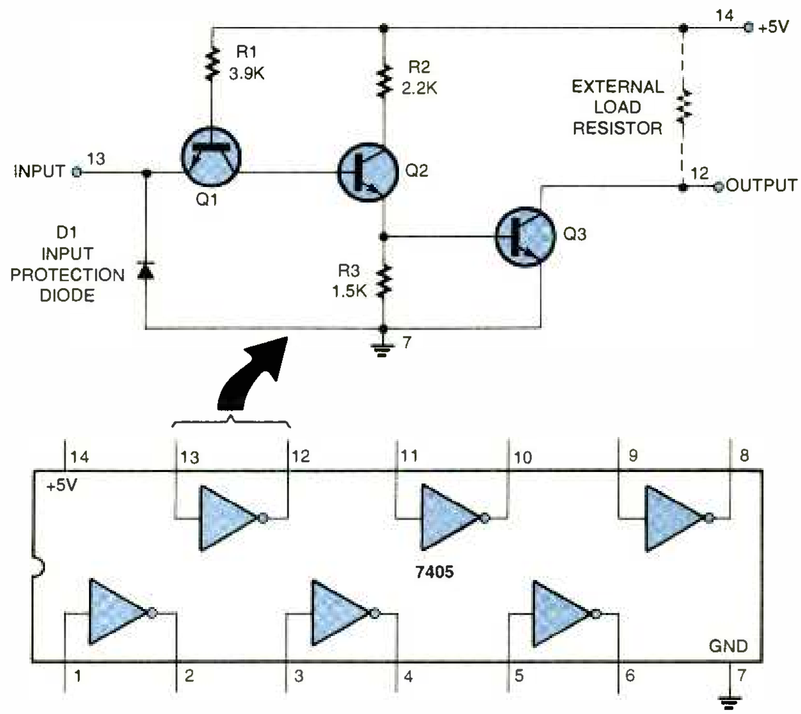



*Fig. 1. Circuit topology illustrating one of six open-collector inverter circuits in a typical open-collector hex inverter IC. Identifications of transistors, etc. are for reference only and do not represent discrete components.*

## THE 7400-TTL FAMILY

The 7400 family of TTL ICs has been around for about thirty years and is still going strong in many circuit applications. Most commercial TTL ICs in the 74XX family are useful over a 0° to 70°C operating environment. The one or two letters following the "74" indicate the special TTL family (if applicable), as follows: (74XX)—standard, or regular TTL, (74LXX)—low-power, (74HXX)—high-power, TTL (74SXX)—Schottky, (74LSXX)—low-power Schottky, *etc.* Which sub-family to select depends upon several design considerations, such as speed, power consumption, frequency of operation, and, of course, price and availability. The sub-family designation is then followed by a 2, 3, or 4-digit device-identification number. For example, a 74L04 is a low-power hex inverter (six inverters in one IC package).

Since these are digital gates, we only have to be concerned with a logic "1" (high) and a logic "0" (low) for their input/output levels. The ideal operating power-supply voltage for these devices is 5 volts, but they are designed to function with a supply of 4.5 to 5.5 volts. The ideal signal input low, or "0" logic level would be zero volts. However, in the real world this doesn't happen often, so a recommended maximum "LOW" voltage level is 0.8 volts. Any voltage above 0.8 volts and less than about 2 volts is considered a non-logic level and does not represent either a ""LOW-" or a "HIGH-" logic level. A typical ""LOW" for the TTL gate is about 0.1 to 0.4 volts.

The ideal "HIGH-"output logic level for a TTL gate would be 5 volts, but in reality the actual value will be somewhere between 3.0 to 4.5 volts—with a minimum allowable level of 2.5 volts. A typical "HIGH" output is about 4.0 volts.

A TTL gate supplies a maximum "HIGH-"(source) output current of 0.4 mA and a maximum ""LOW" (sink) current of 16 mA. The current requirement for single-gate input is only 40 µA when the input is "HIGH" and 1.6 mA when the input is ""LOW." Each TTL output can drive 10 input gates, which is referred to as the IC's fan-out capabilities.

A typical TTL open-collector inverter circuit is shown in Fig. 1. This is the equivalent circuit that makes up one of the six inverters in a 7405 hex inverter. A pull-up resistor must be tied to the open collector and the 5-volt source for the circuit to operate.

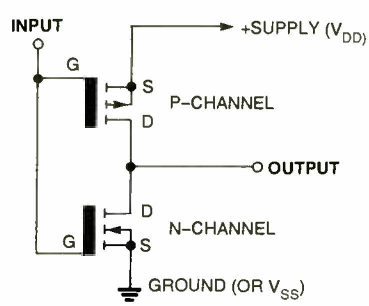
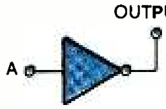



*Fig. 2. Schematic diagram of a CMOS device, consisting of a P-channel and N-channel enhancement-type MOSFET, fabricated on a single substrate.*

## THE 4000-CMOS FAMILY

The CMOS 4000 logic family is one of the most popular and user-friendly lines of digital ICs available to the experimenter. Like the TTL family, there are numerous subfamilies associated with CMOS devices. For simplicity CMOS sub-families are assigned numbers similar to the TTL-numbering system, with one to three letters indicating the sub-family and as many as five numbers indicating the specific device, as follows: (40XX)—standard CMOS; (74CXX)—CMOS version of TTL; (74HCXX)—high-speed CMOS; (74HCTXX)—high-speed CMOS, TTL-compatible, *etc*. For example, a 74HC04 IC is a high-speed CMOS hex inverter.

CMOS devices require very little operating power, and during standby almost no current is required. The supply voltage requirements are anything

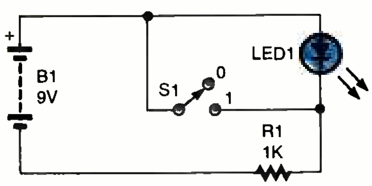



A

TRUTH TABLE

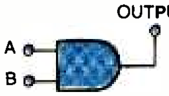
| A | OUTPUT |
|---|---|
| 0 | 1 |
| 1 | 0 |

B




C

*Fig. 3. In (A) is shown the logic symbol for an single inverter, with truth table in (B), and the resulting hard-wired equivalent in (C).*

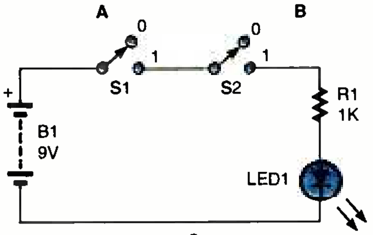



A

TRUTH TABLE

| A | B | OUTPUT |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

B




C

*Fig. 4. Here we have the* AND *logic symbol in (A) and its truth table representation in (B). The equivalent logic circuit is given in (C).*

but critical, allowing voltages of 3 to 16 volts to be used. The CMOS inputs require almost zero drive current because their input impedance is like an open circuit. Also, due to the wide range between the logic voltage levels, these devices offer excellent noise immunity.

Since the CMOS devices can operate over a wide voltage range, an exact digital-input "HIGH-" or "LOW-"voltage level can not be given. A logic-input "LOW" level is defined as any voltage less than 30% of the supply voltage. If the circuit is operating with a 10-volt supply, the maximum voltage for a logic "LOW" is about 3 volts. A logic input "HIGH" is any voltage greater than 70% of the supply voltage, and with a 10-volt supply the minimum logic "HIGH-"voltage level would be 7 volts. The output "HIGH-"logic voltage level rises to about 99% of the supply voltage, and the "LOW-"logic level drops to near-zero volts or circuit ground.

There are several CMOS characteristics that can be disadvantages in some circuit designs, and the following points should be remembered. CMOS devices are slower than similar devices in the TTL family, with propagation delays in some devices as high as 100 ns. Static discharge can kill any CMOS device with a single strike, so extra care must be taken in handling. All unused CMOS inputs must be tied to either ground or battery positive; and if any are left open, strange things will happen. Always check all inputs and make sure they go somewhere. Use a grounded soldering iron when installing a CMOS IC on a circuit board.

## CMOS-COMPLEMENTARY MOSFET PAIR

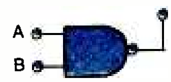
Figure 2 illustrates a typical CMOS-complementary MOSFET pair that is found in the basic 4000 IC family. Two enhancement-mode MOSFET transistors are connected across the power source with the P-channel device connecting to the positive source and the N-channel to circuit ground.

Taking the input to positive supply turns on the N-channel MOSFET (P-channel is off) and sets the output to about zero volts, giving a "LOW" output. With the input at ground, the P-channel MOSFET turns on (N-channel is off) and brings the output up to the source voltage, producing a "HIGH" output. The output is the opposite of the input, as in an inverter stage.

## LOGIC NOT GATES

The logic gate, no matter what IC family, is the basic building block for all digital circuitry. The simplest of all logic gates is the NOT gate or inverter. Figure 3A shows the schematic symbol for a NOT gate or inverting buffer. The truth table in Fig. 3B indicates that a logic low at the gate's input produces a logic-high output, and a logic-high input results in a logic-low output. Figure 3C shows an equivalent hard-wired circuit that will help you understand the logic. If switch S1 is in the "0" position, the LED is lit or on. Moving the switch to the "1" position turns the LED off.

The 4049 hex-inverting buffer and the 4050 hex non-inverting buffer are two very popular CMOS ICs that exhibit the NOT function. Each buffer, operating from a 5-volt supply, can fan out to drive two TTL-input gates.

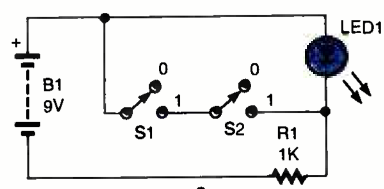



A

TRUTH TABLE

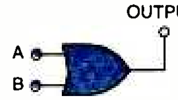
| A | B | OUTPUT |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

B




C

*Fig. 5. The versatile* NAND *circuit is shown symbolically in (A), with truth table in (B), and an equivalent configuration in (C).*

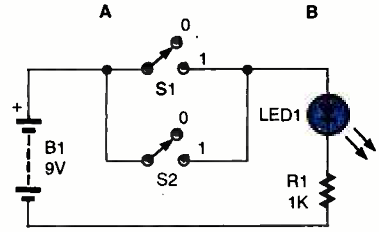



A

TRUTH TABLE

| A | B | OUTPUT |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

B




C

*Fig. 6. Here we have the* OR *logic symbol in (A) and its truth table representation in (B). The equivalent logic circuit is given in (C).*

## LOGIC AND GATES

The next gate we're going to look at is the two-input AND gate that is shown in Fig. 4A. Let's compare the logic results defined in the truth table of Fig. 4B to the operation of the equivalent circuit in Fig. 4C. It is obvious that both switches, S1 and S2, must be closed to turn the LED on. Any other combinations of inputs will not give a "HIGH" output. In an AND gate, all inputs must be high before a high output will occur—any other combination of inputs only produces a logic-low output. The 4081 IC is a typical quad 2-input AND gate.

## LOGIC NAND GATES

Figure 5 shows a NAND gate, which actually is an AND gate with an inverter connected to its output. Compare the AND gate and the NAND gate truth tables, and you will see what I mean. In a NAND gate, *all* inputs must be logic high to produce a logic-low output. Any other input combinations produce a logic-high output. Check out the equivalent logic circuit in Fig. 5C, and you can prove this to yourself. To turn on the LED (logic high), either/both switches must be opened ("0" position). A 4011 IC is a typical quad 2-input NAND gate.

## LOGIC OR GATES

Next on the list is the OR gate. The OR gate symbol is shown in Fig. 6A, along with the truth table in Fig. 6B, and the equivalent logic circuit in Fig. 6C. All inputs of an OR gate must be logic low to produce a logic-low output. Any other input combination will produce a logic-high output. If any input is logic high, the output also is a logic high (LED lit in Fig. 6C). The 4071 IC is a typical quad 2-input OR gate.

## LOGIC NOR GATES

The NOR gate, see Fig. 7, is nothing more than an OR gate with an inverter connected to its output. Compare the OR and NOR truth tables, and you'll see that this is true. All inputs of a NOR gate must be logic low to produce a logic-high output. All other input combinations will only produce a logic-low output. Check out the equivalent circuit in Fig. 7C, and you can prove the truth table true. If either/both S1 or S2 are closed, then the LED cannot go on. A 4001 IC is a typical quad 2-input NOR gate.

## LOGIC AND, OR, AND NOR GATES

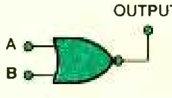
We have just covered the five most valuable and often-used gates in digital circuitry. Look these over and see if you can determine which of the five gates can easily be used to make any and all of the remaining four gates. Here's a hint. The most popular and often-used gate is the NAND gate. Now take a look at the four gates in Fig. 8—all are made up out of standard NAND gates.

Our first constructed gate is the NOT gate in Fig. 8A. To turn a NAND gate into a NOT gate or an inverter, just tie the two inputs of gate1 and gate2 together and apply the common input. If a non-inverting buffer is needed, just cascade another NAND gate.

Moving on to the AND gate shown in Fig. 8B, this development uses two standard NAND gates, gate1 and gate2, connected in series to form an AND gate. Go back to the truth table in Fig. 4B. All gates in an AND gate must be high to produce a logic-high output. If inputs "A" and "B" (in Fig. 8A) are logic high, its output at gate1 is low. This logic low is inverted by the second NAND gate, gate2, which produces a high output. Inputs high/output high equals an AND gate.

The OR gate, see Fig. 8C, is made up of three NAND gates. gates1 and 2 are connected in an inverter configuration with their outputs driving the inputs of gate3. Go back and look at the OR gate's truth table in Fig. 6B, and we see how the constructed OR gate operates. All inputs of the OR gate must be a logic low to produce a logic-low output. If we connect inputs "A" and "B" (in Fig. 8C) to ground (low), the output of the two

*(Continued on page 58)*

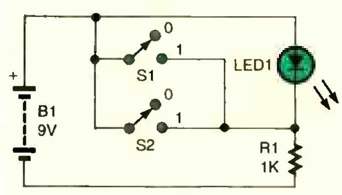



A

TRUTH TABLE

| A | B | OUTPUT |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

B




C

*Fig. 7. The logic symbol of a NOR circuit is shown symbolically in (A). The truth table is defined in (B), while the circuit in (C) represents the NOR operation.*

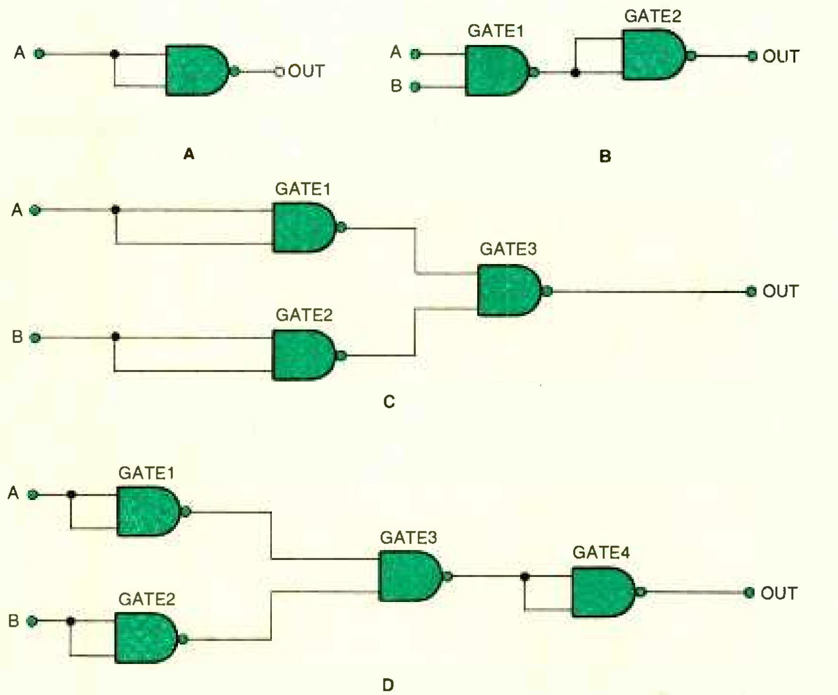



*Fig. 8. This sequence of circuits shows how NAND circuits are the "building blocks" of other common logic circuits. Tying the two inputs of a single NAND gate together is used in (A) to define an inverter operation (or NOT logic). Two series-connected NAND gates are used to make up the AND gate of (B). The OR gate of (C) can be constructed with three NAND gates, two of which are paralleled as inverters and series-connected to a third NAND gate. The NOR gate of (D) is constructed with the OR gate circuit of (C), but with a NAND-inverter added at its output.*

## PARTS LIST FOR THE AUDIO Q-MULTIPLIER

**SEMICONDUCTORS**
D1, D2—1N60, germanium, general-purpose diode
IC1—LF351 low-noise, JFET-input, op-amp, integrated circuit (NTE857M, or equivalent)
IC2—LM386 low-voltage, audio-power amplifier, integrated circuit (NTE823, SK9210, or equivalent)
IC3—7824 fixed, 24-volt, 1-amp, regulator, integrated circuit (NTE972, SK3670, or equivalent)
IC4—7812 fixed, 12-volt, 1-amp, regulator, integrated circuit (NTE960, SK3592, or equivalent)
Q1—3N140 dual-gate MOSFET (NTE221, Thomson SK3065, or equivalent)

**RESISTORS**
(All fixed resistors are $\frac{1}{4}$-watt, 5% units.)
R1, R15—1-megohm
R2, R10—100,000-ohm
R3—6800-ohm
R4—1200-ohm
R5, R6—240,000-ohm
R7—250,000-ohm, linear-taper potentiometer
R8—1-megohm, linear-taper potentiometer
R9—500,000-ohm, audio-taper potentiometer
R11, R13—1000-ohm
R12—560-ohm
R14—5000-ohm, trimmer potentiometer
R16, R17—4700-ohm
R18—10-ohm

**CAPACITORS**
C1, C11—0.05-µF, ceramic-disc
C2, C15, C17—10-µF, 16-WVDC, electrolytic
C3, C8, C9, C16—0.1-µF, ceramic-disc
C4, C5—620-pF, ceramic-disc
C6—1000-pF, ceramic-disc
C7—2000-pF, ceramic-disc
C10—50-µF, 35-WVDC, electrolytic
C12, C19—220-µF, 16-WVDC, electrolytic
C13—500-µF, 35-WVDC, electrolytic
C14—0.005-µF, 500-WVDC, ceramic-disc
C18—100-µF, 35-WVDC, electrolytic

**ADDITIONAL PARTS AND MATERIALS**
BR1—1-amp, 100-PIV, full-wave bridge rectifier (*RadioShack* 276-1152, or equivalent)
J1—Phone jack
S1—SPST switch (part of R9)
SPKR1—8-ohm speaker
T1—25.2-volt AC, 450-mA, standard power transformer (*RadioShack* 273-1366, or equivalent)

**NOTE**: Transistor Q1, and the ICs and diodes, are available from *DC Electronics*, P.O. Box 3203, Scottsdale AZ 85257; Tel: 800-467-7736 or 800-423-0070.

Use the minimum amount of receiver signal necessary to obtain a clean output tone. Excessive receiver output will cause the circuit to generate noise bursts. If you want to connect headphones at the circuit's output, connect an 8.2- to 10-ohm, 1-watt resistor from the output (negative end of C12) to ground.

Keep in mind that the Q-multiplier cannot eliminate all QRM. If you are monitoring a CW signal with a tone around 1 kHz and the interfering signal has a tone near 800 Hz, there will be little suppression of the interfering signal. The Q-multiplier works best at suppressing a signal that is at least double the frequency of the desired tone.—*Craig Kendrick Sellen, Waymart, PA*

*Fine circuit, Craig; this project should be useful to every ham and SWL.*

That's about it for this month's column. Remember—this is **your** column—keep those circuits, solutions, and ideas coming in. Besides the fame of seeing your circuit in print, for each circuit that appears, you will receive a special gift.Write me—Alex Bie, *Think Tank*, **Popular Electronics**, 500 Bi-County Blvd., Farmingdale, NY ■

## CIRCUIT CIRCUS

*(continued from page 53)*

gates is high. Both inputs of gate3 are also high, producing a logic-low output, as in a standard OR gate.

Our last constructed gate is the NOR gate shown in Fig. 8D. If we just think about it for a minute, we can save some logic tracing by briefly going back and looking at the description of the NOR gate. The NOR gate is an OR gate with an inverter connected to its output. Therefore, gate4, in Fig. 8D, simply inverts the output of the OR gate of Fig. 8C, turning it into a NOR gate.

Any time in the future when you are breadboarding a new circuit and find that you are short an OR, NOR, AND, or NOT gate, scratch around in the junk box and see if you can find a NAND gate and continue on. I also hope that the basic logic-gate information we covered here will be helpful as well.

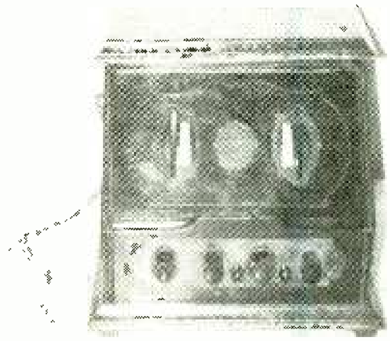
It's time to close for now—see you here again next month, same station, same time—logically speaking!

Comments? Via e-mail at cdrakes@ipa.net, or snail-mail at P.O. Box 445, Bentonville, AAR 72712, ■

## ANTIQUE RADIO

*(continued from page 50)*

same (2 volts at 0.06 amps DC) filament supply because I substituted 30-series tubes for the originals in both radios. Other battery sets I might want to operate could have 01-A tubes (whose filaments require 5 volts at 0.25 amps) or X199s (3.3 volts at 0.06 amps).



*Newly-minted cabinet for the* Radiola 20 *is very similar in style to the original. Power-supply circuit card can be seen at left.*

Accordingly, I decided to put together a universal-battery substitute, which has a female-edge connector as its output. The circuit cards on the *A-K 32* and *Radiola 20* are equipped with male-edge connectors to mate with that female, and they have resistor networks to adjust the voltages, as necessary, for the particular set. In order to demonstrate either set, I slip the relevant edge connector into the output connector on the power supply and away we go.

*Vic has supplied excellent documentation for his ingenious power-supply scheme, so we'll turn the column over to him again next month and go on with his letter. See you then!—Ellis* ■