Coherent Carrier Regeneration Using a Long Loop PLL Technique

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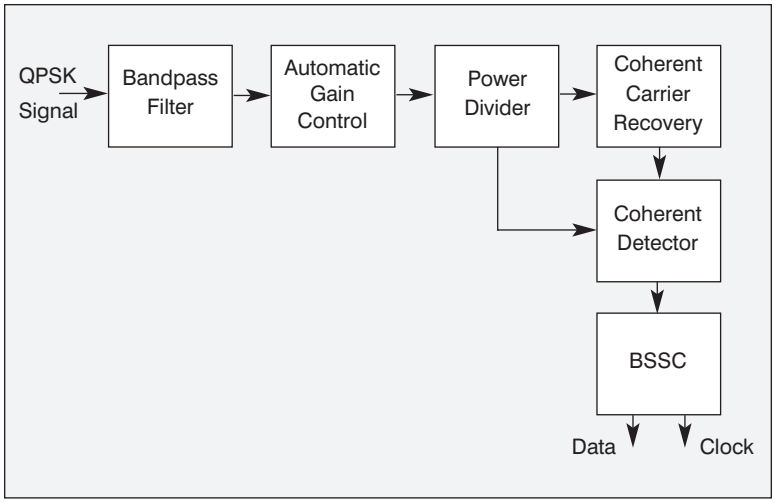
Demodulation of QPSK modulated data involves the regeneration of the coherent carrier in a phase lock loop. Various schemes are used for this purpose in designing the demodulators for tracking and receiving very high data rate signals from remote sensing satellites. A concept implementing the long loop carrier tracking phase lock loop technique is described here, which is used for carrier recovery in the demodulator. The unit has been successfully developed and tested in the ground station. This concept has facilitated a significant improvement in the loop performance for signal acquisition at very low signal to noise ratios. Signal acquisition and data retrieval at very low antenna elevation angles while tracking low altitude satellites has been achieved through this scheme.



■ **Figure 1. QPSK demodulator for remote sensing satellite data reception.**

Introduction

The design of the coherent carrier recovery circuit for the demodulation of suppressed carrier PSK signals is very critical and involves several performance considerations. Various carrier regeneration schemes have been developed and implemented in this demodulator design for optimal performance, in different applications.

A scheme implementing the long loop carrier tracking phase lock loop along with even law non-linearity has been developed and used for the design of a very high data rate QPSK demodulator to receive data from remote sensing satellites. This scheme has provided better lock threshold performance and loop stability in regenerating the coherent carrier for low input signal to noise ratios at different QPSK modulated data rates, when compared to conventional techniques.

The demodulator using this technique acquires the lock and starts regenerating the coherent carrier at very low input S/N ratios, a feature very useful in remote sensing satellite ground station applications where a coherent continuous clock is required to be supplied to the recording system, even from antenna angles lower than 1 degree in elevation.

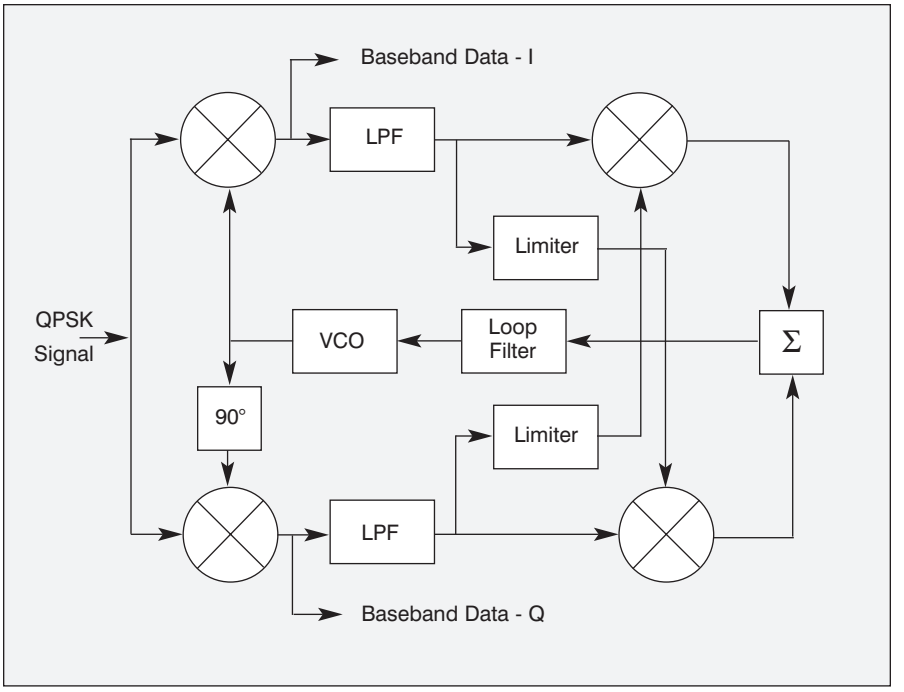
This paper describes the design of the QPSK demodulator using the long loop coherent carrier regeneration scheme, and shows the merit of its performance while demodulating the QPSK signals at different data rates and varying signal to noise ratios.

Measured results regarding the unit's coherent carrier acquisition performance are tabulated and a comparison is provided with the theo-

retically computed values. A comparison is also provided with the performance of demodulators designed using other techniques.

Configuration of the QPSK demodulator

The configuration of the demodulator used for the remote sensing satellite data is shown in Figure 1. The input QPSK modulated signals are bandpass filtered in a broadband filter and given to a non-coherent AGC amplifier. The constant level signals from the AGC amplifier are power divided into two paths. One path goes to the coherent carrier recovery circuit and the other path goes to the coherent data detector. The I and Q data streams from the coherent data detector are then input to the bit synchronizer and signal conditioner unit, where the coherent symbol timing is recovered and the data is synchronized to the symbol timing clock. The outputs of this circuit are the required serial data and bit rate clock.



■ **Figure 2. Hard limited Costas loop.**

The input broadband bandpass filter passes the QPSK modulated signals with proper out of band rejection. The automatic gain control circuit is a non-coherent AGC in order to assure that its transient behavior is not a function of carrier regeneration acquisition time.

The coherent carrier recovery circuit employs nonlinear squaring devices and a phase lock loop to regenerate the coherent suppressed carrier from input modulation. This circuit is designed for handling a wide range of input data rates on QPSK modulation without significant performance degradation. This feature has enabled the demodulator to be adaptable for multi-satellite data reception in one unit with only a plug in change required for bit synchronization [1].

The coherent data detector extracts the in phase (I) and quadriphase (Q) data streams and lowpass filters them to isolate the carrier component. Proper care has been taken in this circuit to avoid the crosstalk between the I and Q channels by using circuit elements with very good amplitude and phase balance specifications and by compensating for the phase mismatch between the modulated input and the regenerated carrier.

The bit synchronizer circuit has input matched filters which are symbol rate specific, to optimize the signal to noise ratio of the data streams before synchronization. The symbol timing is generated through an even law nonlinearity coupled with a phase lock loop. The recovered symbol clock estimates the data pulses, and the synchronized parallel data streams are differentially decoded for resolving the carrier phase ambiguity. The decoded data are serialized and taken as output of the unit.

Design options for carrier recovery

The crucial circuit element which decides the performance of the demodulator is the coherent carrier regeneration circuit. Several schemes are developed for coherent carrier regeneration, among which are the following design options discussed in this paper.

1. Carrier recovery through Costas loop.
2. Carrier recovery through multiplication loop.

Implementation of the Costas loop

Hard limited Costas loop or polarity loop is one of the popular approaches used in the demodulation of QPSK signals [2]. This technique is unique in that it performs both phase coherent suppressed carrier reconstruction and synchronous data detection within the loop. Figure 2 shows the implementation of the polarity loop for a QPSK demodulator.

For any carrier tracking analysis, the description of the linear PLL model is inevitable [3]. Out of this work, a fundamental expression relates the root mean squared phase error to the *SNR* in the loop:

$$\sigma_\phi^2 = \frac{1}{\rho_L}(\text{rad})^2 \qquad (1)$$

where $\rho_L = SNR$ in the loop. Or,

$$\sigma_\phi^2 = \frac{1}{(S/N)i} \cdot \frac{B_L}{B_i} \qquad (2)$$

where:

$(S/N)i$ = input signal to noise ratio.
B_L = one sided loop band width
B_i = one sided IF band width (arm filter band width)

The above relation concerns the carrier referencing for unmodulated or non-coherent modulation inputs.

The tracking performance of a suppressed carrier loop is analyzed by another relationship involving squaring loss S_L:

$$\sigma_\phi^2 = \frac{1}{\rho_L S_L} \tag{3}$$

The squaring loss describes the degradation in loop *SNR* due to *S*×*N* and *N*×*N* distortions occurring in the non linearity in carrier regeneration. This depends upon the shape of the arm-filter, the data waveform and the operating E_b/N_0.

Much work has been done in estimating the squaring loss. Simon [4] has derived a closed form expression for squaring loss which is shown as

$$S_L = \frac{D_m}{K_d + K_L \dfrac{B_i / f_s}{2R_d D_m}} \tag{4}$$

where:

D_m = modulation distortion factor
f_s = Data rate in symbols/sec
R_d = Symbol signal to noise ratio
K_L= a constant dependent upon the filter type and can be written as:

$$K_L \cong \frac{\int_{-\infty}^{\infty} \left|\widetilde{H}_c(w)\right|^4 dw}{\int_{-\infty}^{\infty} \left|\widetilde{H}_c(w)\right|^2 dw}$$

where $\widetilde{H}_c(w)$ is the filter transfer function. It is also shown that

K_L = (2n – 1)/2n for an n-pole Butterworth filter
K_d = a constant dependent upon both baseband data power spectrum and the filter type. This can be written as

$$K_D \cong \frac{\int_{-\infty}^{\infty} S_m(w)\left|\widetilde{H}_c(w)\right|^4 dw}{\int_{-\infty}^{\infty} S_m(w)\left|\widetilde{H}_c(w)\right|^2 dw}$$

where $S_m(w)$ represents the data power spectrum.

The effects of signal suppression due to hard limiting is also introduced into the above expression for squaring loss. Simon [2] has shown that inclusion of a limiter introduces a signal suppression factor into the analysis which can affect the loop performance. For higher E_b/N_0 ratios (E_b/N_0 >10 dB), there is an actual improvement in the loop's squaring loss while, at low *S*/*N* ratios, the limiter degrades the loop performance. The expression for the squaring loss has also been derived in terms of E_b/N_0 [5] and written as:

$$S_L = \left[\frac{h_1}{\alpha} + \frac{h_2 T_b / \alpha}{2E_b / N_0}\right]^{-1}$$

where

T_b = Bit duration

$$\alpha = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_m(w)\left|\widetilde{H}_c(w)\right|^2 dw$$

$$h_1 = \int_{-\infty}^{\infty} S_m(w)\left|\widetilde{H}_c(w)\right|^4 dw$$

$$h_2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|\widetilde{H}_c(w)\right|^4 dw$$

where

$H_c(w)$ = Low pass equivalent of the input bandpass filter transfer function.
$S_m(w)$ = Spectrum of the modulated signal.

Also, incorporating input E_b/N_0 into the equation (3), we get:

$$\sigma_\phi^2 = \frac{B_L}{E_b / N_0 \cdot f_s \cdot S_L} \tag{5}$$

where

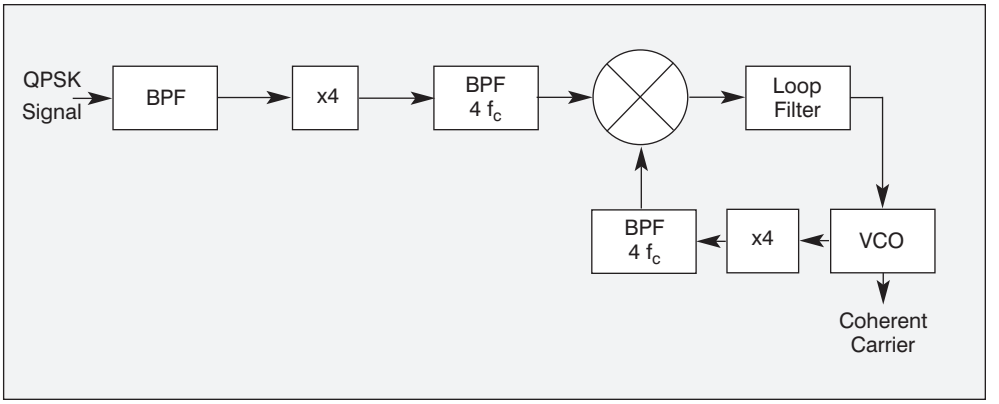
σ_ϕ^2 = Max. allowable RMS phase jitter (rads).
E_b/N_0 = Energy per bit to noise density ratio required for desired bit error rate performance.

Having calculated the loop squaring loss, and knowing the required *SNR* in the loop, RMS phase jitter in the recovered carrier is calculated.

Implementation of multiplication loop

The explanation of this technique is similar to the Costas loop, as both are identical in performance [6]. The difference in the scheme is in the implementation of the non-linearity for modulation wipe-off as shown in Figure 3. The received QPSK signal plus noise is filtered and passed through the fourth power non-linearity. The output after the non-linearity is given to a phase locked loop which locks to the fourth harmonic of the received carrier. The signal × noise and noise × noise distortions occuring in the carrier regeneration loop are controlled

mainly by the excess noise bandwidth in the input bandpass filter preceding the squaring devices. The jitter in carrier referencing is hence determined by the characteristics of this bandpass filter. Layland [7] has proposed an optimum squaring loop filter considering the various factors contributing to squaring loss. However, design of the arm filters, or prefilters to the squaring devices, need not be on the lines of matched filtering for optimizing the data signal-to-noise ratio used before data estimation in bit and symbol timing synchronizers. The jitter or the *SNR* in the phase lock loop, and the static phase error in the regenerated carrier, are some of the degradation factors which contribute to overall losses in data detection. Smith A. Rhodes [8] and V. K. Prabhu [9] have calculated the QPSK losses due to imperfect carrier synchronization and plotted the curves of detection performance for QPSK as shown in Figure 4. The loss in detection is derived as:



■ **Figure 3. Carrier recovery by a multiplication loop.**

$$L(\text{dB}) = \frac{4.34}{\rho_L}\left[(1+2\gamma)\left(1+\frac{(1+2\gamma)}{2\rho_L}\right)\right]$$

ρ_L = SNR in the loop

$\gamma = Z^2 \cdot E_b / N_0$

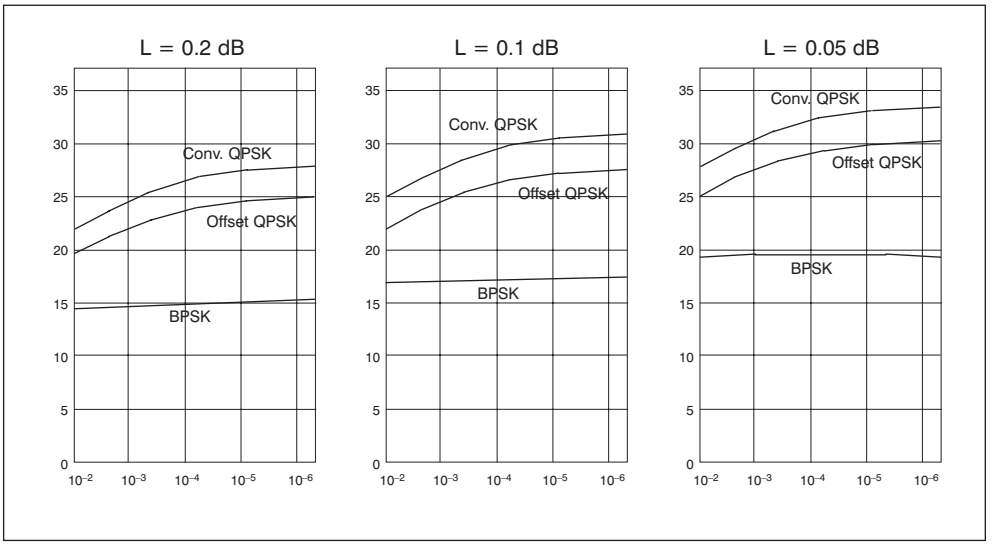
Z^2 = effective loss in E_b/N_0 caused by synchronization error ϕ.

The plots show the values of the required *S*/*N* ratio in the phase lock loop for given bit error rate performance at different detection loss (*L* dB) values. It is seen from the above equation and the plots that to keep the detection losses to a minimum and achieve bit synchronization for lower values of loop *SNR*, it is essential to reduce the jitter in carrier referencing and minimize synchronization errors.

Coherent carrier regeneration by the long loop method

The squaring loop and Costas loop explained above have been considered for fixed data rate input signals. In cases where the demodulator has to be designed to be adaptable to signals with varying input data rates, the effects of the excess noise bandwidth of the pre-filter or arm filter before squaring will be quite significant. While the pre-filter bandwidth has to be optimized for highest baud rate input signal, the signals with lower data rates face severe reduction in signal-to-noise ratio in the wider pre-filter. Also, at the lower antenna elevation angles (less than 5 degrees), the signal reduction due to path loss and terrain reflections causes further degradation in input *S*/*N* ratio to the carrier regeneration nonlinearity. All these effects put together will reduce signal-to-noise ratio in the loop, thus resulting in a requirement for higher system link margin for carrier lock acquisition.

One could use a narrow band pass filter to improve the *S*/*N* ratio at the input of PLL in a short loop configuration, but this would face minimum bandwidth limitation posed by the very high input Doppler offsets on the received signal while tracking low earth orbiting satellites. The Doppler offset for some circular orbits may be as high as 400 kHz. This results in the requirement that the pre-PLL filter passband response be flat at least over ±2 MHz, resulting in a noise bandwidth



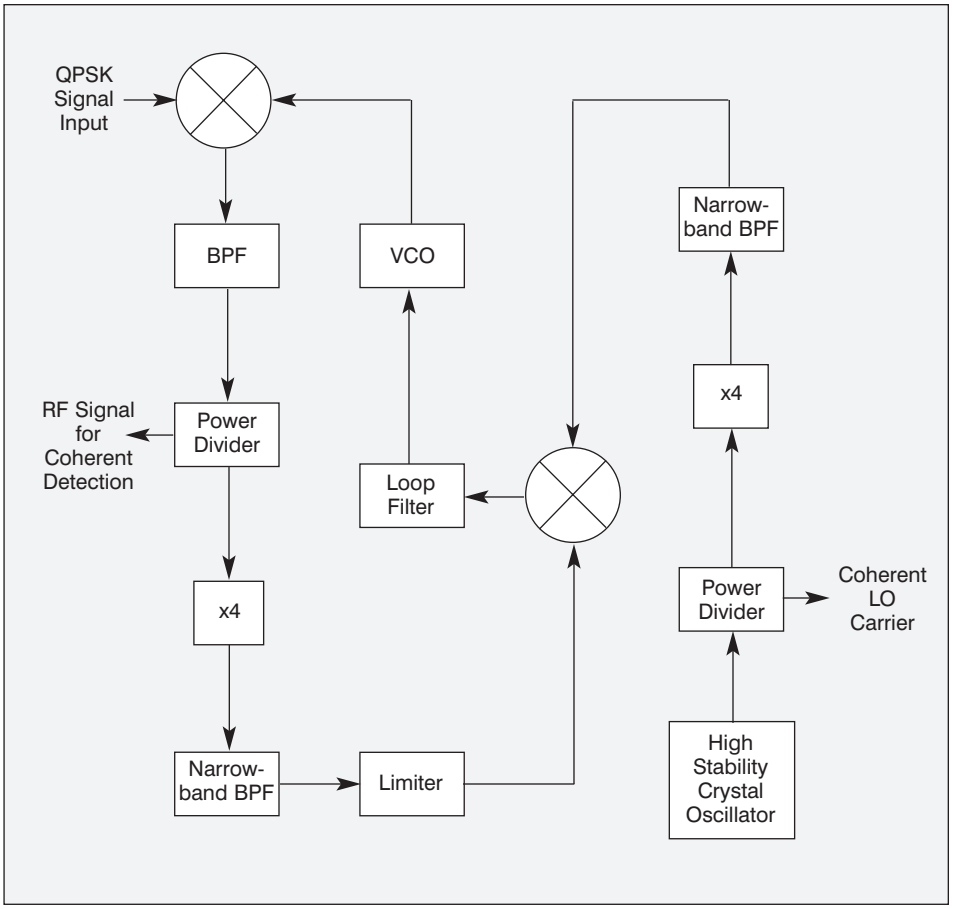
■ **Figure 4. Loop *SNR* (vertical scale = 10 log[ρ_L]) versus bit error rate (horizontal scale) at different detection loss values (L).**

much larger than that.

In order to maintain the pre-PLL filter noise bandwidth at the minimum possible, carrier regeneration using a long loop phase lock scheme has been implemented and the demodulator has been successfully developed.

The long loop technique for coherent carrier regeneration from a QPSK modulated signal is described with the help of Figure 5. The received modulated QPSK signal is passed through an automatic gain control circuit to provide a constant output level independent of the larger signal level variations at the input. The input modulated RF signal is mixed with a VCO signal in the carrier referencing phase lock loop to provide an IF signal. The IF signal is then passed through the bandpass filter with the bandwidth that is selected optimally for minimum squaring loss for the highest input baud rate.

The filtered signal is then passed through the non-linearity to remove the modulation. The fourth harmonic component of this IF carrier frequency is then filtered through a very narrow bandpass filter, with the bandwidth as small as possible and the signal always centered at a fixed frequency. The output from the BPF is then phase locked with the ×4 multiplied component of a very highly stable crystal oscillator source. The crystal oscillator source frequency is centered at the IF carrier frequency and becomes the coherent carrier reference for data detection after phase locking. The source frequency after multiplication is passed through a bandpass filter with identical characteristics as the one which is in the signal path at the input of the PLL. This ensures the correct phase referencing in the phase lock loop.



■ **Figure 5. Coherent carrier regeneration by the long loop method.**

The PLL tracks the Doppler frequency variations of the input signal by correcting the VCO output frequency accordingly, while maintaining the IF output of the mixer at a constant frequency. The mixer output is power divided, with one portion fed to the coherent detector for data demodulation and the other portion fed to the loop. The VCO is swept for initial signal acquisition and is designed for acquiring the signal with a Doppler shift as high as +500 kHz.

Tabulation & Results

Improvement of the lock threshold performance of the phase lock loop, in a long loop configuration with a narrowband filter, has been analyzed with the help of the following equation (6). The equation relates the $(S/N)i$ in the narrow band pre-PLL filter to the input carrier-to-noise ratio in the pre-filter prior to the nonlinearity [10, 11]:

$$(S/N)i = \frac{(1/16)(B/B_N)(C/C_N)}{1+4.5(C/N)^{-1}+6(C/N)^{-2}+1.5(C/N)^{-3}} \qquad (6)$$

where

B = Noise bandwidth of pre-filter to the nonlinearity
B_N = Noise bandwidth of the narrowband pre-PLL filter

The results in terms of threshold loop SNR have been tabulated for different lock threshold E_b/N_0 values at different data rates in Table 1. The results are also plotted in Figure 6.

The theoretically computed results are cross checked with measured values and found to be matching. However, the values deviate slightly from the theory, due to the implementation margin of the modulator at the higher data rates.

For measurement of $(S/N)i$, signal to noise density

Data Rate	Lock Threshold E_b/N_0	Lock Threshold C/N_0 measured at PLL input (output of narrowband filter)	$(S/N)i$ & SNR_L with measured value of C/N_0 at PLL input		$(S/N)i$ & SNR_L calculated theoretically with eqns. (6) and (7)	
(Mbps)	(dB)	(dB-Hz)	$(S/N)i$ (dB)	SNR_L (dB)	$(S/N)i$ (dB)	SNR_L (dB)
6	12.72	57	-10	7	-9.9	7.1
10	10.5	57	-10	7	-9.9	7.1
20	8.0	58	-9	8	-8.7	8.3
30	6.2	58	-9	8	-8.7	8.3
40	5.0	58	-9	8	-8.7	8.3
50	4.5	59	-8	9	-7.4	9.6
60	3.7	59	-8	9	-7.4	9.6
70	3.1	59	-8	9	-7.4	9.6
80	2.5	59	-8	9	-7.4	9.6
90	2.0	59	-8	9	-7.4	9.6
100	1.5	59	-8	9	-7.4	9.6
105	1.3	59	-8	9	-7.4	9.6

Notes:
1. Noise Bandwidth of the pre filter to multiplier = 116.14 MHz
2. Noise Bandwidth of the pre-PLL narrowband filter = 5.04 MHz
3. PLL loop Noise Bandwidth = 100 kHz

■ **Table 1. Results with pre-PLL narrowband filter.**

ratio S/N_0 at the input of the narrow band filter is measured, and $(S/N)i$ is computed by dividing the S/N_0 ratio with the noise bandwidth of the filter. The noise bandwidth of both filters is measured with the help of a broadband white Noise Generator with a known noise power density.

For each measured value of $(S/N)i$ at the input of the phase lock loop or at the output of the narrowband pre-filter, the signal to noise ratio in the loop $(SNR)_L$ is calculated by:

$$SNR_L = \frac{(S/N)i \cdot B_n}{B_L} \tag{7}$$

where B_n and B_L correspond to the noise band width of pre-PLL filter and PLL loop band width respectively. These results are also included in Table 1. The results in Table 1 can be compared with the results tabulated in Table 2 obtained by directly computing the $(SNR)L$ with the help of equation (6), the case where no pre-PLL filter is incorporated, or where the Costas loop is used for carrier recovery.

These results are also plotted in Figure 6. It can be seen from the plots that there is an

Data Rate	Lock Threshold E_b/N_0 at input of pre-filter to non-linearity	Lock Threshold C/N_0 measured at PLL input	Threshold loop SNR_L calculated from the measured value of C/N_0 at PLL input	Threshold loop SNR_L calculated from eqn. (6) directly
(Mbps)	(dB)	(dB-Hz)	(dB)	(dB)
6	15.7	64	14	14.3
10	13.5	64	14	14.3
20	10.5	64	14	14.3
30	9.2	65	15	15.4
40	8.0	65	15	15.4
50	7.0	65	15	15.4
60	6.2	65	15	15.4
70	5.5	65	15	15.4
80	5.0	65	15	15.4
90	4.5	65	15	15.4
100	4.5	66	16	16.5
105	4.3	66	16	16.5

Notes:
1. Noise Bandwidth of pre-filter to nonlinearity = 116.14 MHz
2. Noise Band width of PLL = 100 kHz
3. SNR_L calculated from equation(6) by replacing the noise bandwidth B_n of pre-PLL filter with the loop bandwidth B_L of PLL.

■ **Table 2. Results without pre-PLL narrowband filter.**

improvement of more than 3 dB in the lock threshold performance of long loop PLL configuration over a case where pre-PLL narrow band filter is not incorporated, or a Costas loop is used. This means the carrier acquisition lock will occur at lesser input E_b/N_0 values in long loop PLL configuration. All the above measurements were carried out with a pre-PLL filter having a noise bandwidth of 5.04 MHz. The improvement in the performance will be greater if the noise bandwidth is further reduced, as there is no limitation to its reduction.

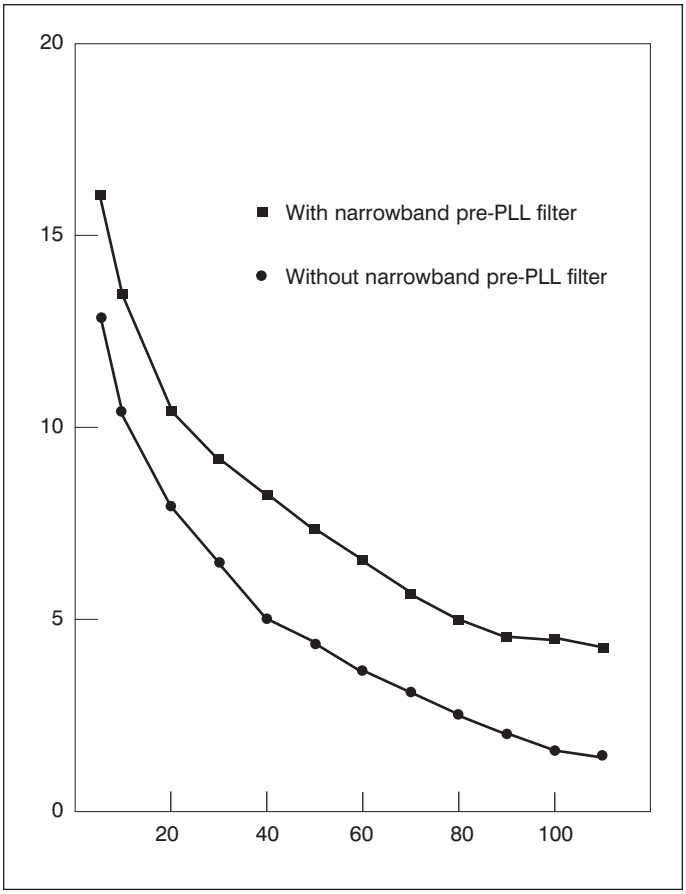
Conclusion

The paper establishes the advantage of long loop configuration over short loop schemes. The control of pre-PLL noise bandwidth in this technique has provided significant improvement in lock threshold of the demodulator, thus facilitating its usage for carrier acquisition from received modulated signals with very low *S*/*N* ratios.

The highly stable crystal oscillator source with which the regenerated carrier signal is locked, forms the coherent reference with a very high *S*/*N* ratio, resulting in reduction of detection loss. The demodulator has been tested in practice at a satellite ground station by tracking and acquiring the signals from remote sensing satellites. Carrier acquisition has been possible at antenna elevation angles as low as 0.5 degree, where the received signal has a low *SNR* and fluctuates widely due to terrain reflections. The system margin for signal acquisition has thus been extended. ■

References

1. P. M. Rao, G. Uma Devi and P. K. Jain, "Design of Multifunction Digital Data Demodulator and Bit synchronizer for Remote Sensing Satellite Data Reception," *Institute of Electronic and Telecommunication Engineers Technical Review*, Vol. 13, Nos. 4 & 5, 1996.
2. M. K. Simon, "Tracking performance of Costas loops with hard limited in phase channel," *IEEE Transactions on Communications*, Vol. COM-26, No.4, April 1978.
3. Floyd M. Gardner, *Phase Lock Techniques*, 2nd edition, John Wiley & Sons, New York, 1979.
4. M. K. Simon, "On the calculation of squaring loss in Costas loops with arbitrary arm filters," *IEEE Transactions on Communications*, Vol. COM-26, Jan 1978.
5. Robert M. Gagliardi, *Satellite Communications*, Van Nostrand Reinhold Company Inc., 1987.
6. W. C. Lindsey and M. K. Simon, "Data Aided Carrier Tracking Loop," *IEEE Transactions on Communi-cations*, Vol. Com-19, April 1971.
7. J. Layland, "An Optimum Squaring Loop Filter," *IEEE Transactions on Communication Technology*, Vol.



■ **Figure 6. Plot of measured results using the data from Tables 1 and 2.**

COM-18, No.5, Oct. 1970.

8. Smith A. Rhodes, "Effect of noisy phase reference on coherent detection of offset-QPSK signals," *IEEE Transactions on Communications*, Vol. COM-22, Aug. 1974.

9. V .K. Prabhu, "PSK performance with imperfect carrier phase recovery," *IEEE Transactions on Aerospace and Electronic Systems*, Vol. AES-12, No.2, March 1976.

10. Tri Ti Ha, *Digital Satellite Communications,* 2nd Edition, Mc Graw-Hill Publishing Company, New York, 1990.

11. S. A. Butman and J. R. Lesh, "The effects of band-pass limiters on n-phase tracking systems," *IEEE Transactions on Communications*, Vol. COM-25, No.6, June 1977.

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