# DC-12GHz 4-Bit GaAs Monolithic Digital Attenuator

*A novel switchable attenuator is described which operates from DC to 12GHz, has 15dB range, 3.5dB maximum loss and a die size of only 1.2 x 0.8 mm.*

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Digitally switched attenuators can provide wide range, accurately stepped control with little variation with temperature and high power handling. Relative to analog attenuators they have little distortion at high attenuation settings. The customary digital attenuator design involves a series of switched-path, binary-weighted attenuators connected by transfer switches [1]. Thus, a four-bit attenuator would require 8 SPDT switches and four thru-line/pad combinations. But an MMIC rendition of this approach results in excessive die size and insertion loss [2]. Alternative MMIC approaches include a DC-1.6GHz implementation or a narrow-band loaded-line technique at X-band [3, 4].

This design uses a two-state circuit in which the ratio of low to high insertion loss can be precisely defined. A binary weighted cascade of 'n' such elements provides an n-bit digital attenuator. The approach minimizes die size and insertion loss by combining the switching and attenuation functions in a single circuit. The topology is self-decoding and requires no additional logic on or off the chip.

*Digital attenuators offer more repeatable performance than analog, but the customary switched path approach is bulky and has high insertion loss.*

*Design*

The objective was to develop a fully monolithic, broadband, digital attenuator. Economy of die size, good attenuation accuracy and minimal insertion loss were the design goals. It was also desirable to utilize the unique features of monolithic integration such as close device to device tracking, uniformity of switching characteristics and low phase deviation to advantage in the design.

Figure 1 shows a two state prototype bit used in the design that can be set electronically to either a high or low insertion loss state.

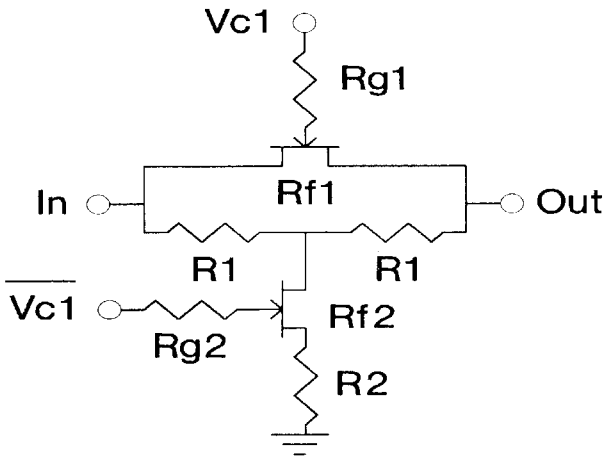


**Figure 1. Prototype attenuator bit.**

Analysis of the prototype attenuator is accomplished using the equivalent circuit of the equivalent FET model of Figure 2 and the following assumptions:

a) Gate resistances Rg1 and Rg2 are large in comparison with the reactance of the FET gate to channel capacitances.

b) The impedance of the FET in its off-state is high compared to all the other circuit impedances.

c) The circuit reactances due to FET capacitances are negligible.

The objective is to synthesize a circuit with a precise value of relative attenuation using Resistors R1 and R2 and FET on resistances Rf1 and Rf2. Thus for the high insertion loss state (FET1 off, FET2 on)

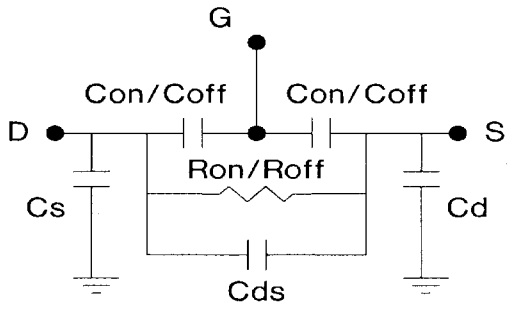


**Figure 2. Linear FET model of the prototype attenuator bit.**

*Eq. 1*

$$S_{21_H} = \frac{Z_0 (2R_1 + R_{F1})}{Z_0 (2R_1 + R_{F1}) + 2R_1 R_{F1}}$$

and for the low insertion loss state (FET1 on, FET2 off)

*Eq. 2*

$$S_{21_L} = \frac{2Z_0 (R_1 + R_{F2})}{Z_0^2 + 2Z_0 (R_1 + R_2 + R_{F2}) + 2(R_1 (R_1 + R_{F2})) + R_1^2}$$

The relative attenuation is therefore

*Eq. 3*

$$A_{REL} = \frac{2 (R_1 + R_{F2}) [Z_0 (2R_1 + R_{F1}) + 2R_1 R_{F1}]}{[Z_0^2 + 2Z_0 (R_1 + R_2 + R_{F2}) + 2(R_1 (R_2 + R_{F2})) + R_1^2] (2R_1 + R_{F1})}$$

Similar equations can be derived for the return loss in both states. Given a specific value of relative attenuation the width of FET1 can be determined based on isolation and bandwidth considerations. Solution of the above equations results in unique values of Rf2, R1 and R2.

The technique was used to synthesize 1dB, 2dB, 4dB and 8dB attenuator bits. A cascade of these circuits results in a 4 bit, 1dB step, attenuator. Figure 3 shows the resulting topology while Table 1 gives the circuit element values.

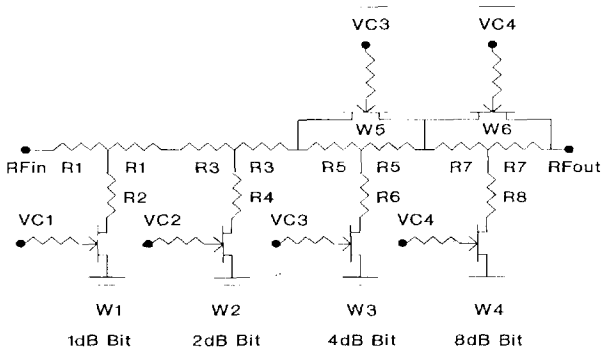


**Figure 3. Four bit digital attenuator topology.**

**Table 1. Element values for the digital attenuator.**

| *Bit Size* | *Series Resistor* | *Shunt Resistor* |
|---|---|---|
| 1dB | R1 = 2.9 ohms | R2 = 250 ohms |
| 2dB | R3 = 5.8 ohms | R4 = 115 ohms |
| 4dB | R5 = 8.5 ohms | R6 = 50 ohms |
| 8dB | R7 = 21 ohms | R8 = 13 ohms |
| *Bit Size* | *Series FET* | *Shunt FET* |
| 1dB | – | W1 = 60 micron |
| 2dB | – | W2 = 60 micron |
| 4dB | W5 = 500 micron | W3 = 120 micron |
| 8dB | W6 = 250 micron | W4 = 120 micron |

For operation at the highest frequency FET periphery is minimized, and with it device capacitance. Also, the series FETs are omitted from the 1 and 2dB bits, since their small series resistance does not require shunt compensation to realize better than 20dB return loss in both states. They have only 0.25dB insertion loss realized in this manner. The values of the gate resistors are chosen to equalize the switching time constants for the series and shunt switching elements of each bit, thereby providing uniformity in switching for the complete attenuator.

*The 1 and 2 dB bits do not require the series FET for good match in the through state, and they have broader bandwidth without it.*

The power handling of the device is influenced by resistor maximum current ratings, open channel current for each device in its on-state and the pinch-off voltage in its off-state. Specifically
Ipeak < Imax
and
Vpeak < 2*(Vcontrol-Vp)
determines the maximum current and voltage swing for each FET. Non-linear simulations predict a 1dB deviation from small signal attenuation settings at one half watt (27dBm) for this attenuator.

*Performance*

A four bit digital attenuator designed using the techniques outlined above has been fabricated and tested. An ion implanted process with an N+/N carrier profile is used [5]. The process uses 1 micron, self aligned gates and plated airbridges. A very high degree of device to device uniformity was experienced. Figure 4 shows the completed chip with a die size of 1.2 x 0.8mm (48 x 32 mils). Figure 5 shows the small signal characteristics of the design.

The attenuator design exhibits exceptionally broadband, well matched performance from DC to 12GHz. The reference insertion loss is less that 2dB from DC to 2GHz and is less than 3dB from DC-6GHz. The reference insertion loss at 12GHz is 3.5dB compared with over 10dB for prior designs [2]. The worst case VSWR at 12GHz is 1.8:1 over all attenuation states. Despite the broadband nature of the design, its attenuation accuracy, as evidenced in Figure 6, is q0.5dB or better over the DC - 12GHz bandwidth and 15dB attenuation range. This accuracy compares very well with hybrid approaches. Thus this device is capable of controlling over 100mW of RF power with little or no degradation in attenuation accuracy.

*The MMIC process used ion implantation, self aligned gates and plated air bridges for repeatable device to device performance.*

The non-linear characteristics of the device are such that the 0.1dB compression point occurs at

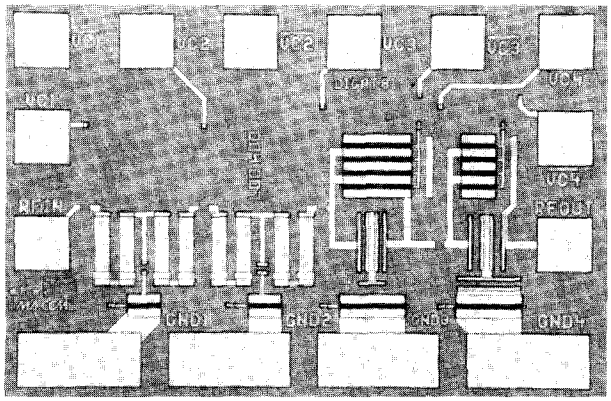

**Figure 4. Photograph of the 4 bit attenuator chip (1.2 x 0.8mm die size).**

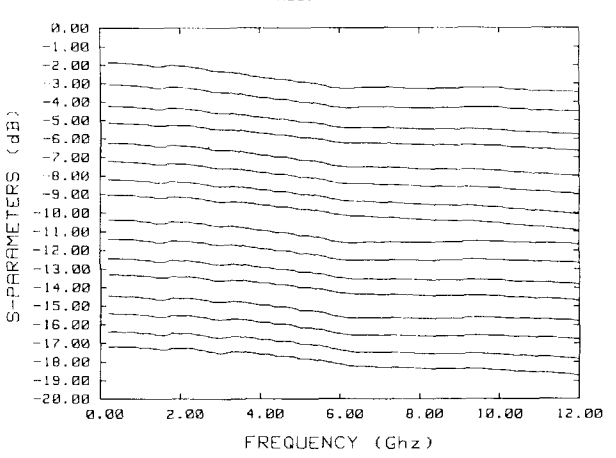


**Figure 5A. Insertion loss versus frequency.**

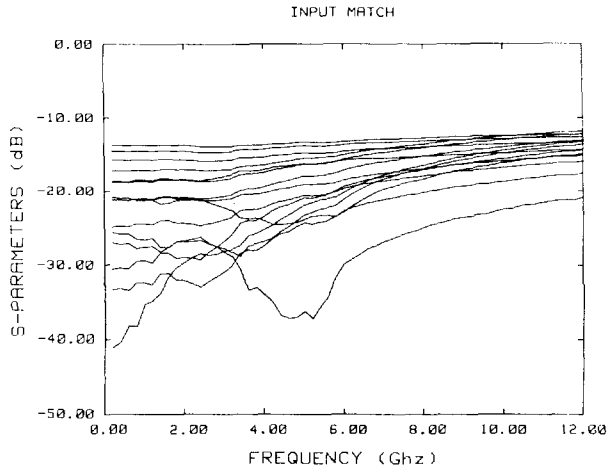


**Figure 5B. Return loss versus frequency.**

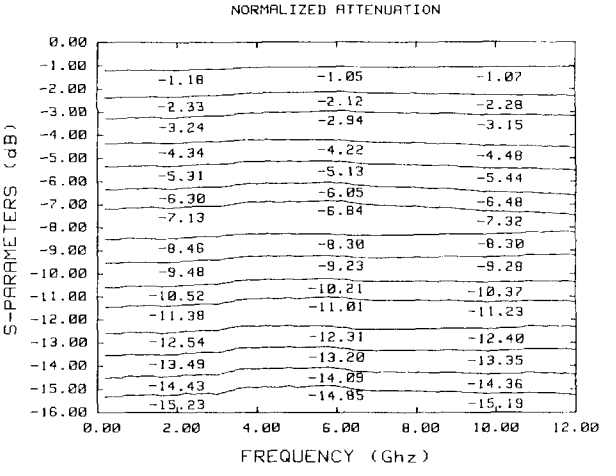


**Figure 6. Relative attenuation and attenuation accuracy.**

22dBm and the 1.0dB compression point is in excess of 28dBm in all states. The total leakage current with a -5V control is less than 20 microamperes, corresponding to negligible control power dissipation.

Exceptionally fast switching, with a 10/90% RF risetime of 2.5ns (Figure 7) applies. The 100% settling time is 22ns, with none of the 90/100% delay common to many hybrid approaches. Video breakthrough is well controlled; a 15mV peak signal is detected from a 1nS control pulse as shown in Figure 8. This video breakthrough represents the worst case for the device, obtained for the condition in which it is switched through its entire attenuation range with a very fast (1nS) edge speed.

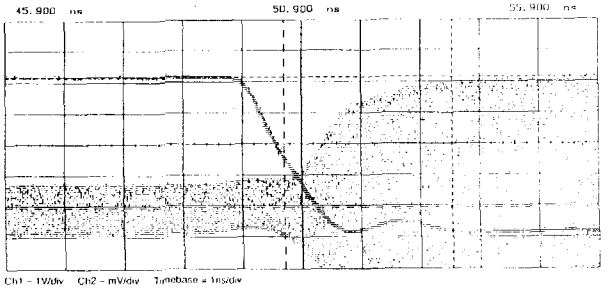


**Figure 7. Transient response switching from 15dB to 0dB relative attenuation.**

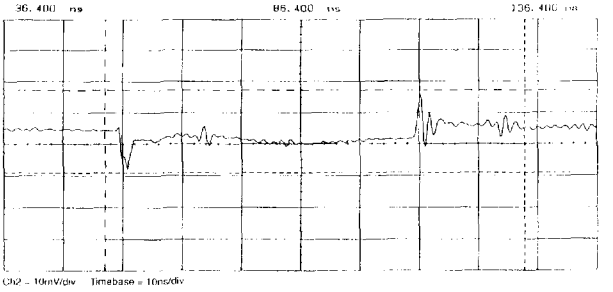


**Figure 8. Video breakthrough from the rising and falling 1nS edges of -5V control pulses.**

*Switching speed of 2.5 nanoseconds was obtained, without a delay period and with only 15mV peak video breakthrough.*

Since this attenuator is fully realized as a monolithic circuit, it requires a minimal number of bond wires. Furthermore, its circuit elements are small enough to be lumped elements even at 12GHz. This significantly reduces the phase deviation as a function of attenuation setting, which is a major problem with hybrid circuits. The total phase deviation

is only 6 degrees at 2GHz and 35 degrees at 12GHz. Figure 9 shows the relative phase shift versus frequency with attenuation state as parameter.

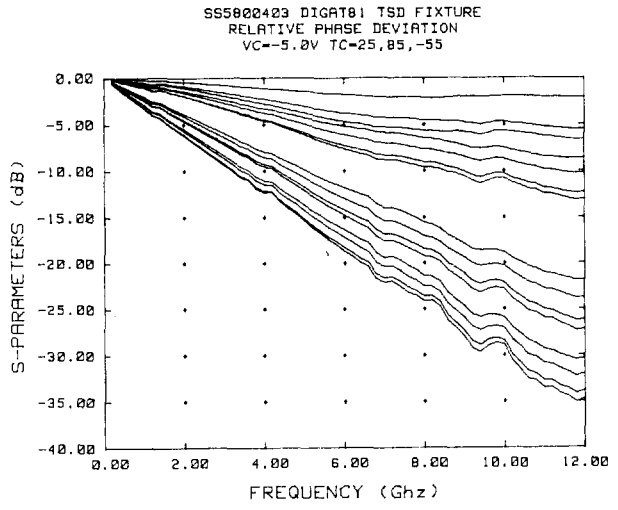


**Figure 9. Relative phase shift versus frequency (over all attenuation states).**

The similarity of the MMIC components on the same chip in their sensitivity to temperature variations allows precise temperature tracking to be achieved for different attenuation settings. The temperature drift in the low attenuation states is negligible. It is only q0.3dB at 15dB attenuation over a temperature variation of -55xC to +85xC.

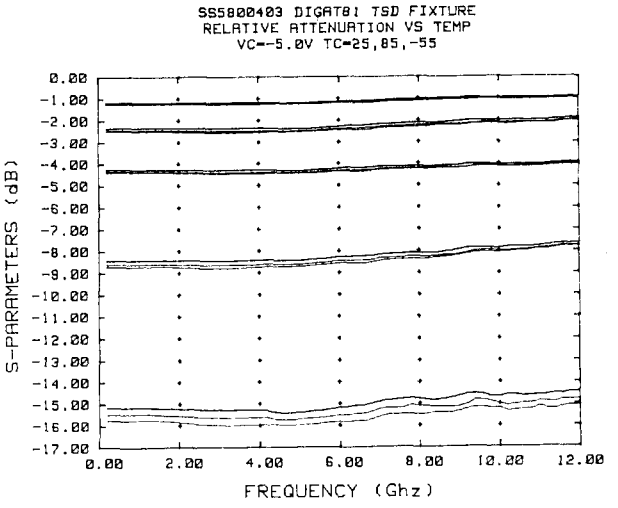


**Figure 10. Temperature drift for the four basic attenuation states from -55xC to +85xC.**

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6. Portions of this paper were presented at the 1991 GaAs Conference, Monterey, California in a paper entitled "An ultra broadband DC-12GHz, 4-bit GaAs monolithic digital attenuator."