Estimating GaAs IC Operating Temperatures

The author describes two computer programs (which he will give to the reader for a $15 handling fee) that calculate the temperature distribution in a packaged IC and show the results in a thermal profile illustration, greatly reducing the risk of designing an IC with hotspots.

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The prediction of maximum chip operating temperature for GaAs ICs is of considerable importance for reliability projections. Of special significance for GaAs (and other compound semiconductors), compared to Si, is the lower thermal conductivity, a characteristic which can lead to localized hot spots.

This paper describes the techniques which we have developed to deal with the peak temperature prediction during the design phase for GaAs ICs. Basic to our approach is a requirement to avoid elaborate and expensive design tools such as finite element modelers, which also do not typify user friendly software.

The techniques developed are based on proven analytical techniques and are implemented in two computer programs called: TACO and TempEst, which can be executed on MS-DOS based Personal Computers, are extremely fast, and require almost no training to use, ideal for the IC designer who has more interest in circuit realization than computer modeling. The programs have been proven useful after nearly five years of use, with dozens of IC designs for digital, microwave and precision analog circuits.

We make them available free of software charges (only a nominal cost for disk copying and handling is made) to encourage designers to address the critical area of IC temperature distributions early in the design cycle.

A generic representation of the thermal environment for a typical GaAs integrated circuit is shown in Figure 1, from which it is seen that typical individual devices—including MES-FETs, resistors and other heat producing elements—occupy only a small portion of the IC chip area.

We expect the overall reliability of the IC to be determined by peak hotspot temperature.

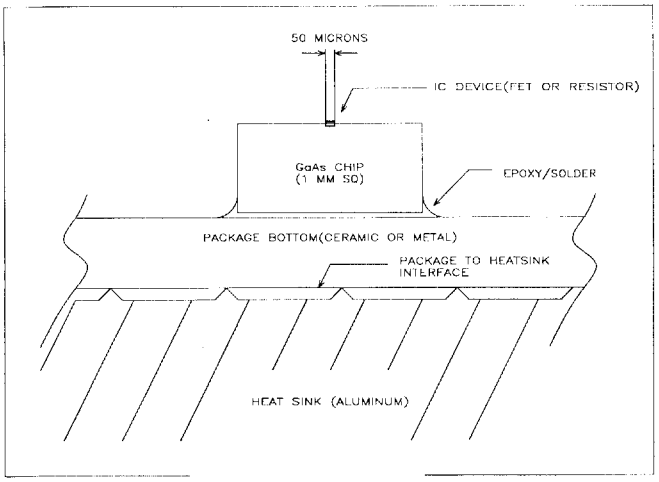

Figure 1. To-scale generic thermal environment for a typical GaAs IC chip.

We also expect the overall reliability for the IC as a whole to be determined principally by the peak temperature on the die of the hottest individual element. Beyond the circuit design, which determines the amount of dissipation in each element, the temperature of this hottest element depends upon a combination of the local hot-spotting effects as well as the heat conducting properties of its package design. Thus a complete thermal analysis must take into account all of these aspects[1, 2].

TACO (Thermal Analysis of Chip Operation)

TACO implements detailed modeling of local hot-spotting, the effect of localized heating due to the small physical size of the electrical components of an IC and the finite thermal conductivity of GaAs. It does not depend significantly on packaging details[1].

The analysis gives the superposition of all of the contributing heat sources in the IC.

TACO's analysis is based on the integral expression (Equation 1 in the Appendix) for a point heat source over the die surface. The point source is extended to cover a uniform rectangular source of heat, representing the rectangle of the heat dissipating element of the IC circuit. Since heat flow in solids is a uniform process over the temperature ranges to be encountered, the final temperature distribution at the surface of the complete IC can be found as the superposition of all of the contributing heat dissipating rectangles (circuit elements).

While this analysis could be carried out using hand calculations, and would have been prior to modern computers, the complexity of the formula (Equation 3 of the Appendix) would render such an approach both tedious and error prone. Rather, the equations are programmed for execution on a DOS (IBM compatible) personal computer. TACO can be used for

1) sizing individual resistors and FETs,
2) localized thermal modeling of cells,and
3) various other thermal analyses.

An example of the last is the computation of the thermal impedance of an airbridge support post to estimate its maximum current carrying capacity (prior to fusing).

For simple cases having up to 25 heat sources, the analysis takes only a few seconds.

TACO operates with a simple input command language describing the distribution and magnitude of heat sources over the IC die surface as well as the form of the presentation of the calculation desired. Both tabular and detailed graphical outputs are available, including the very useful thermal contour plot (Figure 3). For simple cases (having up to 25 heat sources) the program produces these outputs within a few seconds when operated on a personal computer having a 286 or better processor with 1 megabyte or more of available program memory.

Commands can be inputted at the program's prompt or from an ASCII text file. Example commands are:

1) temp 75
2) fet 0 0 60 .33
3) isotherms 90 100 110 120 130

The first statement sets T1 to 75C, the second locates a 60 micron FET at (0,0) dissipating 0.33 mW of power per micron of gate width and the last statement instructs the TACO to plot the isotherms at 90, 100, 110, and 130C.

Good agreement is obtained between these estimates and actual liquid crystal and infrared measurements.

Good-to-Excellent agreement is obtained between the estimates made using TACO and actual measurements obtained with liquid crystal and infrared measurements performed on fabricated circuits using the approximation that the effective length of the heat generating region of a FET is 4 microns[1]. The reasonableness of this approximation can be appreciated by referring to the model in Figure 2 which shows the approximate location of the actual heat generating region of an FET on the drain side of the gate metallization.

The measurements only show the surface temperature, which is maximum on the gate metallization. The use of an effective length of 4 microns in the temperature formula is a concession to the approximation of an actual element's heat source as a simple rectangular. The use of this effective length is an empiric adjustment in the calculation which yields both the correct peak temperature as well as a correct temperature distribution with distance from the FET active area.

The temperature profile computed using TACO to model an input cell is shown in Figure 3. In this instance the thermal modeling results displayed were obtained after the cell had been produced. The resultant temperatures were too high and the cell had to be redesigned. In the future such redesign can be avoided through the use of TACO and TempEst early, in the initial design phase of the IC.

TempEst (Temperature Estimator for packaged ICs)

TempEst is a computer program for estimating the operating temperature of ICs in standard packages, particularly GaAs ICs in ceramic packages. It was developed because the use of a single package "thermal resistance model" was inadequate for determining peak temperatures in ICs and accordingly for estimating their long term reliability.

A second program, TempEst, is used for estimating temperatures in packaged devices.

Developed subsequently to TACO, it employs a single menu/result screen—making unnecessary even the learning of the simple command language used by TACO—from which the user specifies parameters for a present package configuration.

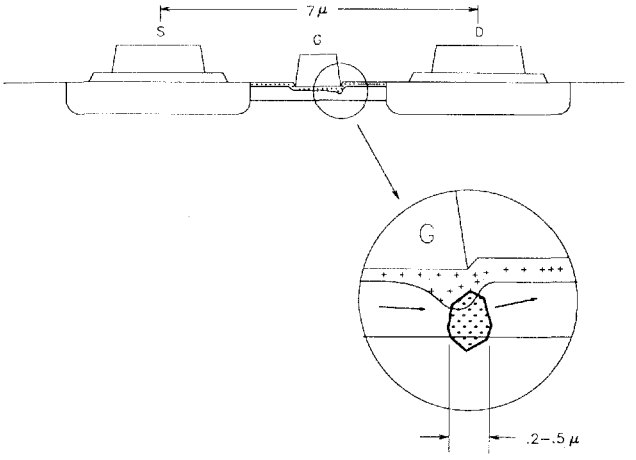

Figure 2. Approximate location of the heat generating region of an FET.

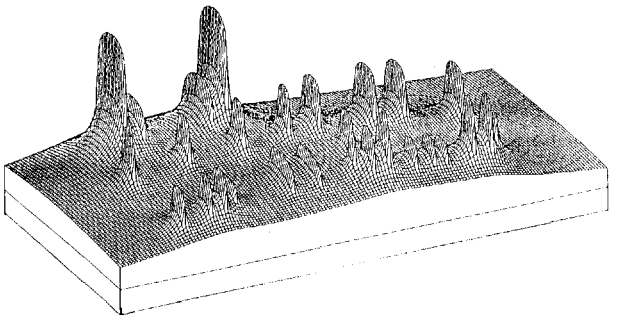

Figure 3. Temperature profile for an input cell—computed by TACO.

Input data for TempEst includes package and die dimensions, materials properties, and hot-spot data. Parameters to be inputted are selected by

pushing the key indicated next to the item and then responding to inquiries presented at the bottom of the screen. Selection of some items will bring up secondary screens requesting more information. For example, selecting a thermal conductivity item causes TempEst to ask if you want to input a "value" or a "material".

If material is chosen, a list of materials is presented from which a selection is made. When any parameter value is changed, TempEst immediately recomputes the temperatures and updates the output display.

The input screen with sample results are shown in Figure 4. The program uses no graphics and makes minimal demand on the memory, processor speed and other PC facilities. The information in

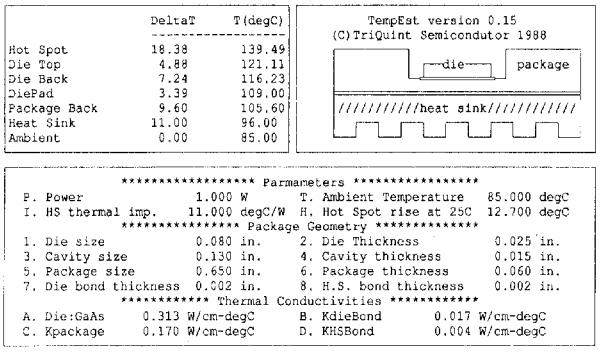

Figure 4. Main input screen for TempEst.

the upper left hand corner of the menu/result screen (Figure 4) are the estimated temperatures based on the inputs provided by the user. The figures listed under DeltaT alert the user of the relative contributions of various packaging components in setting the allowable peak-to-ambient temperature difference. This is helpful because it reveals where to concentrate one's efforts to reduce the peak temperature.

TempEst is based on a straightforward but detailed model (Figure 5) which includes thermal conductivity of the materials, and a thermal network using "lumped" approximations for package, chip, die attach, and heat sink components. The die-surface model assumes that the temperature rise at any point is due to small heat sources distributed uniformly over the die, plus a single, worst element, local hot spot.

Materials information can be entered manually, but TempEst already contains the parameters for most packaging materials in common use. The program is flexible enough to handle most common

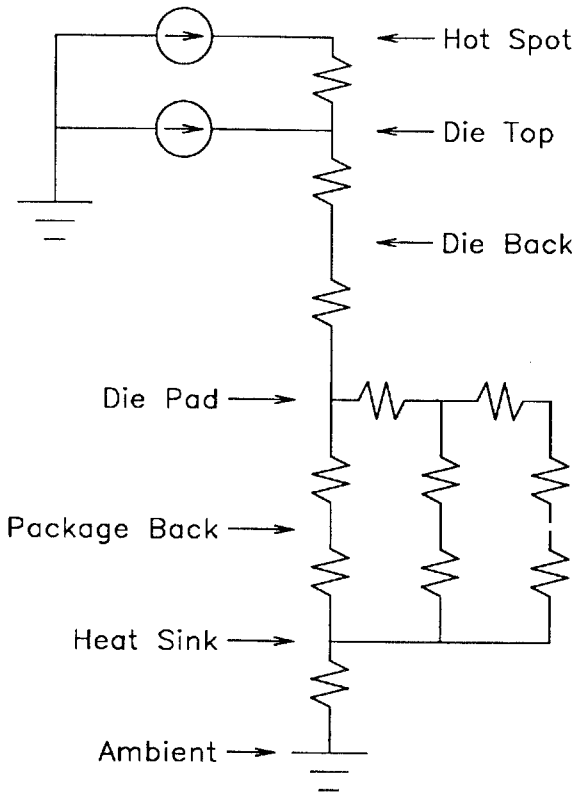

Figure 5. Thermal network used by TempEst

package chip geometries and incorporates the following features:

1. Program or user specification of materials and thermal conductivities.

2. Built-in selection of common materials, including the variation of thermal conductivity with temperature, especially important for GaAs.

3. Built-in thermal impedance estimator for air-cooled heat sinks.

4. Built-in hot-spot estimator. Though less comprehensive than the detailed analysis provided by TACO, this feature provides good hot-spot estimates for common FETs, including multifinger FETs, and resistor layouts. The user simply answers queries about the type of device and layout geometry, and TempEst computes the rest.

In comparisons with experimental results (see, for example [1,5]), TempEst has produced excellent estimates of peak temperatures within the context of limited input information, that is a more accurate estimate would require significantly more detailed information about the distribution of heat sources on the chip, and considerably more computing effort. In most cases, this is of more academic than practical interest.

Some typical comparisons between measured hot-spot temperatures and results computed with TempEst are illustrated in Table I.

Table 1. Measured hot-spot temperatures compared with TempEst predictions for two GaAs ICs.

Device	Technique	Base Temp.(°C)	Hot-Spot Meas.	Hot-Spot TempEst
Resistor	Liquid Xtal	-4	67	63
	Infra-red	128	226	230
FET	Liquid Xtal	28	63	68

The temperature estimates are particularly useful at the design stage to answer 'what if' questions.

TempEst has been particularly useful for peak temperature estimation at the design stage, when critical decisions about circuit design and packaging are made. It is helpful in answering such questions as:

– What is the effect of die size?

– What if we used solder instead of epoxy for die attach?

– What if we use elastomer pads instead of heat sink compound to contact the heat sink?

– What if we used a 0.030 inch thick cavity base instead of 0.015?

– How does the pitch of an interdigitated FET affect the peak temperature?

– If we measure the peak die temperature at 25C and then put the package in an oven at 175C for accelerated life testing, what peak temperature can we expect? Notice that the built-in temperature variation of the GaAs thermal conductivity is important to this question.

Availability

Copies of TempEst on 5-1/4 inch, DOS formatted disks and an instruction manual can be obtained by from: David Smith, TriQuint Semiconductor Inc., 3625A Murray Blvd., Beaverton, OR 97226. Include a check or money order for $15 made out to TriQuint Semiconductor Inc. for copying, shipping and handling.

References

1. D. H. Smith, A. Fraser, and J. O'Neil, "Measurement and prediction of operating temperatures for GaAs ICs," SEMITHERM '86 Symposium Technical Digest, 1986.
2. D. H. Smith, "Predicting operating temperatures for GaAs ICs," IEEE GaAs IC Symposium Technical Digest, pp. 187-191, 1991.
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4. K. Trigger and B. Chao, "An analytical evaluation of metal-cutting temperatures," *Transactions of the American Society of Mechanical Engineers,* vol. 73, pp. 57-68, Jan. 1951.
5. W. J. Roesch, "Thermo-reliability relationships of GaAs ICs," IEEE GaAs IC Symposium Technical Digest, 1988.

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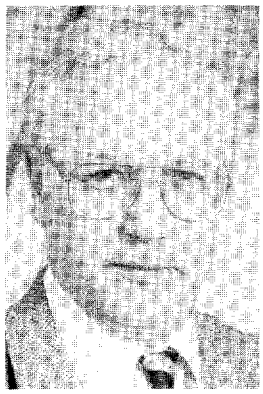

Appendix

TACO's Analysis is based on integration of the expression for a point heat source over the die surface.

Equation 1.

$$T(\vec{x}) = T_\infty + k^{-1}(T)\int_S q(\vec{x})d^2\vec{x}/|\vec{x}-\vec{x}'|$$

For local heating the boundary conditions

Equation 2

$$T \to T_\infty \text{ as } |x| \to \infty$$

are satisfied automatically.

Kirchoff's integral transformation [1,3],

Equation 3.

$$\tau(T) = T_0 + k^{-1}(T)\int_T^{T_0} k(T')dT'$$

is used to accommodate temperature dependence of the thermal conductivity in GaAs.

An analytical expression for this integral can be worked out for uniform rectangular heat source[4,1]:

Equation 4

$$T(x,y) = \frac{P}{2\pi klw}\times$$
$$\left[(x-x_0+\frac{l}{2})\ln\left(\frac{(y-y_0+\frac{w}{2})+\sqrt{(x-x_0+\frac{l}{2})^2+(y-y_0+\frac{w}{2})^2}}{(y-y_0-\frac{w}{2})+\sqrt{(x-x_0+\frac{l}{2})^2+(y-y_0-\frac{w}{2})^2}}\right)\right.$$
$$-(x-x_0-\frac{l}{2})\ln\left(\frac{(y-y_0+\frac{w}{2})+\sqrt{(x-x_0-\frac{l}{2})^2+(y-y_0+\frac{w}{2})^2}}{(y-y_0-\frac{w}{2})+\sqrt{(x-x_0-\frac{l}{2})^2+(y-y_0-\frac{w}{2})^2}}\right)$$
$$+(y-y_0+\frac{w}{2})\ln\left(\frac{(x-x_0+\frac{l}{2})+\sqrt{(x-x_0+\frac{l}{2})^2+(y-y_0+\frac{w}{2})^2}}{(x-x_0-\frac{l}{2})+\sqrt{(x-x_0-\frac{l}{2})^2+(y-y_0+\frac{w}{2})^2}}\right)$$
$$\left.-(y-y_0-\frac{w}{2})\ln\left(\frac{(x-x_0+\frac{l}{2})+\sqrt{(x-x_0+\frac{l}{2})^2+(y-y_0-\frac{w}{2})^2}}{(x-x_0-\frac{l}{2})+\sqrt{(x-x_0-\frac{l}{2})^2+(y-y_0-\frac{w}{2})^2}}\right)\right]$$

In this equation, the temperature is measured at (x,y) and the heat source is centered at (xo, yo). Superposition can be used to model mutual heating of multiple IC elements - for example multi-fingered MESFETs.