Wideband Gain Block Amplifier Design Techniques

Here is a thorough review of the device design requirements for a general-purpose amplifier RFIC

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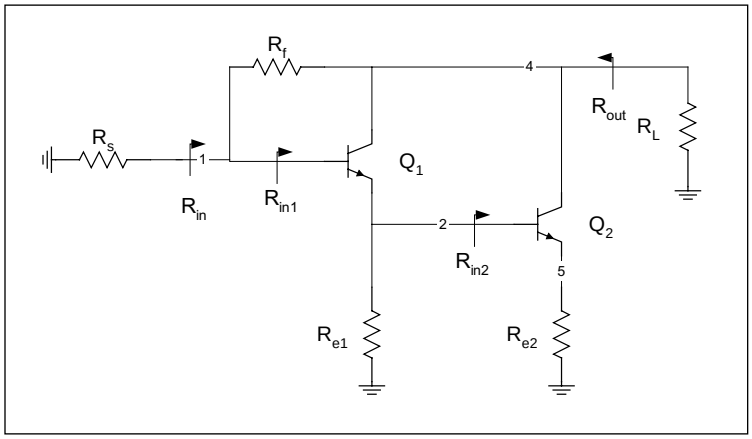
Wideband highly linear gain block amplifiers are becoming a popular, cost-effective alternative to the discrete designs presently used in many systems. These wideband gain blocks offer highly repeatable linear fixed gains with internally matched impedances and minimal external component count, which reduces manufacturing costs.

Replacing existing discrete designs with gain block amplifiers further reduces manufacturing costs by decreasing tuning time during manufacture, as well as reducing initial system design time. System designs can be simplified and completed faster. This reduction in time-to-market can remove costs from product development (and increase profit margins), simply by using gain block amplifiers.

The RF3348 is the first product in RF Micro Devices' RF3340 gain block amplifier series. This series offers low cost gain blocks with performance that exceeds that of previously available units. The RF3348 amplifier is designed to replace more expensive and less reliable discrete amplifiers and permit better distortion performance for a given DC power consumption. This article addresses the methods used to design and manufacture the RF3348 wideband linear amplifier. The amplifier is realized with a simple Darlington amplifier topology. Techniques used in the design of the amplifier include minimization of small signal nonlinear effects while achieving maximum linear amplification, gain flatness and input/output return loss.



▲ **Figure 1. Simplified Darlington amplifier circuit used for analysis of circuit behavior.**

Amplifier nonlinear design issues

Four distinct distortion-causing mechanisms in realistic amplifiers contribute to signal degradation, voltage compliance and nonlinear device parameters. The device parameters are nonlinear transconductance, nonlinear base-collector capacitance and nonlinear output resistance. These sources of distortion must be addressed with either design techniques or appropriate use of integrated device technology.

- *Voltage compliance.* Power supply level and circuit bias points within the amplifier must be sufficient to allow linear voltage swings for maximum input power drive levels. Overdriving the amplifier to levels exceeding bias conditions will cause voltage clipping in the output signal. Voltage clipping is the result of transistors being driven to "turn-off" during maximum power input signals. The

power supply level must be selected to provide adequate bias and voltage headroom for maximum output power levels. Typically, an RF choke provides amplifier bias by directly connecting the output to the DC level of the power supply. This bias configuration allows the output signal to swing around the average DC level of the power supply. Large negative output swings act as a decreasing power supply and tend to turn the amplifier off, which causes voltage clipping.

- *Nonlinear transconductance.* The exponential I-V characteristics of BJT devices inherently exhibit nonlinear operation when operated in an open loop state. Using emitter degeneration and shunt feedback with adequate bias current can permit the amplifier to obtain very good linear operation.
- *Nonlinear amplifier input/output impedance.* Nonlinear variations in amplifier input/output impedance produce distortion in the output signal. The open loop output impedance of the amplifier is ideally large and constant, but in reality a dependence on bias current and device physical parameters exists. This dependency causes nonlinear loading of the output, which distorts the output signal. In addition, parasitic base-to-collector capacitance exhibits nonlinear characteristics, which distorts the output signal. RF Micro Devices' GaAs HBT technology exhibits excellent input/output impedance due to very high output impedance and almost constant base-to-collector capacitance versus input voltage.
- *Minimizing nonlinear effects by design.* The RF3348 was implemented with a single-ended Darlington feedback amplifier configuration with an emitter degeneration resistor, as shown in Figure 1. The main advantages of the Darlington topology are high, nearly constant gain versus frequency response and good input/output return loss. Feedback resistors R_s, R_e and R_F are used to determine closed loop gain while fixing the input and output impedance to 50 ohms. A properly biased Darlington amplifier circuit minimizes nonlinear device effects with negative feedback.

Small signal amplifier design

Classical feedback amplifier methods of loop transmission analysis [1] are used to analyze the resistor shown in Figure 1. The loop transmission of the amplifier is found by breaking the feedback loop at the base of Q_1 in Figure 1, applying a test disturbance signal to the base and monitoring the return signal. The loop transmission is the ratio of return signal to test signal. The approximate mid-band loop transmission of the amplifier, using Figure 1, is given by

$$T_{mid} \approx -\left(\frac{R_1 \| R_{in_2}}{R_1 \| R_{in_2} + r_{e_1}}\right)\left(\frac{R_L \| r_o \| R_{F2}}{R_e + r_{e_2}}\right)\left(\frac{R_{in_1}}{R_{in_1} + R_f}\right) \quad (1)$$

where R_L is the load resistance, r_o is the open loop output impedance; r_{e1} is the dynamic emitter resistance of Q_1; r_{e2} is the dynamic emitter resistance of Q_2; and R_{in1} and R_{in2} are the impedance looking into the bases of Q_1 and Q_2. The ideal closed loop gain is the ratio of the feedback resistor and source impedance as given by

$$A_{CL_{ideal}} = \frac{-R_F}{R_S} \quad (2)$$

The actual amplifier closed loop gain at mid-band frequencies is given by

$$A_{CL} = A_{CL_{ideal}} \times \frac{-T_{mid}}{1 - T_{mid}} \quad (3)$$

where T_{mid} is the mid-band loop transmission or loop gain of the amplifier.

The characteristics of Equation (3) show the tendency of negative feedback to force the closed loop gain to approach its ideal value for large values of loop gain. This forcing effect can resist amplifier non-linear output fluctuations if $T_{mid} >> 1$ and amplifier operation within voltage compliance. In multiple GHz-wide bandwidth amplifiers, large loop gains are not possible because of possible instabilities. Wideband gain block amplifier designs achieve small signal linearity performance by combining both minimization of device nonlinear effects and negative feedback correction.

Amplifier input/output impedance at mid-band frequencies is mainly determined by amplifier parameters R_f, R_{e2} and R_s. Assuming amplifier input and output loading effects are negligible, R_{INOL} is approximately equal to R_{OUTOL}. The approximately equal value of R_{IN} and R_{OUTOL} is $R_f + R_s$. Using Blackman's theorem, the input impedance of the amplifier at mid-band frequencies is given by

$$R_{IN} = R_{IN_{OL}} \times \frac{1}{1 + |T_{mid}|} \quad (4)$$

The mid-band output impedance is given by

$$R_{OUT} = R_{OUT_{OL}} \times \frac{1}{1 + |T_{mid}|} \quad (5)$$

Negative feedback reduces open loop input/output impedance, as seen in Equations (3) and (4). The same forcing effect that forces the gain of the amplifier to approach its ideal value causes this reduction in amplifier open-loop input/output impedance. This effect is accomplished through voltage sampling at the output and information processing by current summation at the input. Negative feedback thus tends to idealize the input impedance presented to the input current signal while making the amplifier's output appear as an ideal

voltage source. The transformation of the amplifier's input and output into an idealized impedance and voltage source fixes the input/output impedance and minimizes effects of Beta variation, reactive loading and other non-linear variations for frequencies approaching the amplifier's 3-dB bandwidth. In contrast, low bandwidth op-amp type circuits with very high loop gain lower the input/output impedances to very small values and approach the ideal gain with high accuracy. Wideband circuits use these feedback principles to achieve desired gain and input/output return loss by adjusting the loop gain while maintaining stability against oscillations, near constant gain, and input/output return loss with process parameter variation. This loop gain adjustment is analogous to adding input and output ideal series resistance to an amplifier with very high loop gain. Therefore, wideband gain blocks can be realized with highly precise input/output impedance matching.

$$T(f) \approx -\frac{|T_{mid}|\left(1+\frac{j\times f\times \tau_{z_1}}{2\times\pi}\right)\left(1+\frac{j\times f\times \tau_{z_2}}{2\times\pi}\right)}{\left(1+\frac{j\times f}{2\times\pi\times f_{t_1}}\right)\left(1+\frac{j\times f}{2\times\pi\times f_{t_2}}\right)\left(1+\frac{j\times f\times \tau_{in}}{2\times\pi}\right)\left(1+\frac{j\times f\times \tau_{out}}{2\times\pi}\right)}$$

▲ **Equation (9).**

Three non-linear, small signal terms, r_{e1}, r_{e2} and r_o, are present in the loop gain Equation (1). These nonlinear terms cause output nonlinearity when the amplifier is operating with small input signals. Sensitivity analysis assuming small signal operation shows the effects of these nonlinear terms on loop gain [2]. Sensitivity of the loop transmission with respect to r_{e1} is given by

$$S_{r_{e_1}}^{T_{mid}} \approx \left(\frac{r_{e_1}}{R_{e_1}\|R_{in_2}+r_{e_1}}\right)\left(\frac{R_{e_2}+r_{e_2}}{R_L\|r_o\|R_f}\right)\left(\frac{R_{in_1}+R_f}{R_{in_1}}\right) \quad (6)$$

with respect to r_{e2} by

$$S_{r_{e_2}}^{T_{mid}} \approx \left(\frac{r_{e_2}}{R_{e_2}+r_{e_2}}\right)\left(\frac{R_{e_1}\|R_{in_1}+r_{e_1}}{R_{e_1}\|R_{in_1}}\right)\left(\frac{R_{in_1}+R_f}{R_{in_1}}\right) \quad (7)$$

and with respect to r_o by

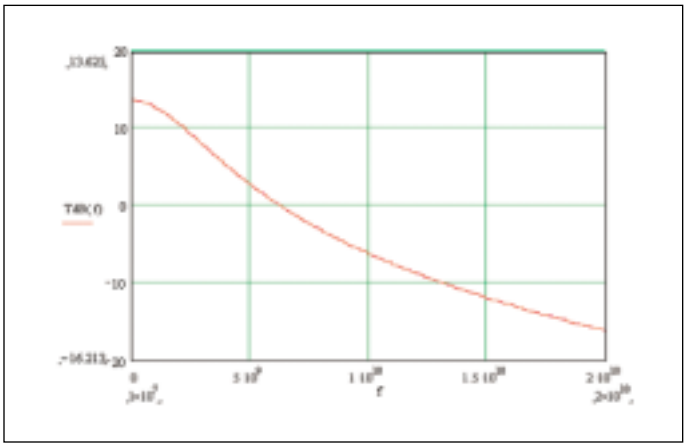
$$S_{r_o}^{T_{mid}} \approx \left(\frac{r_o}{R_L\|R_f+r_o}\right)\left(\frac{R_{e_1}\|R_{in_1}+r_{e_1}}{R_{e_1}\|R_{in_1}}\right)\left(\frac{R_{in_1}+R_f}{R_{in_1}}\right)\left(R_{e_2}+r_{e_2}\right) \quad (8)$$

Equation (6) suggests the sensitivity of the loop transmission, with respect to r_{e1}, can be minimized if $R_{e1} \| R_{in2} >> r_{e1}$. Since R_{e1} biases transistors Q_1 and Q_2, its value should be large compared to r_{e1}. Equation (7) suggests the sensitivity of the loop transmission, with respect to r_{e2}, can be very small if $R_{e2} >> r_{e2}$. Small r_{e2} is usually the case because large bias current is required in Q_2 to deliver maximum output power. Since R_{e2} approximately determines amplifier open loop gain and greatly effects noise figure, it should be made as small as possible. These criteria on R_{e2} suggest reducing r_{e2} with large bias current in the output-driving transistor Q_2 to improve the linear performance. Loop gain sensitivity, with respect to r_o, shows linearity is improved if $R_L \| R_f << r_o$, as shown in Equation (8). This is the case with very high output impedance RF Micro Devices GaAs HBT devices. Therefore, maximizing R_{e1} and increasing Q_2 bias current with the use of RF Micro Devices' GaAs HBT devices in wideband Darlington topology amplifiers will optimize small signal linear performance.

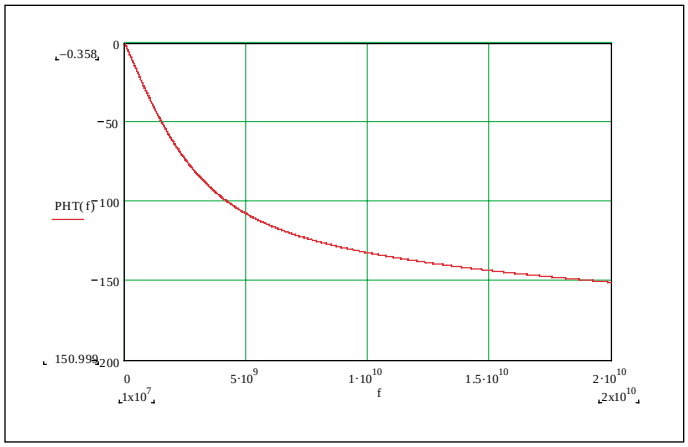
Small signal amplifier frequency response

An approximate expression for frequency response of the loop gain can be found using the time constant method [2]. Once the frequency-dependent expression for loop gain is found, the closed loop amplifier response is simply obtained by substitution for T_{mid} in Equation (3). The time constant method consists of calculating the time constants at each node within the amplifier, including the frequency limitations of the active devices, f_T. These time constants represent poles and zeros in loop gain frequency response. Transistor unity current gain frequencies are included in the analysis as poles and combine with the time constants for the approximate frequency-dependant loop gain expression is given by Equation (9) above, where f_{T1} and f_{T2} are poles associated with devices Q_1 and Q_2, t_{in} and t_{out} are time constants associated with the amplifier's input/output, and f_{z1} and f_{z2} are locations of parasitic zeros. The remaining poles associated with nodes 2 and 5 can be neglected because the impedance at these nodes is very small and resulting poles are located at frequencies beyond the loop gain unity gain frequency.

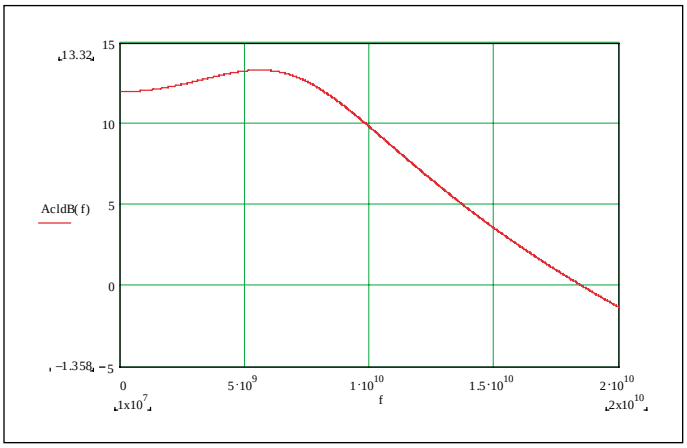
The zero described by f_{z1} in Equation (8) is due to the parallel connection between the feedback resistor R_f and parasitic base to collector capacitance of transistor Q_1. Zero and f_{z2} in Equation (8) result from parasitic series inductance and degeneration resistor R_{e2}. Dominant poles in the frequency response are due to both input and output time constants, which are at a much lower frequency compared to the unity current gain frequencies of the transistors. Large parasitic shunt capacitance increases these input/output time constants. Also, these dominant poles have approximately equal frequency locations since the circuit has equal source/load imped-



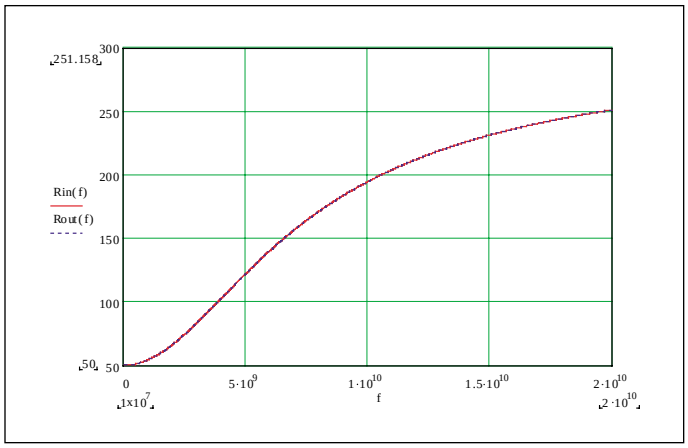
▲ **Figure 2(a). Darlington amplifier loop gain plot.**



▲ **Figure 2(b). Darlington amplifier loop gain phase plot.**



▲ **Figure 3. Darlington amplifier closed loop gain dB magnitude plot.**



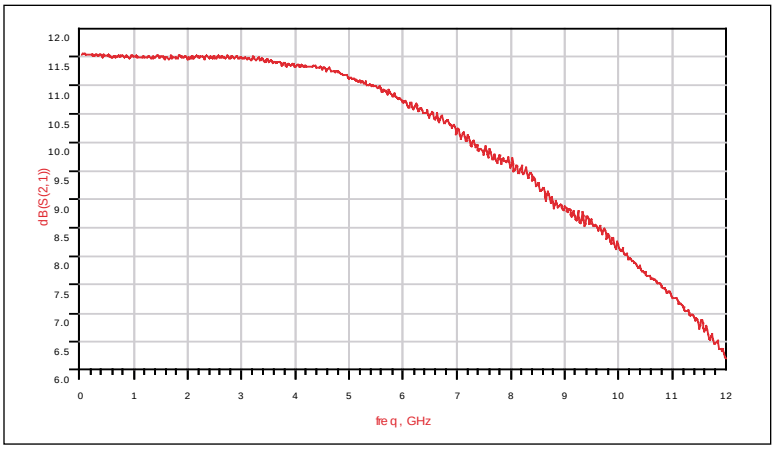
▲ **Figure 4. Plot of the Darlington amplifier input/output impedance vs. frequency.**

ance and approximately equal parasitic shunt capacitance. Therefore, the loop gain expression has a dominant double pole, which causes excessive phase shift and results in low amplifier phase margin. The zeros at f_{z1} and f_{z2} tend to neutralize the poles at f_{T1} and f_{T2} by decreasing loop gain phase shift. Stability against oscillations is secured because the low mid-band loop gain value will reach its unity gain frequency before loop gain phase shift reaches 180 degrees, as shown in Figures 2(a) and 2(b). This results in a stable design that exhibits the gain peaking frequency response as shown in Figure 3.

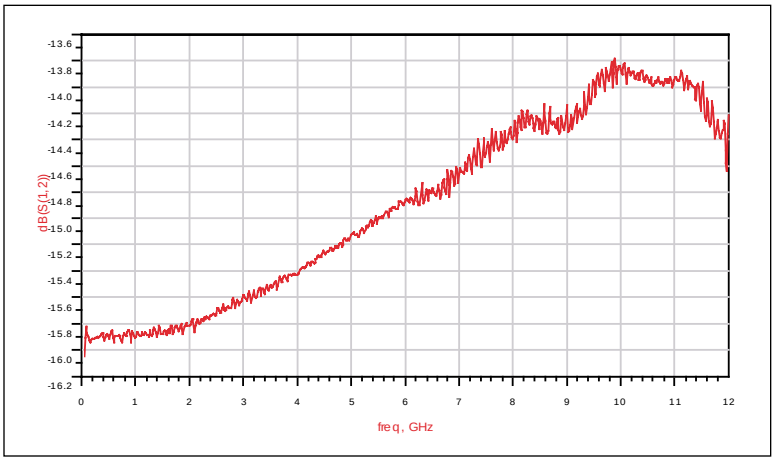
The amplifier-closed loop gain frequency response exhibits a very flat response with 2 dB peaking and a 3 dB bandwidth of 9.8 GHz. Equation (2) correctly predicts the gain roll off seen in Figure 3 and shows that this decrease in closed loop gain approaches zero as T approaches zero. Adding series resistance to the base of Q_1 further reduces loop gain phase shift. The value of this series resistance is found through circuit simulations. This simple solution improves phase margin and reduces frequency peaking by effectively adding a low pass filter to the amplifier's frequency response.

The maximum stable bandwidth of the amplifier is limited by the unity current gain frequencies of devices Q_1 and Q_2. These device-induced poles in Equation (9) are essentially fixed depending on bias conditions. Attempts to improve bandwidth by decreasing input/output time constants will produce amplifier instabilities when the dominant double pole frequency approaches f_{T1} and f_{T2}. Bandwidth can be slightly improved with careful choice of package type and PCB layout, but care must be taken in order to maintain amplifier stability. RF Micro Devices' GaAs HBT technology possesses an f_T approaching 30 GHz, which is sufficient for this design.

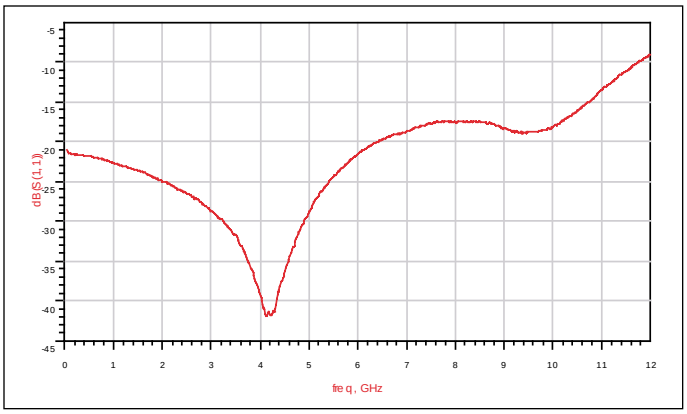
The frequency response of the input impedance is found by substituting Equation (9) into Equation (3) and Equation (4) for the output impedance. The input/output impedance is set to 50 ohms by the loop gain (very precisely for low frequencies), but increases with decreasing loop gain, as shown in Figure 4. This



▲ **Figure 5. Measured amplifier gain, S_{21}.**



▲ **Figure 6. Measured amplifier reverse gain, S_{12}.**



▲ **Figure 7. Measured input reflection coefficient, S_{11}.**

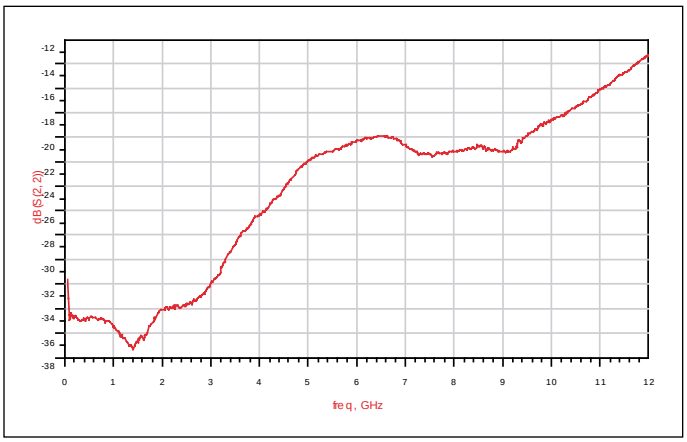
shows how effectively negative feedback fixes the input/output impedance for frequencies within the 3 dB bandwidth of the loop gain. Equations (3) and (4) show that this increase in impedance is expected because R_{in}/R_{out} approaches R_{INOL}/R_{OUTOL} as T approaches zero with increasing frequency, as shown in Figure 2. Amplifier input/output impedance is more sensitive to changes in loop gain compared to closed loop gain due to the inversely proportional loop gain relationship. The closed loop gain of the amplifier is less sensitive because the loop gain correction factor in Equation (2) tends to ratio to unity.

Large signal amplifier considerations

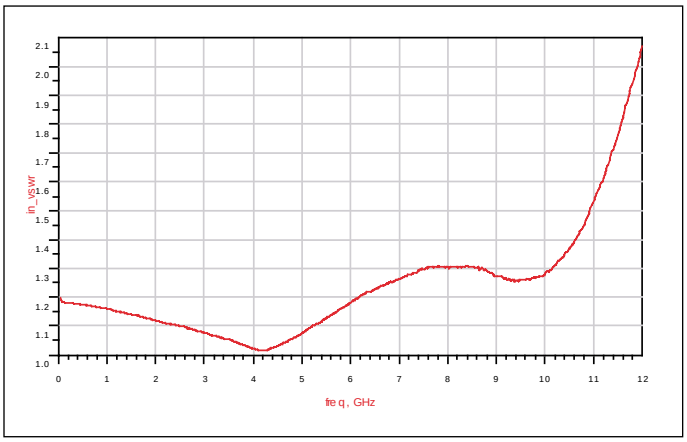
The Darlington amplifier operates in a Class A state. This operating state simplifies amplifier design since constant power is dissipated regardless of input power level. Usually these gain blocks are operated under small signal conditions achieving highly linear amplification. This small signal operation places more importance on output third order linearity instead of maximum output power. Designing the amplifier for output third order linearity allows the assumption of amplifier operation at maximum output levels 10 dB less than the 1 dB compression point. If we assume that the output third order intercept point is 10 dB higher than the 1 dB compression point, then determination of maximum amplifier output power is achieved. We also assume that the maximum deliverable output power from the amplifier is equal to maximum output power of transistor Q_2. Therefore, the bias current in Q_2 must be set at a sufficient level to deliver maximum required output power.

This current can be easily calculated from the specified output 1 dB compression power into the source impedance. This calculated current is the ideal minimum bias current that will deliver maximum specified output power. The final Q_2 bias current will be slightly larger than the calculated value and is easily found with nonlinear circuit simulations. Transistor Q_1 must be biased with sufficient current to drive the base current of Q_2 and voltage swing on R_1. This current is small compared to the current in Q_2, but must be large enough to drive the frequency dependant base current of Q_2 for the amplifier's bandwidth. The final value of the bias current for Q_1 is easily found with nonlinear circuit simulations of output 1 dB compression point versus frequency.

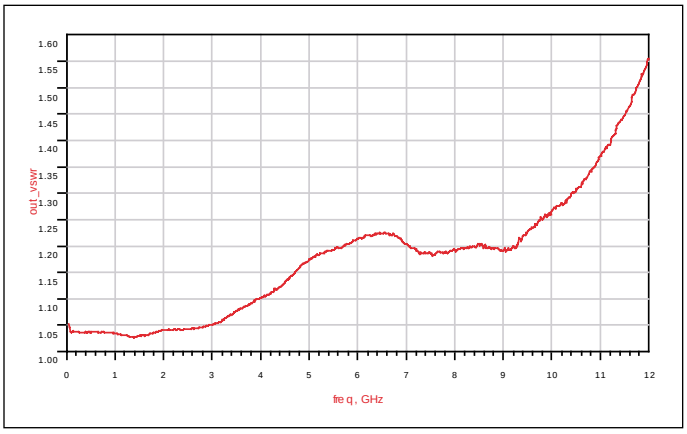
The voltage compliance of the amplifier is evaluated to ensure sufficient voltage head room within the amplifier and eliminate distortion caused by voltage clipping. This can be challenging considering the trend toward decreasing supply voltages. This problem is made worse because the amplifier drives output power directly into system impedance, which causes large output voltage swings that limit the maximum deliverable amplifier output power. Connecting the collectors of Q_1 and Q_2 to the output allows large negative output voltage swings



▲ **Figure 8. Measured output reflection coefficient, S_{22}.**



▲ **Figure 9. Measured input VSWR.**



▲ **Figure 10. Measured output VSWR.**

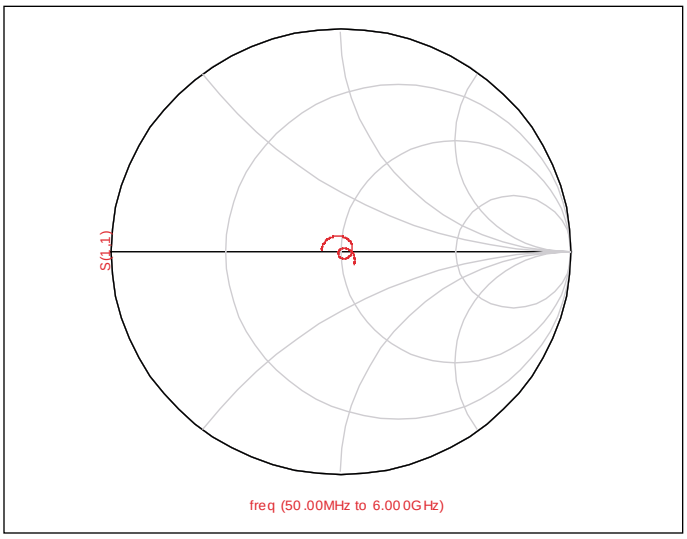
to decrease the collector voltage of Q_2 below its saturation point, which causes severe distortion. Increasing the power supply voltage or decreasing the bias voltage of Q_1 can improve this distortion mechanism. Performing time domain simulations of the circuit and observing the collector current of Q_1 versus time with increasing output power easily detects this effect during large negative output swings. When the collector current of Q_1 approaches zero, the base current of Q_2 approaches zero and turns off the amplifier. The design of the amplifier must include evaluation and compensation of this Q_1 saturation effect to ensure amplifier output power drive capability.

The RF3348 was designed using these general guidelines, which provide a means to calculate the initial values of R_{e1}, R_{e2}, R_f and bias currents. The limitations of these small signal approximations are the inabilities to predict large signal and high frequency device effects accurately. Modern analog circuit simulators accurately predict these effects with sophisticated small and large signal models. All final component and bias values were found using the nonlinear analog circuit simulator Advanced Design System by Agilent Technologies.

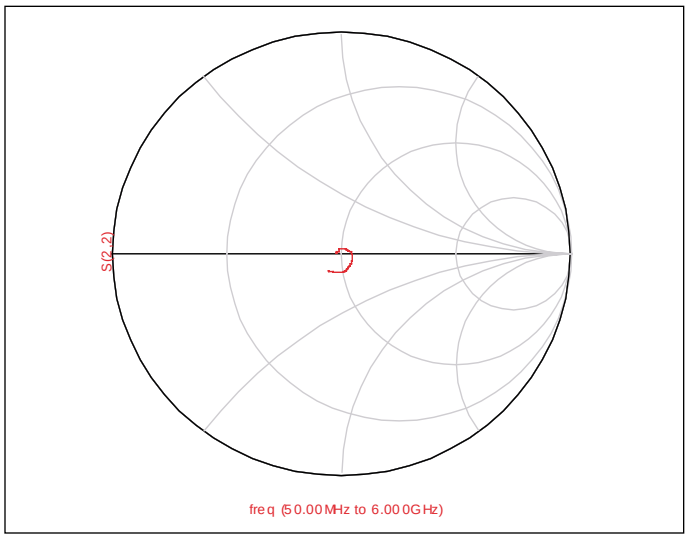
Measured results

The RF3348 was evaluated by measuring the amplifier's *S*-parameters, NF, output 1 dB compression point and output third order intercept point. The scattering parameters of the amplifier were measured using high frequency input/output bias tees and test fixture specifically designed for the ceramic Micro-X package as shown in Figures 5 through 13. The use of this test fixture ensures test data will not include degradation due high frequency PCB and passive component limitations. A frequency range of 50 MHz to 12 GHz with 401 points was used for *S*-parameter measurements with a source power level of –10 dBm. S_{21}, plotted in Figure 5, shows very good amplifier gain flatness, as predicted by Equation (2). The added series resistance with the base of Q_1 has removed the expected gain peaking in the frequency response. The measured 3 dB bandwidth is 9.5 GHz, which agrees very well with analytical 3 dB bandwidth shown in Figure 3. The reverse gain S_{12} is very flat over amplifier bandwidth with typical magnitude values 5 dB less than the forward gain, as shown in Figure 6, which is an indication of amplifier stability against oscillations.

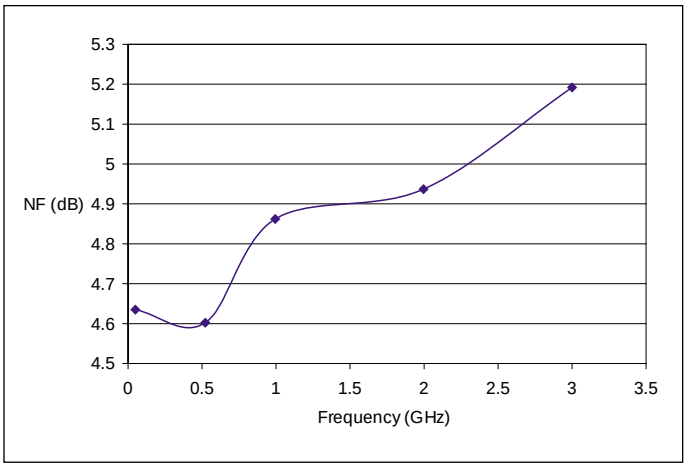
Measured input/output reflection coefficients S_{11} and S_{22} are plotted in Figures 7 and 8. The measured input return loss of the amplifier is better than 18 dB within the 3 dB bandwidth with a maximum of 42 dB around 4.1 GHz, as shown in Figure 7. This maximum is caused by the large input capacitance of Q_1 resonating with stray input inductance. The measured output return loss is better than 20 dB for entire amplifier 3 dB bandwidth and better than 32 dB up 3 GHz, as shown in Figure 8. Input and output VSWR is better than 1.3 and 1.25 over the entire 3 dB bandwidth, as shown in Figures 9 and 10. The output return loss is more consistent with the analytical approximation given by Equation (4). This results from the very high output



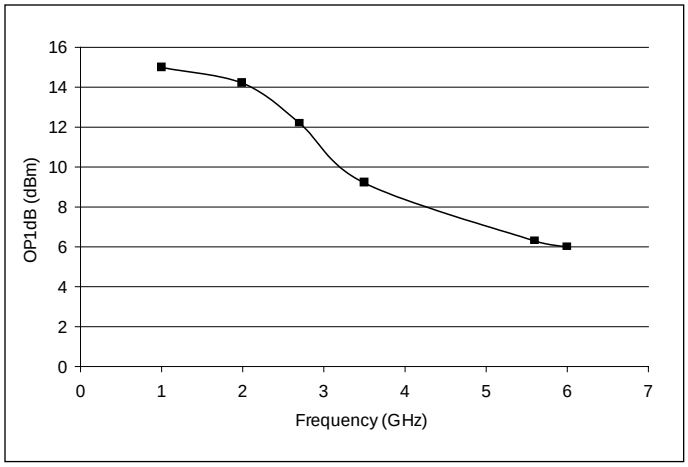
▲ **Figure 11. S_{11} Smith chart plot.**



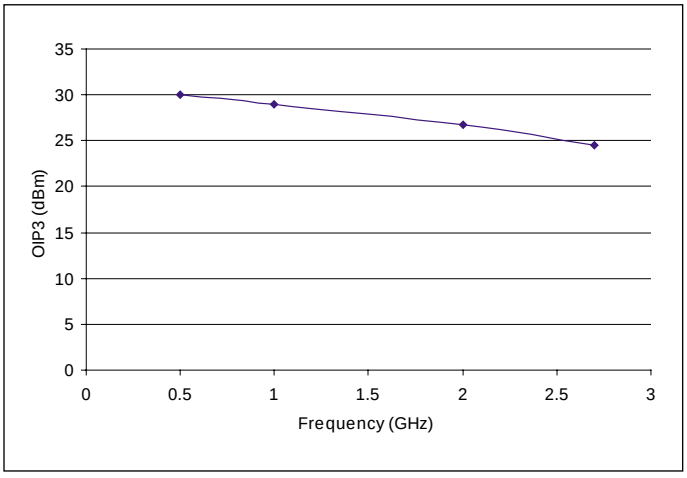
▲ **Figure 12. S_{22} Smith chart plot.**



▲ **Figure 13. Measured amplifier noise figure.**



▲ **Figure 14. Measured amplifier output 1 dB compression point.**



▲ **Figure 15. Measured amplifier output third order intercept point.**

GaAs HBT device output impedance that does not significantly load the closed loop output impedance. This excellent mid-band input/output return loss performance shows how effectively negative feedback can hold the input/output impedance to a near constant value of 50 ohms, as shown in Figures 10 and 11. Only at high frequencies does the input/output return loss begin to decrease with decreasing loop gain, as predicted by Equations (3) and (4). Amplifier noise figure was measured at 1 GHz to 3 GHz, as shown in Figure 12. Noise figure results show the 1 GHz noise figure is 4.7 dB and increases 0.3 dB to 5 dB at 3 GHz, which is consistent with beta roll off of input transistor Q_1.

Amplifier large signal parameters output 1 dB compression point was measured at frequencies 1 GHz to 6 GHz, as shown in Figure 15. Results show the output 1 dB compression point is 15 dBm at 1 GHz and 9 dBm at

6 GHz with a 2 dB decrease from 1 GHz to 2.7 GHz. These results show the effects of Q_2 beta and loop gain roll off for frequencies greater than 3 GHz. The output compression point remains nearly constant up to 3 GHz then rolls off due to decreasing loop gain. The output third order intercept point was measured using the two-tone method [3] at 1 GHz, 2 GHz and 3 GHz, as shown in Figure 16. Results show the amplifier output third order intercept point rolls off by 5 dB at 3 GHz.

Conclusion

This article has presented simple analysis and design techniques for wideband Darlington negative feedback amplifier design. A high performance wideband gain block amplifier was successfully realized by utilizing these proposed design techniques. Results show that the simple mid-band approximations used to predict amplifier performance gives very good correlation with high-frequency measurements. This emphasizes how effectively design properties of negative feedback and optimum device technology can realize high performance wideband gain block amplifiers. These realized amplifiers have very good small signal, noise and large signal performance. Results showed that measured amplifier data meets all required specifications. ■

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