Fundamentals of RFIC Package Characterization

RF and microwave packages are a necessary part of the total circuit and must have their effects included in design

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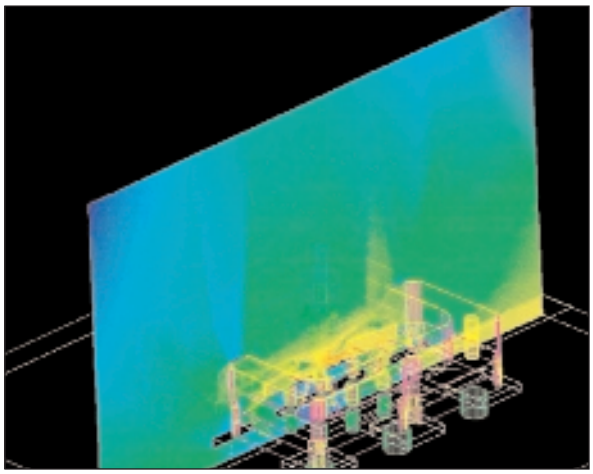
Most RFIC designers concentrate their characterization effort on the die. Overlooked in the design process is the package. This article gives a sampling of the basic issues involved in package characterization and discusses fundamental characterization concepts.

The design cycle of an RFIC is well-known. Built from a database of elements, the RFIC or MMIC seeks a response that will meet the customer's needs. To understand how the design will hold up over IC process variances, stability and sensitivity analyses are performed until a satisfactory circuit is obtained. Next, the components in the schematic are laid out. An optimal layout achieves the circuit in the smallest area. Wafer die are then fabricated to the layout. Following several weeks of fab processing, sample die are measured in the lab. Correlation is established between simulated and measured. If problems arise, the die is redesigned. After a number of iterations, a die with acceptable RF performance is achieved. Throughout this cycle, the RFIC designer directs maximum effort to the die design.

The second step is the package. Ideally, the package should be transparent to the die, "invisible" at RF. At high frequencies, nothing physical is invisible over a significant bandwidth. The package frequently adds another iteration to the design cycle. More troublesome is that the package is not predefined; each is custom-designed to the die layout. For superior performance, packages cannot be simply pulled off the shelf.

All the customer cares about is the performance of the final component. Yet the component is composed of pieces, like a puzzle. Try to understand how the pieces behave separately and together. With the right tools and procedures, the puzzle can be solved. Five concepts guide RFIC package characterization.

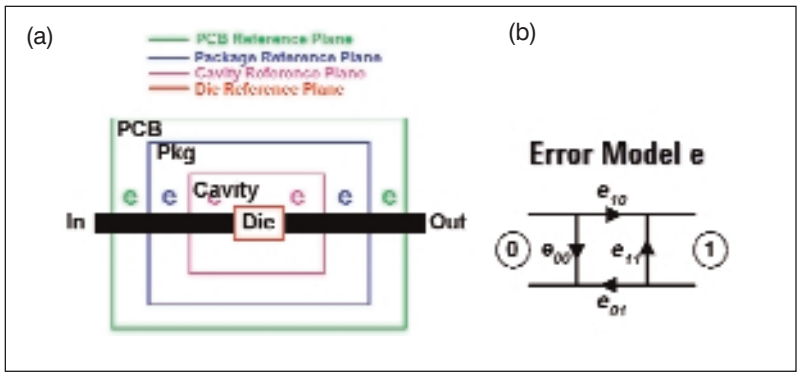


▲ **Figure 1. E-field plot of a component soldered to a PCB.**

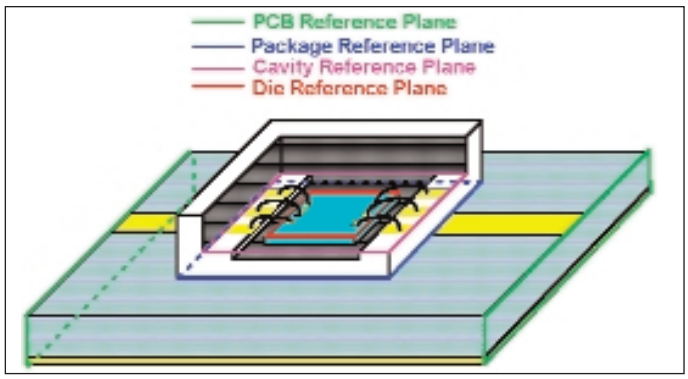
Using electromagnetic field simulators

Understanding electromagnetic interactions is at the heart of package characterization. Conductor layers couple to nearby conductors. Coupled electric fields induce current. The induced current leads to more E-fields elsewhere. Dielectric interfaces reflect some energy but allow a portion to pass. Inadequate grounding allows energy to propagate in the ground plane [1]. These electromagnetic effects, while difficult to quantify, impact the package RF behavior.

Electromagnetic field simulators provide insight into dynamic field action within the package. This supports the equivalent-circuit modeling effort. Shown in Figure 1 is an E-field

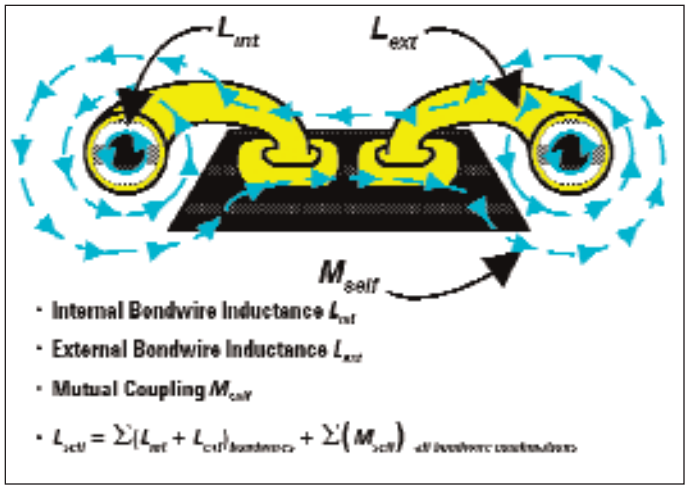


▲ **Figure 2. (a) Division of the component into calibration planes; (b) Error adapter for a segment between planes.**



▲ **Figure 3. The component divided into physical calibration planes.**

plot of a component soldered to a PCB. The plane cuts through the middle of the PCB, microstrip and package. The package is a LCC (Leadless Chip Carrier). Solderpads, shown in white, mount the package to the PCB. Filled vias in the PCB, shown in green, ground the unused pins. Epoxied inside the package is a die. The current on its surface creates intense E-fields, shown in yellow. The package is unlidded, so electric fields radiate out the top. One-mil diameter bond wires connect the package and die pads inside. Each connection is double-bonded.



▲ **Figure 4. Inductances associated with bond wires.**

Layering the RFIC design

Calibration planes section the component, as shown in Figure 2. Mathematical error models represent each portion. Measurements are then referred to the bounds of the reference planes. Typically, inside the boundaries is what is being measured and outside is the test system. This is the concept of a reference plane. Sectioning the component into reference planes can become complicated, as shown in Figure 3. For example, the area between the package and die pads contains bond wires. Coupling occurs from the bond wires to adjacent metal in the package and on the die. This makes the bond wire cavity the most difficult to characterize. Arbitrarily allotting coupling effects to one reference plane or the other is valid. However, such decisions should be clearly described.

Reference planes consist of two types, physical and electrical. Upon calibration, the electrical reference plane and the calibration plane align along the same line. Unlike physical reference planes, electrical reference planes can overlap. In packages, coupling overlaps the electrical calibration planes.

Package behavior affecting RF characterization

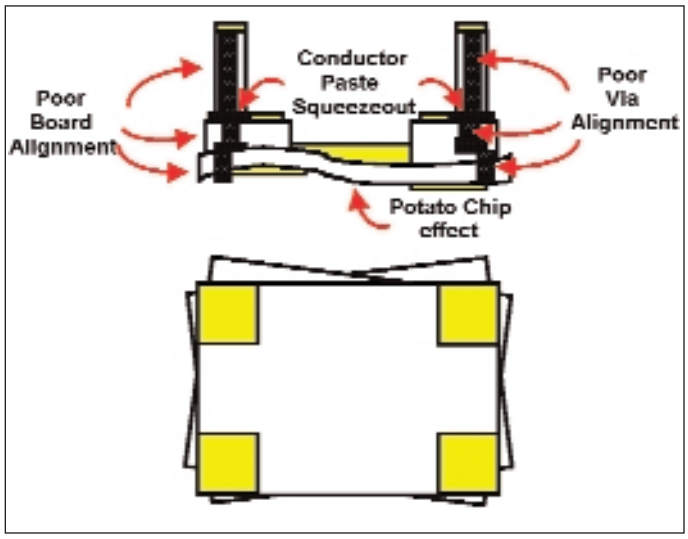
Inductance L is the proportion of magnetic flux ψ to the current flow I that created it. In a bond wire, inductance exists internally and externally (see Figure 4). Internally, I flows uniformly through the bond wire at DC. As the frequency f increases, I flows closer to the surface. This property is known as the skin depth. The wire's internal inductance L_{int} decreases as the square root of f, or –10 dB per decade. As f increases, the current moves toward the surface. Dynamic I creates ψ, so ψ exists nearer the surface, too. As I crowds, less of it flows. This makes for less ψ.

Externally, flux lines run just beyond the wire's diameter. This leads to external inductance L_{ext}. If two or more bondwires connect to the same pad, then current will flow in both. Since I flows in the same direction, external ψ lines will constructively couple. The net self-inductance L_{self} is the sum of the individual bondwire inductances ($L_{int} + L_{ext}$), plus the mutual coupling M_{self} between them. When bondwires are orthogonal, no coupling occurs.

The package design can point to problems with the die design, such as on-die mutual coupling between elements.

Selecting the style of package

Out of a multitude of packages on the market today, three common ones are discussed here.



▲ **Figure 5. Mechanical issues associated with multi-layer ceramic boards.**

1. *Small-outline transistor* (SOT) packages are the most common. The black plastic acts as a dielectric covering ($\varepsilon_r \approx 5$), which affects the fields coming off the die surface. It loads the conductors differently than air ($\varepsilon_r = 1$). The die will be encased in plastic. RF on-wafer testing occurs with air above the die. This is an important detail. The S-parameters of the die are often imported into Agilent's ADS CAE package for simulation. To emulate the final product, they should be accompanied by EM-field simulations of the encapsulated die. The SOT legs add loss and parasitic effects limiting the high-frequency performance.

2. *Single-layer ceramic* does away with package legs. Alumina provides a durable mounting surface and a uniform dielectric. A thin-film etch process offers better tolerances on the conductor line widths. This package is a compromise between the SOT and multi-layer ceramics.

3. *Multi-layer ceramics* permit vertical circuit integration. When the boards are fired at low temperatures, passive components can be incorporated into the body of the package [2]. This shrinks the size of the circuit. Although offering the most benefits, multi-layer ceramics require an intense design effort. Good electrical performance hinges on detailed electromagnetic field analysis. Mechanically, various problems can occur in the layer stack (see Figure 5).

Sketch a design flow

Most RFIC designs adhere to a common flow. First, review the design specs. Understanding the spec flow-down process, the IC fabrication process and the package process, as well as knowing the limits of manufacturing, comprise a huge amount of information. Engineering teams are often dedicated to each. Second, divide the component into layers. Due to ground plane leakage and die radiation, the layers are never fully separate. Consider merging layers.

Third, design the component from the inside out. Calibrated RF on-wafer testing makes the die the best-defined layer. Adjust input/output ports on the die and package pads to meet the RF performance. When optimizing, determine the degree of fit needed. Characterize and model each layer, selecting the best hardware and software to use. Understand the limits of each characterization method. The primary difficulty is translating mechanical package tolerances to electrical performance.

Conclusion

Most RFIC designers limit their understanding of the package to a simple RF lumped-element equivalent-circuit model. The major RF variations in the package usually depend on less than 20 percent of the circuit elements. Finding which are the critical ones is the challenge. A detailed characterization effort gives a better understanding of the package's contribution.

Some RF applications are more forgiving of packaging mistakes than others. In linear amplifiers and power amplifiers, simply increasing the gain a few tenths of a dB overcomes package losses. When package parasitics lead to oscillation, the solution is not so simple. Some applications are especially sensitive to package parasitics. Examples are low-noise amplifiers and filters. These can require more than 50 dB of sensitivity. Such sensitivity is affected by package reactances less than 100 pH or 100 fF. The application often determines the degree of package modeling required. ■

References

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