

# Converter Enables Cost-Effective Software-Defined Radio Architectures for Base Stations

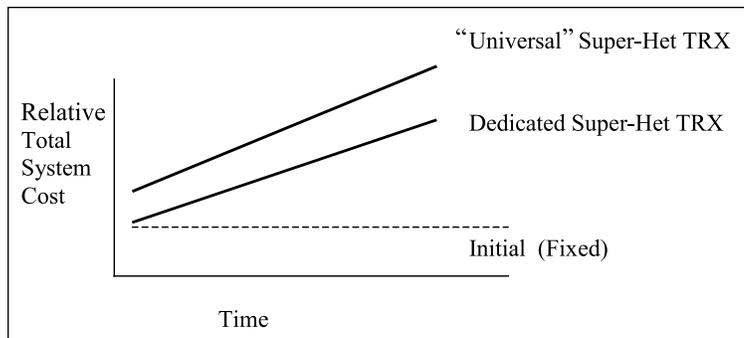
**By Jon Hall**  
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Software-defined radio (SDR) has been touted as the savior in wireless base station transceiver designs. Unfortunately, its realization has been hampered by the lack of commercially available components. A key component in the SDR system capability is the digitizer, or the analog-to-digital converter (ADC), such as the AD6645 from Analog Devices. This 14-bit/105 million samples per second (MSPS) ADC allows system designers to push more of the signal processing into the digital domain, thus offering more system flexibility and higher field reliability. This article discusses the challenges in an SDR system and how the AD6645 helps solve them.

A key to any transceiver system design is operational flexibility and field reliability. Within the cellular infrastructure market, these two goals are major concerns for service providers. While each is an element of the total system cost, there is a trade off between a system supporting various operating modes and its field reliability.

## Classic transceiver approaches

In the past, a transceiver system utilized the highest performance analog and digital components available and, in most cases, this dictated the signal processing architecture, such as a single carrier, super-heterodyne radio configuration. This configuration is simple to design but is more complex at the system level since redundant components are needed to support multiple standards and additional channels. This

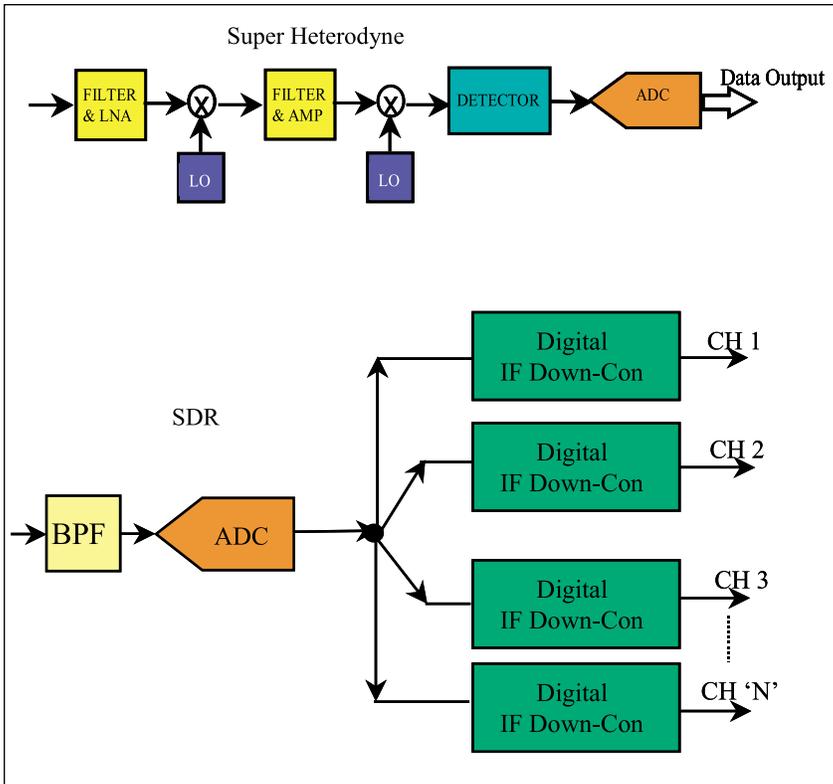


▲ Figure 1. Total system costs for a dedicated transceiver (TRX) platform versus a “universal” transceiver.

redundancy increases reliability concerns and leads to the increased field operational cost.

A super-heterodyne transceiver can be designed to take into account all possible physical scenarios, i.e., sharing a platform between service providers and support of multiple air interface standards, for example, UMTS, CDMA2000 or cdmaOne. Although this might be attractive in terms of performance and flexibility, having redundant components for each required signal chain and equivalent signal-processing algorithms for multiple air interface standards is costly. Operational cost increases if a change is needed after deployment and a technician must reconfigure the transceiver system.

A transceiver system optimized for a single air interface standard poses less of a field reliability concern because it is simpler than a “universal” superheterodyne system. What is lost is the ability to reconfigure the transceiver, which means the service provider is forced to purchase a new transceiver subsystem. In general, service providers and original equipment manufactur-

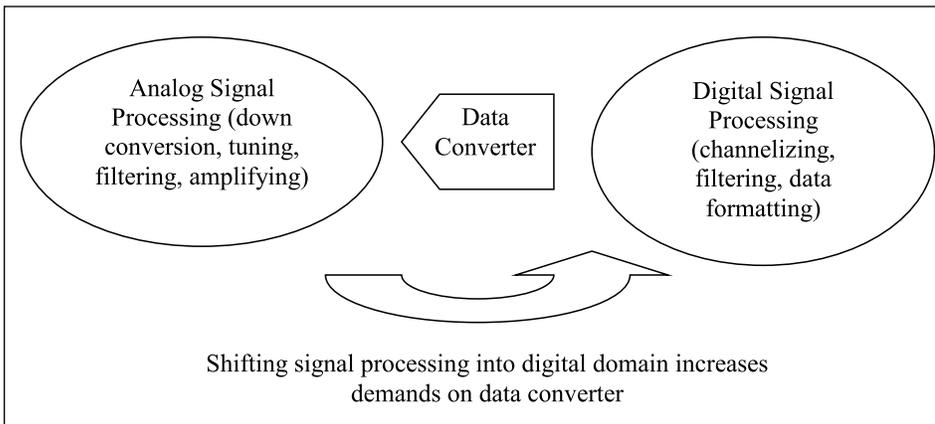


▲ Figure 2. Traditional superheterodyne receivers versus SDR receiver architecture.

ers (OEMs) of transceiver systems have struck a balance between available feature sets and operational complexity. This balance has been a function of available sub-component technologies, the cost of operations and the market dynamics within the service provider's territory.

**Software-defined radio: increased processing content**

SDR shifts signal-processing demands from the analog to the digital domain, reducing analog component susceptibility to environmental changes and requires fewer subcomponents. The net result is a more configurable transceiver system with lower total system costs.



▲ Figure 3. Shift in overall signal processing.

This places a higher performance burden on the data converter that must then support higher sampling rates and resolutions. For example, a dedicated standard receiver for second generation (2G) air standards commonly uses a superheterodyne architecture with an 8- or 10-bit data converter sampling less than 30 MSPS.

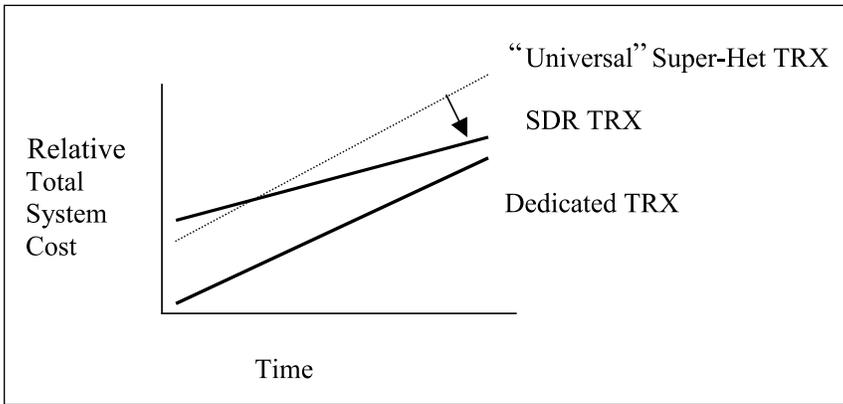
Dynamic performance requirement for a 2G system is dictated by the fact it is co-located from a spectrum point of view with a first generation (1G) system. Consequently, the dynamic range requirements translates to greater than 100 dB to combat the inherent blockers within the same spectrum. A 3G SDR receiver increases the spectrum bandwidth requirement by at least a factor of 20 for a single carrier architecture. For a multi-carrier receiver platform, the bandwidth requirement can be as high as 20 MHz, with dynamic requirements needing to be at least 65 dB SNR and -82 dBc SFDR over the entire bandwidth at a higher input frequency.

**14-bit 105 MSPS ADC converter**

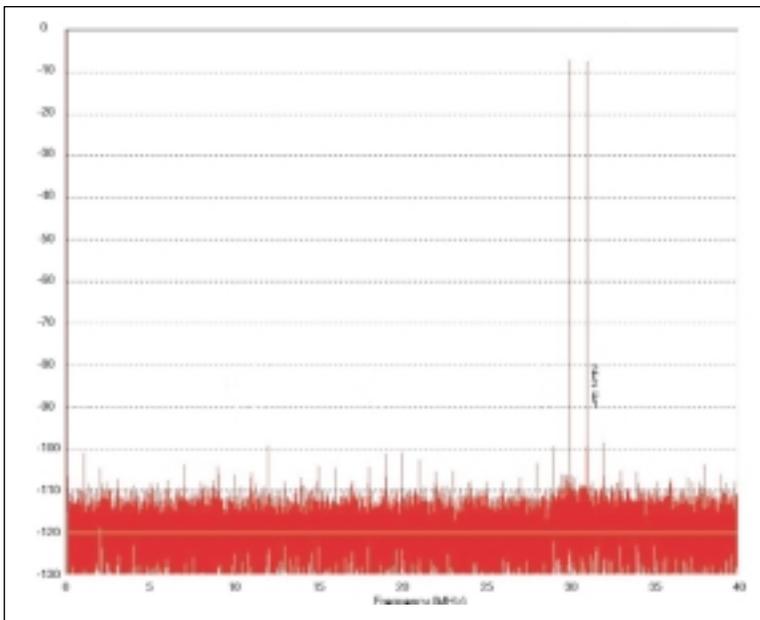
A data converter capable of supporting these requirements is the recently announced AD6645. This 14-bit/105 MSPS ADC enables multicarrier, multi-mode transceiver base station architectures with high signal quality and a configurable air interface. A fast conversion rate supports more cost-effective transceiver designs for two reasons. First, it enables intermediate frequency (IF) sampling, thus eliminating a down-conversion stage and associated components. The reduced part count improves transceiver reliability. Second, a fast conversion rate reduces costs by requiring less expensive analog filters and takes advantage of the inherent processing gain achieved by oversampling, such as 24 times the chip rate (92.16 MSPS), in a 3G transceiver.

The SNR of 74 dB with a 70 MHz input provides sufficient performance to support multi-carrier 3G wireless architectures and thus further reduces analog component redundancy. The SFDR of 89 dB with a 70 MHz input meets 3G blocking specifications.

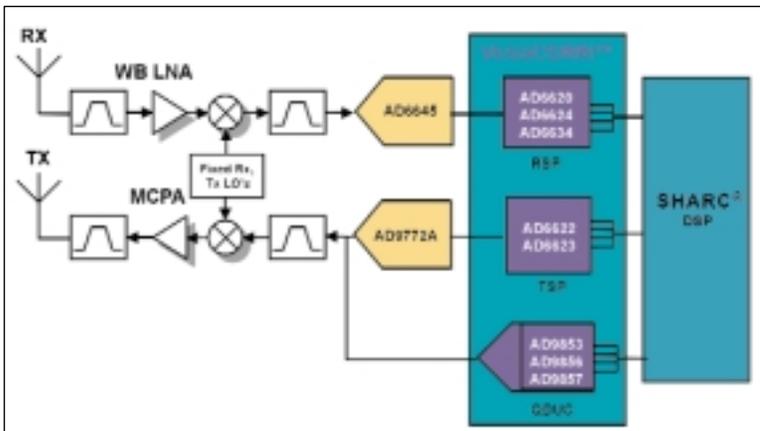
The AD6645 is packaged in a thermally enhanced 52-lead PowerQuad® 4. It is available in two speed grades, 80 and 105 MSPS, priced at \$54 and \$75, respectively, in quantities of 1,000 or more pieces.



▲ Figure 4. SDR TRX versus dedicated superheterodyne TRX.



▲ Figure 5. AD6645 two-tone spectral plot. 16K FFT, 76.8 MSPS, with 30 and 31 MHz (-7 dBFs) input.



▲ Figure 6. SDR architecture with a complement of Analog Devices Solutions.

## Other SDR components for 3G

ADI offers complete all-air-interfaces base station signal chain solutions, including analog RF and IF signal processing, data conversion and digital signal processing. Additional devices are an extension of the core technology found in the AD664x family of high-performance converters and are a part of ADI's SoftCell™ multicarrier transceiver chipset, which includes components from ADI's VersaCOMM™ digital converters, TxDACs™, ADCs and the SHARC® family of DSPs. These functional blocks are the keys to implementing a software-radio transceiver.

The receiver front end of an SDR consists of an analog RF downconverter that converts the desired sign band to an IF for digitization. This downconversion is followed by the AD6645 or another high-performance analog to digital converter. After the digitization of this IF, the output is processed by a receive-signal processor (RSP), such as the VersaComm digital converter family of products. This RSP, typically a dual or quad channel, provides tuning and channel filtering. The output of the RSP consists of a channel-filtered digital IF signal requiring only demodulation by a DSP, such as the TigerSharC DSP product family. In the transmit direction, the DSP sends modulated digital data to a transmit-signal processor (TSP), also a part of the VersaComm digital converter family of products, for further modulation. This data is then converted into the analog domain using a high-performance digital to analog converter, such as the AD9772A or AD9777, where it is up converted to the desired RF frequency.

## Summary

The AD6645 makes an SDR-based transceiver possible. SDR flexibility hedges against the reality of evolving standards and uncertainty of deployment strategies. The reduced complexity in analog signal processing and overall subcomponent count reduces both repair and overall operational costs. ■

## Author information

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