Low-Cost MMDS Upconverter for Outdoor Applications

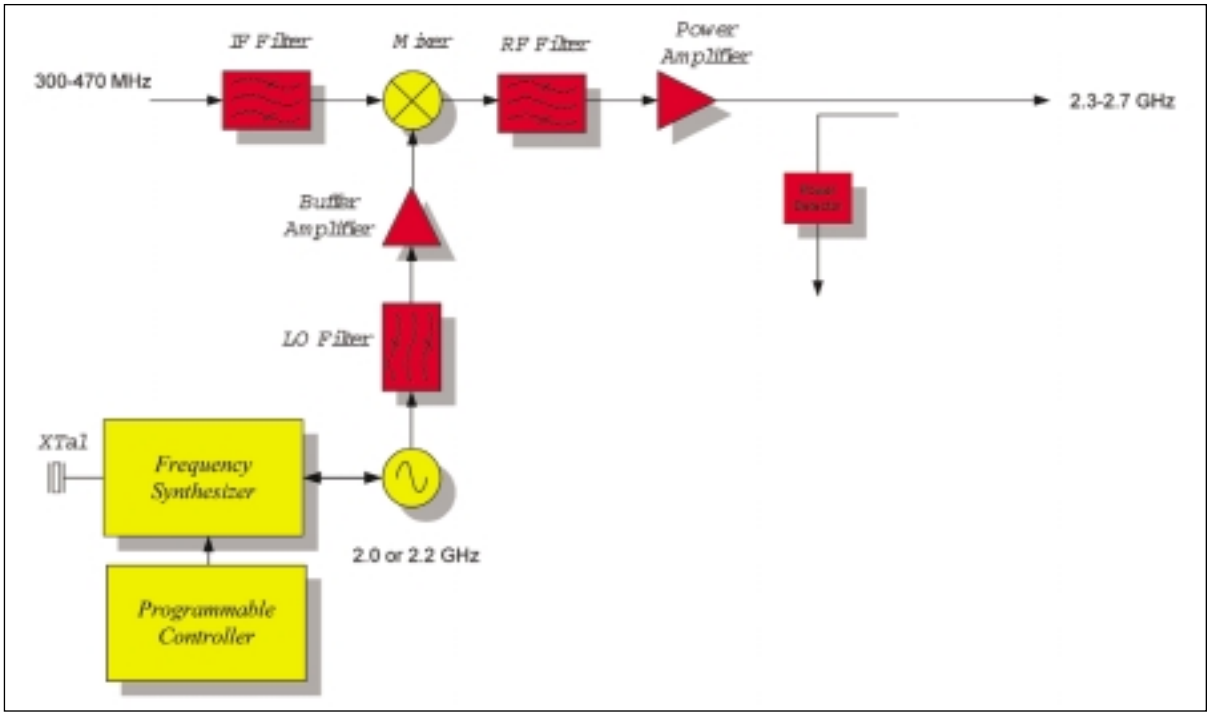
By Yorgos E. Stratakos
HELIC S.A.

This article discusses a low-cost homodyne hybrid multichannel multipoint distribution service (MMDS) upconverter. The design of the radio frequency (RF) bandpass filter shows a sharp out-of-band response and, therefore, permits the use of a single phased-locked oscillator for the upconversion of the intermodulation frequency (IF) signal to the total MMDS band (2.3 to 2.7 GHz).

Two separate bands for the MMDS standard are common: one from 2.3 to 2.5 GHz and the other from 2.5 to 2.7 GHz. The new system was developed on a low-cost Rogers RO4003 substrate material in microstrip, except for the filter, which was implemented in stripline geometry. The spurious emissions of the upconverter were well below 55 dBc and the intermodulation distortion (IMD) performance was excellent.

Introduction

Fixed broadband wireless systems have become more important because of the worldwide last mile problem. Bandwidth hunger, and the inability of standards such as Bluetooth™ 802.11b to cover the demand for more bandwidth have driven the development of more advanced radios both in the fixed and mobile wireless marketplace. The MMDS fixed wireless



▲ **Figure 1. MMDS upconverter system layout.**

▲ **Figure 2. Layout of the stripline bandpass filter.**

standard is well established, and the frequency of operation permits the use of low-cost materials and components to develop a complete upconverter for outdoor use.

The primary goal for this MMDS upconverter was to use low-cost materials and fabrication techniques. The block diagram of the upconverter is shown in Figure 1. The IF bandwidth is 300 to 470 MHz, with an input power of 0 dBm. The phased-locked oscillator is controlled via a serial bus phased-locked loop (PLL), which locks the local oscillator (LO) frequency to either 2.0 or 2.2 GHz.

The filter is a seventh-order Chebyshev bandpass stripline structure. Stripline was chosen because it has equal even and odd mode propagation velocities, lower transmission loss, higher out of band rejection and suppression of even order parasitic passbands.

Special care was taken to suppress unwanted harmonics, such as those at IF frequencies and the LO frequencies. In the IF stage, a fifth-order Chebyshev filter was based on typical surface-mount technology, which exhibits an insertion loss of less than 1 dB and an out-of-band rejection of more than 50 dB.

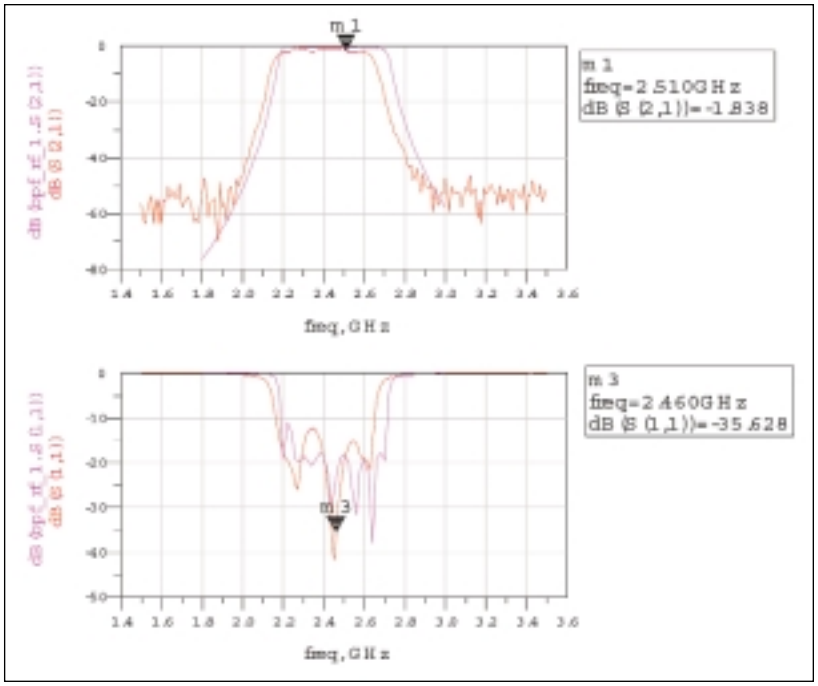
The LO filter is a third-order Chebyshev microstrip bandstop. It suppresses the second- and third-order harmonics by more than 60 dB. Phase noise of the LO is well below –100 dBc at the 100 kHz frequency offset. A buffer amplifier allows the LO output to raise the power level to drive the high IP3 double balanced mixer. Also, it serves as a buffer to prevent frequency pushing or pulling due to mixer impedance changes to the RF or IF.

The RF filter is a seventh-order Chebyshev in stripline. It exhibits an insertion loss of less than 2.5 dB with rejection in the LO frequency band of more than 60 dBc. This is a crucial point in the aspect of the upconverter, since the rejection of the RF filter limits the output level of spurious signals. At the mixer input, the LO level is approximately +13 dBm, which is at least 20 dB higher than the IF signal. The mixer is a balanced device as well as RF filter and is also crucial to the performance of the upconverter.

The power amplifier (PA) operates at class A with an output power of 2 watts. The PA is a four-stage design with a linear gain of 55 dB and voltage standing wave ratio (VSWR) at both ports of less than 2.0. The system is housed in a machined aluminum housing with cavities to prevent crosstalk between the LO and output PA.

The design was simulated at the system level and the circuit level using Advanced Design System (ADS) 1.5 from Agilent Technologies. Table 1 summarizes a set of specifications for this upconverter (see Appendix).

The upconverter DC power is applied through the RF input connector via a built-in low-loss RF bias tee. The overall DC power consumption is approximately 20 watts. Considering the output power is approximately 2 watts CW, the power-added efficiency of the system is 10 percent.

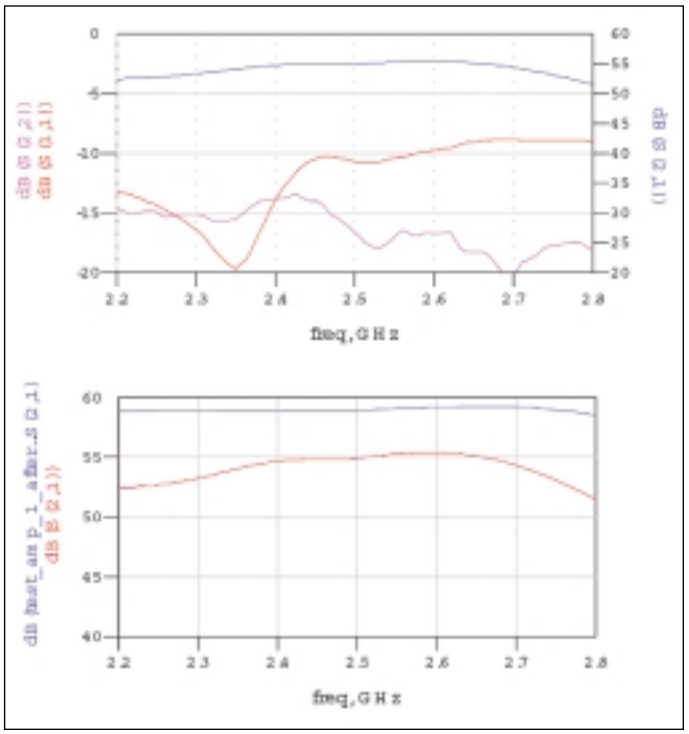


▲ **Figure 3. Simulation and experimental results of the stripline filter.**

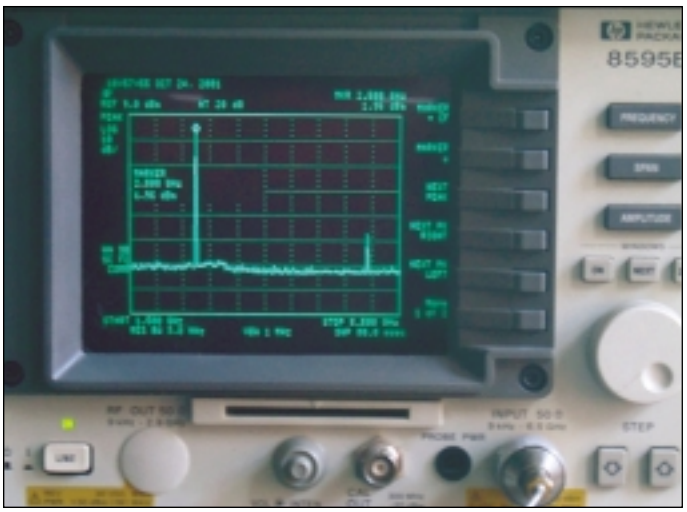
RF bandpass filter

The bandpass filter is a seventh-order Chebyshev hairpin in stripline. The layout of the filter is shown in Figure 2. The dimensions are 6.1 × 1.6 cm. In Figure 3, the filter simulation and experimental results of the *S*-parameters are given.

Good agreement of simulation and experimental results was achieved. The ultimate out-of-band rejection at the LO frequency is limited to 50 dBc instead of 60 dBc due to the substrate surface waves leaking from the input to output.



▲ **Figure 4. *S*-parameters simulation and experimental results of the power amplifier.**



▲ **Figure 5. Spectrum analyzer display of the output spectrum of the power amplifier.**

Power amplifier

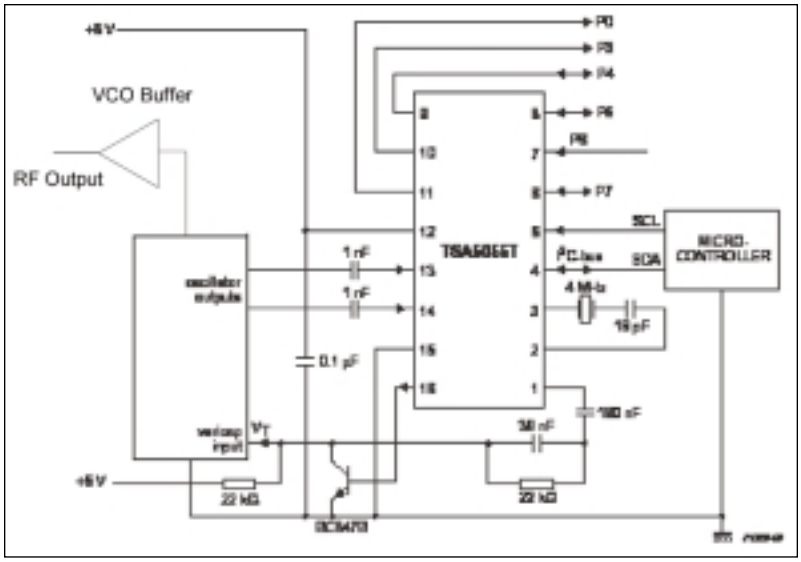
The PA is a four-stage microstrip design with active biasing. It uses two GAL-5 amplifiers from Mini-Circuits, an LP-1500 from Filtronics and a MGF 0909A from Mitsubishi. This design provides gain and output power stabilization versus temperature and component aging. A custom-developed smart start-up and switch-off function uses a single-positive power supply. The occupied area is approximately 12 × 5 cm, excluding the bias circuitry. Protection circuitry incorporates fuses, forward and zener diodes. Transistor selection was based on low cost, large signal performance and reliability.

Figure 4 shows the simulation and experimental results of the PA. Figure 5 shows the measured output power spectrum of the PA. The second harmonic is –45 dBc at the operating point of the amplifier. The simulated and measured gain differ by 4 dB, probably because of inaccuracies in the nonlinear model of the transistor.

Phased-locked oscillator

The phased-locked oscillator is JTOS-2200 PA, a VCO from Mini-Circuits that exhibits a phase noise of –112 dBc at 100 kHz offset. The VCO is phase locked using a Philips TSA-5055TA, which is programmed by a integrated circuit controller through the I2C bus.

The schematic of the phase-locked oscillator is shown in Figure 6. The output low-pass filter suppresses the harmonics to –60 dBc. VCO harmonics prior to filtering are –15 dBc. Several via holes help suppress undesired spurious.

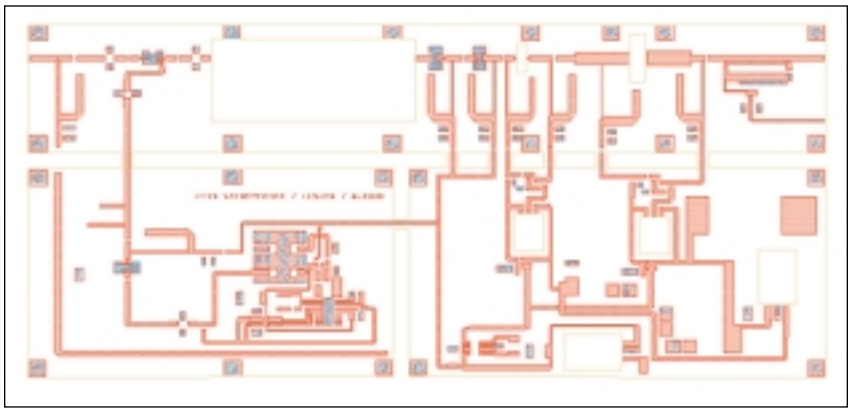


▲ **Figure 6. Schematic of the phase-locked oscillator.**

Final layout

The final layout of the MMDS upconverter is shown in Figure 7. The occupied area is 24 × 12 cm. Figure 7 also shows the outline walls used to eliminate spurious oscillations due to feedback. The RF bandpass stripline filter window is shown in the top left corner. Electromagnetic simulations helped to establish the 3D geometry for the enclosure. This is crucial since the gain of the four-stage PA is 55 dB.

Figure 8 shows the inside view of the MMDS upconverter. The shielding walls and microwave circuitry are shown. The next step will be to reduce the size and the linearity of the upconverter. ■



▲ **Figure 7. MMDS upconverter final layout.**

2. *Design Manuals ADS 1.5*, Agilent Technologies.
3. *Design Manuals HFSS 5.6*, Agilent Technologies.
4. Product Datasheets, Mini-Circuits.
5. Product Datasheets, Mitsubishi Semiconductors.
6. Product Datasheets, Filtronic Solid State.
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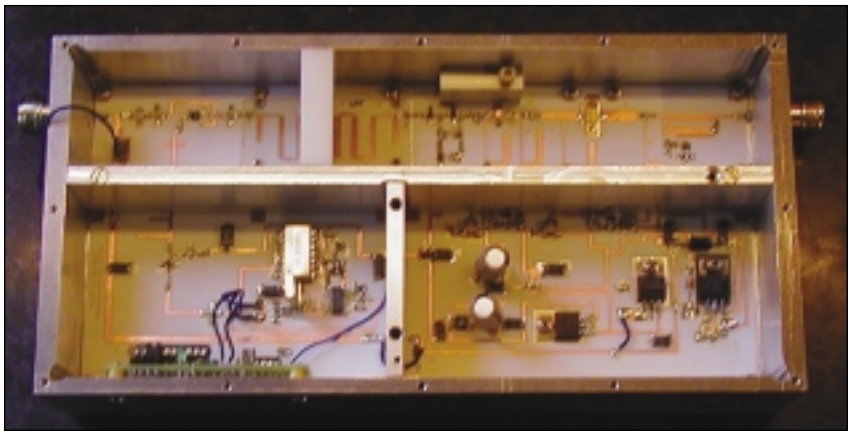

▲ **Figure 8. MMDS upconverter inside view.**

Author information

Dr. Yorgos Stratakos is vice president of engineering and product development at HELIC S.A., a fabless wireless semiconductor company in Argyroupolis, Greece. His research interests include microwave and millimeterwave telecommunication systems, radar, microwave CAD linear and nonlinear techniques, MIC and MMIC design, conformal array systems, adaptive antennas and automated microwave measurement techniques, and advanced packaging techniques. He has contributed to projects RACE, ACTS, COST, ESPRIT and national programs. He may be reached via E-mail: Y.Stratakos@helic.com; Tel: +30109949390; or Fax: +30109949399.

Appendix A

Specification	Goal	Simulation	Measurement
IF frequency range	300 to 470 MHz	300 to 470 MHz	300 to 470 MHz
RF frequency range	2.3 to 2.7 GHz	2.3 to 2.7 GHz	2.3 to 2.7 GHz
IF input power level	0 dBm	0 dBm	0 dBm
RF output power level At 1 dB compression point	1.0 watts	1.5 watts	1.5 watts
Spurious emissions	< 58 dBc	< 62 dBc	< 57 dBc
Return loss in	< 2.0	< 1.7	< 1.4
Return loss out	< 2.0	< 1.7	< 2.0
Power conversion gain compression at 1 dB	41 dB	42 dB	42 dB
Output third order intercept point	+45 dB	+45 dB	+45 dB
Noise figure	10 dB	10 dB	10 dB
Third-order intermodulation products	< 50 dBc	< 55 dBc	< 55 dBc
Power supply	15 VDC/2.5 A	15 VDC/2.5 A	15 VDC/2.2 A
Box dimension	$24 \times 12 \times 1.5$ cm^3	$24 \times 12 \times 1.5$ cm^3	$24 \times 12 \times 1.5$ cm^3
Phase noise at frequency offset of 100 kHz	–100 dBc	–105 dBc	–100 dBc

▲ **Table 1. Specification goals, simulated and measured results for the MMDS upconveter.**