Class E High-Efficiency Power Amplifiers: Historical Aspect and Future Prospect

By Andrei Grebennikov
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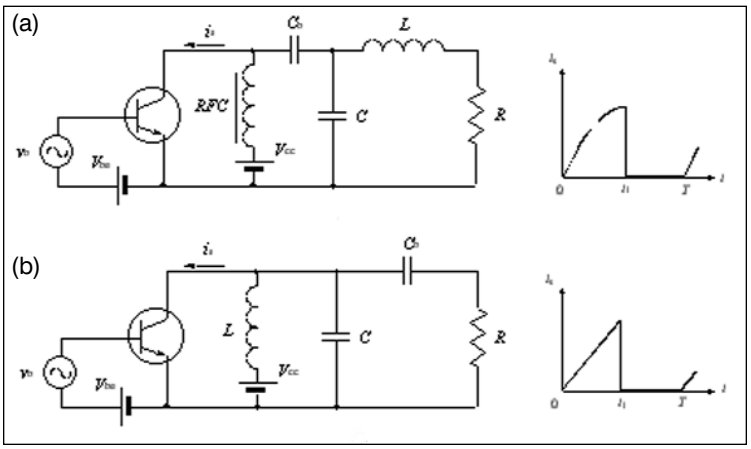
This is part one of a two-part article. The second part will be published in the August 2002 issue of Applied Microwave & Wireless *magazine.*



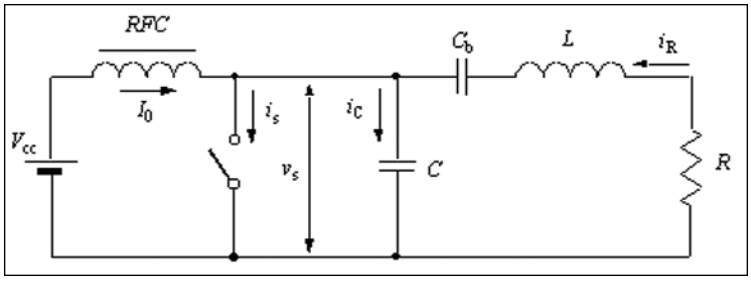
▲ **Figure 1. Single-ended switching power amplifiers with (a) shunt capacitance and series inductance and (b) parallel circuit.**

Class E tuned power amplifiers provide output power from several kilowatts at low radio frequency (RF) ranges up to about 1 watt at microwaves. In Class E power amplifiers, the transistor operates as an on-to-off switch and the shapes of the current and voltage waveforms do not overlap simultaneously to minimize the power dissipation and maximize the power amplifier efficiency. This mode is realized for resonant power amplifiers by an appropriate choice of the values of the reactive elements in its output matching circuit, which is mistuned at the fundamental frequency. Thus, conjugate matching is not performed and increased power amplifier efficiency is achieved at the expense of decreased power gain. However, if the active device has a f_T much higher than the operating frequency, it is possible to realize high efficiency and high gain.

Consider the main achievements of Class E power amplifiers from a historical perspective. In 1966, Lohrman described experiencing the possibility of achieving increased efficiency by mistuning the output matching circuits [1]. Three years later, Artym [2] and Gruzdev [3] presented a theoretical analysis of single-ended switching mode power amplifiers and the calculation of their circuit parameters. The analysis also included a second resonant circuit tuned on the fundamental to provide a sinusoidal output signal [2]. Later, Popov [4] and Kozyrev [5] provided a generalized analysis of the performance and circuit parameters of single-ended switching power amplifiers with shunt capacitance C and series inductance L (see Figure 1(a)) and with parallel LC circuit (see Figure 1(b)). Because these analyses appeared only in Russian, they were overlooked worldwide. These writings contain, however, interesting theoretical results and practical circuit configurations for the successful design of modern RF and microwave switching-mode power amplifiers.

Class E with shunt capacitance

Single-ended switching power amplifiers with shunt capacitance as a Class E power amplifier was introduced by Sokal in 1975 and has found widespread application due to its design simplicity and high efficiency [6]. The characteristics of



▲ **Figure 2. Basic equivalent circuit of Class E power amplifier with one inductance and one capacitance.**

a Class E power amplifier can be determined by finding its steady-state collector voltage and current waveforms.

The most basic circuit of a Class E power amplifier is shown in Figure 2. The loading L-type network consists of the shunt capacitance C and inductance L connected in series with the load R. The shunt capacitance C is comprised of the intrinsic device output capacitance and the external circuit capacitance. The collector of the transistor is connected to the supply voltage by the choke inductance with a high reactance at the fundamental frequency. The active device is considered to be an ideal switch that is driven to provide device switching between one and off states. As a result, the collector voltage waveform is determined by the switch when it is on and by the transient response of the loading network when the switch is off.

To simplify the analysis of Class E power amplifiers, the following assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance and infinite off resistance. Its switching action is instantaneous and lossless (except when discharging the shunt capacitance).
- The total shunt capacitance is independent of the collector and is assumed to be linear.
- The RF choke allows only a constant direct current (DC) and has no resistance.
- There are no losses in the circuit except the load R.

The following analysis for L-type circuits (see Figure 2) is found in [3]. For a lossless operation, the following conditions are optimum for the voltage across the switch just prior to the start of switch on at the moment $t = T$, when the transistor is saturated:

$$\begin{cases} v_s(t)\big|_{t=T} = 0 \\ \left.\dfrac{dv_s(t)}{dt}\right|_{t=T} = 0 \end{cases} \tag{1}$$

where T is the period of input driving signal and v_s is the voltage across the switch. When the switch is on, the system of differential equations is

$$\begin{cases} V_{cc} = L\dfrac{di_R(t)}{dt} + i_R(t)R \\ i_s(t) = I_0 + i_R(t) \end{cases} \tag{2}$$

where the voltage V_{cc} is applied to the plates of the bypass capacitor C_b.

Taking into account that $i_L = 0$ at $t = 0$, the current flowing through the switch is

$$i_s(t) = \frac{V_{cc} + I_0 R}{R}\left[1 - \exp\left(-\frac{R}{L}t\right)\right] \tag{3}$$

If at the moment $t = t_1$ switch is off, then another system of differential equations can be written

$$\begin{cases} V_{cc} = v_s(t) + L\dfrac{di_R(t)}{dt} + i_R(t)R \\ C\dfrac{dv_s(t)}{dt} = I_0 + i_R(t) \end{cases} \tag{4}$$

and the initial conditions are the finite values of Equation (3) as

$$i_R(t_1) = i_s(t_1) - I_0, \quad v_s(t_1) = 0 \tag{5}$$

Hence, the voltage v_s across the switch is

$$v_s(t) = (V_{cc} + I_0 R)\left[1 + \frac{1}{\omega}\sqrt{d^2 + \omega^2}\exp(-\delta t)\sin(\omega t + \varphi)\right] \tag{6}$$

where

$$\omega_0 = 1/\sqrt{LC},\ \delta = \frac{R}{2L} = \frac{\omega_0}{2Q},\ d = \frac{i_s(t_1)}{(E + I_0 R)}\frac{1}{C} - \delta,$$
$$\varphi = \tan^{-1}\left(\frac{\omega}{d}\right),\ \omega = \sqrt{\omega_0^2 - \delta^2}$$

As a result, by satisfying the optimum condition (1), the equations for peak collector voltage v_{smax}, DC current I_0, maximum operation frequency f_{max} and circuit parameters can be calculated. Thus, for a 50 percent duty cycle when $t_1 = 0.5T$,

$$R = 0.35\frac{V_{cc}^2}{P_{out}},\ L = 1.75\frac{R}{\omega},\ C = \frac{1}{4.5\omega R},$$

where $P_{out} = I_0 V_{cc}$ is the output power at the idealized lossless operation conditions.

However, to provide such an idealized switching operation mode, the loaded quality factor of this *L*-type circuit should be sufficiently small. This means that harmonics in the load are high, about 5 to 15 percent [4, 5]. For additional harmonic suppression, the load is connected through a series filtering circuit tuned on the fundamental, such as a simple *LC*-filter shown in Figure 3(a). The loaded quality factor Q_L of the series resonant L_0-C_0 circuit tuned to

$$\omega_0 = 1/\sqrt{L_0 C_0}$$

should be high enough to provide the required harmonic suppression.

For the theoretical analysis, the active device is replaced by an ideal switch (see Figure 3(b)), which is followed by a generalized approach, as given in [5]. We define switch on as τ and switch off as τ_2. Then the switch is closed during $\Delta\tau = \tau_2 - \tau_1$, where $\tau = \omega\tau$. We assume that the losses in the reactive circuit elements are negligible, the quality factor of the loaded L_0-C_0 circuit is high and $i_R(\tau) = I_R \sin\tau$ is the fundamental current flowing into the load.

When switch is on for $\tau_1 < \tau < \tau_2$, the voltage $v_s(\tau) = 0$, the current through the capacitance

$$i_C(\tau) = \omega C \frac{dv_s}{d\tau} = 0$$

and

$$i_s(\tau) = I_0 + i_R(\tau) = I_R(\sin\tau - \sin\tau_1) \tag{7}$$

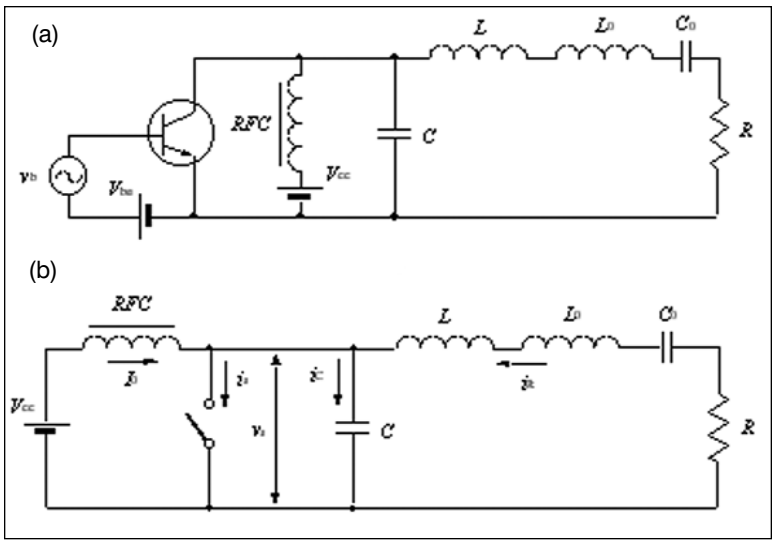
where the DC component $I_0 = -I_R \sin\tau_1$ is defined using the initial condition $i_s(\tau_1) = 0$. When the switch is off for $\tau_2 < \tau < 2\pi + \tau_1$, the current through the switch is equal to zero, i.e., $i_s(\tau) = 0$. Hence, the current through the capacitance *C* is defined by

$$i_C(\tau) = I_0 + i_R(\tau) - I_R(\sin\tau - \sin\tau_1) \tag{8}$$

whereas the voltage across the switch is

$$v_s(\tau) = \frac{1}{\omega C}\int_{\tau_2}^{\tau} i_C(\tau)d\tau = \frac{I_R}{\omega C}\left[\cos\tau_2 - \cos\tau + \sin\tau_1(\tau_2 - \tau)\right] \tag{9}$$

Taking into account that $v_s(2\pi+\tau_1)=0$ from Equation (9), it follows



▲ **Figure 3. Equivalent circuits of Class E power amplifiers with series *LC*-filter.**

$$\cos\tau_2 - \cos(2\pi + \tau_1) + \sin\tau_1(\tau_2 - 2\pi - \tau_1) = 0 \tag{10}$$

and substituting $\tau_2 = \tau_1 + \Delta\tau$ gives

$$\tau_1 = \tan^{-1}\left(-\frac{1-\cos\Delta\tau}{2\pi - \Delta\tau + \sin\Delta\tau}\right) \tag{11}$$

The fundamental voltage $v_{s1}(\tau)$ applied to the switch terminals consists of two quadrature components whose amplitudes can be found using Fourier formulas by

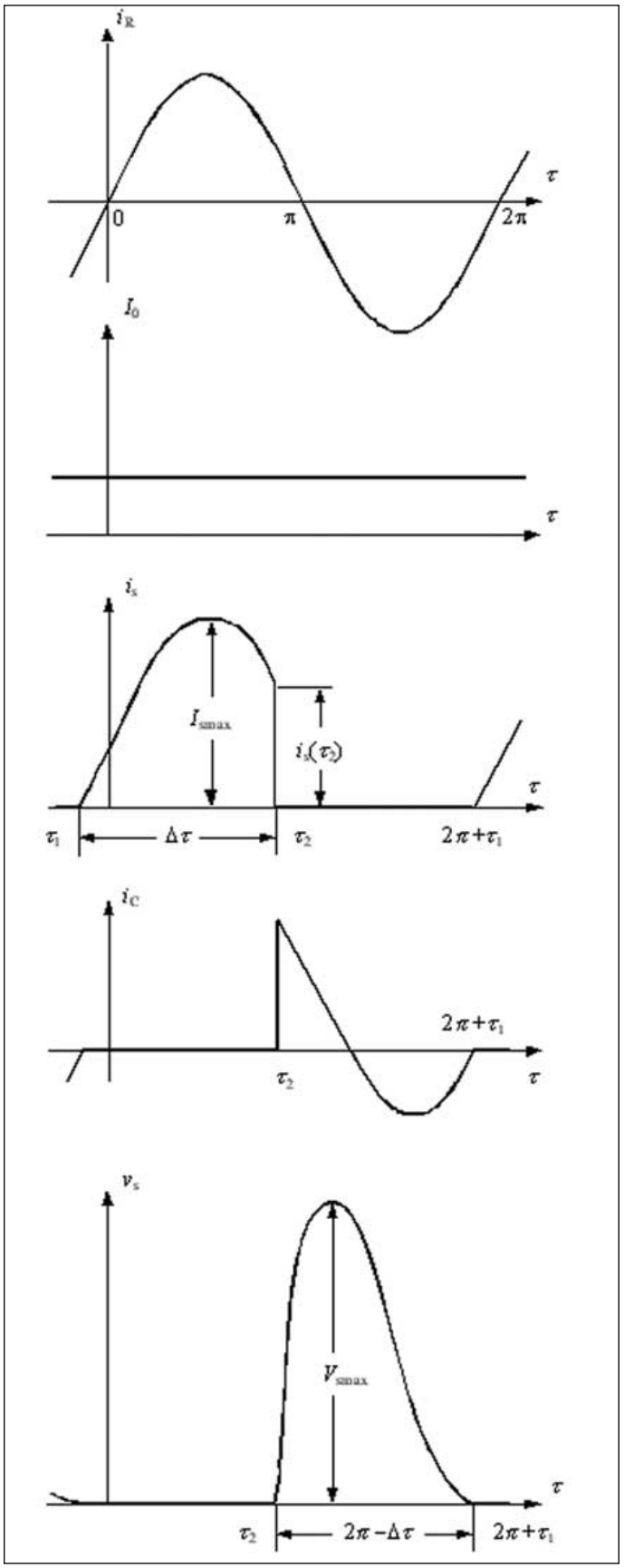
$$V_R = -\frac{1}{\pi}\int_{\tau_2}^{2\pi+\tau_1} v_s(\tau)\sin\tau\, d\tau = I_R R$$

$$V_L = -\frac{1}{\pi}\int_{\tau_2}^{2\pi+\tau_1} v_s(\tau)\cos\tau\, d\tau$$

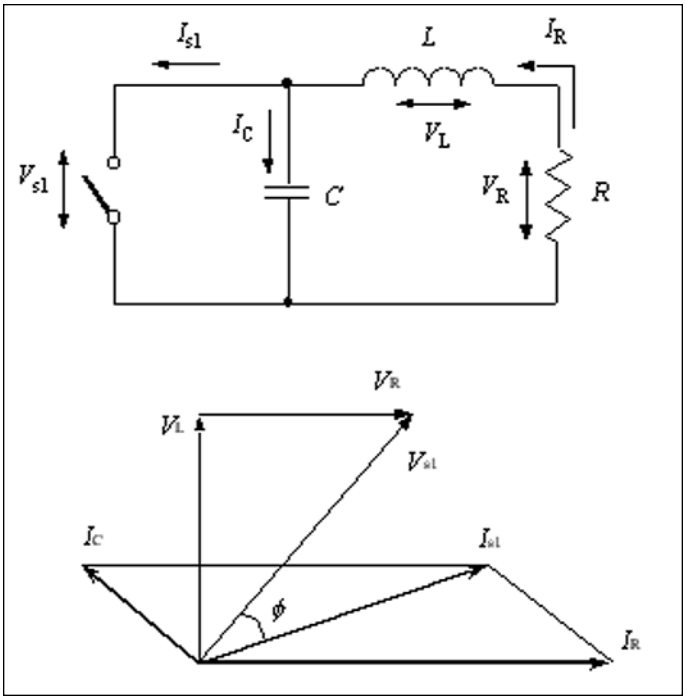
As a result, the normalized loading network parameters as functions of $\Delta\tau$ are

$$l = \frac{\omega L}{R} = \frac{V_L}{V_R} \qquad c = \omega C R = \frac{\omega C V_R}{I_R}$$

Figure 4 shows the voltage and current waveforms for optimum Class E operation with shunt capacitance. When the transistor is turned on, there is no voltage across the switch and the only sinusoidal current i_s with DC component I_0 flows through the device. When the transistor is turned off, the sinusoidal current continues to flow, but now only through the shunt capacitance *C*.



▲ **Figure 4. Voltage and current waveforms for optimum Class E operation with shunt capacitance.**



▲ **Figure 5. Fundamental voltage and current phasors for equivalent circuit diagram corresponding to Class E power amplifier with shunt capacitance.**

As a result, there is no nonzero voltage and current simultaneously and the lack of power loss gives an idealized collector efficiency of 100 percent. Figure 5 shows the phasors of the fundamental voltages and currents for the equivalent circuit diagram for the Class E tuned power amplifiers with shunt capacitance.

An alternative theoretical analysis of a Class E power amplifier with shunt capacitance was given by Raab [7]. The sinusoidal output current is assumed to be

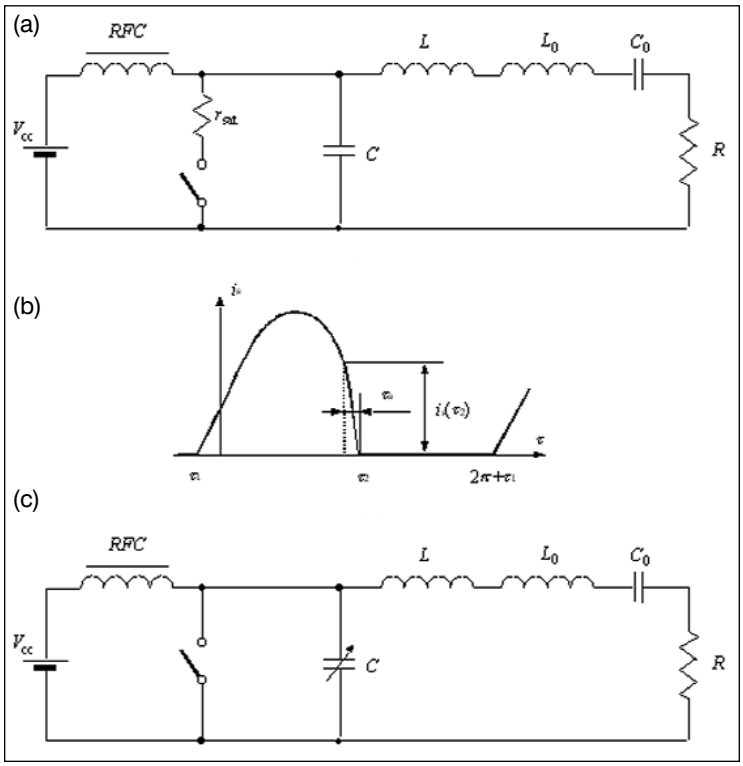
$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{12}$$

where φ is the initial phase shift.

Using the Fourier circuit analysis and simplifying to a 50 percent duty cycle, the normalized steady-state voltage and current waveforms are

$$\frac{v_s(\omega t)}{V_{cc}} = \begin{cases} 0 & \\ \pi\left[\omega t - \dfrac{3\pi}{2} - \dfrac{\pi}{2}\cos\omega t - \sin\omega t\right] & \\ 0 < \omega t \le \pi & \\ \pi < \omega t \le 2\pi & \end{cases} \tag{13}$$

$$\frac{i_s(\omega t)}{I_0} = \begin{cases} \dfrac{\pi}{2}\sin\omega t - \cos\omega t + 1 & 0 < \omega t \le \pi \\ 0 & \pi < \omega t \le 2\pi \end{cases} \tag{14}$$



▲ **Figure 6. Equivalent Class E loading networks (a) with saturation resistance, (b) current waveform with finite time delay and (c) nonlinear capacitance.**

and the phase angle φ is equal to

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482^\circ \tag{15}$$

which is equal to the value of phase shift τ_1 from Equation (11) for $\Delta\tau = \pi$ or 180 degrees.

The peak collector voltage V_{smax} and current I_{smax} can be determined by differentiating the waveforms given by Equations (13) and (14), respectively, and setting the results equal to zero, which gives

$$V_{s\max} = -2\pi\varphi\, V_{cc} = 3.562 V_{cc} \tag{16}$$

and

$$I_{s\max} = \left(\frac{\sqrt{\pi^2+4}}{2}+1\right) I_0 = 2.8621 I_0 \tag{17}$$

The optimum parameters of the loading network are determined by

$$L = \frac{R}{\omega}\tan 49.052^\circ \tag{18}$$

$$C = \frac{1}{\omega R}\frac{8}{\pi\left(\pi^2+4\right)} = \frac{1}{5.4466\omega R} \tag{19}$$

$$R = \frac{8}{\pi^2+4}\frac{V_{cc}^2}{P_{out}} = 0.5768\frac{V_{cc}^2}{P_{out}} \tag{20}$$

$$C_0 = \frac{1}{\omega R Q_L} \qquad L_0 = \frac{1}{\omega^2 C_0} \tag{21}$$

It is important to know the maximum frequency of efficient operation. The approximate maximum frequency of optimum Class E operation is

$$f_{\max} = \frac{1}{\pi^2\left(\sqrt{\pi^2+1}+2\right)}\frac{I_{\max}}{CV_{cc}} \cong \frac{I_{\max}}{56.5\, CV_{cc}} \tag{22}$$

The high-Q_L assumption can lead to considerable error if its value is too small [8]. For example, for a 50 percent percent duty cycle the values of the circuit parameters for the loaded Q less than unity can differ by several tens of percents. For $Q_L \geq 7$, the errors are less than 10 percent and become less than 5 percent for $Q_L \geq 10$. Also, it is necessary to consider the finite value of the RF choke inductance [9].

The above analytical analysis for idealized Class E operations does not consider the losses caused by nonideal active device properties, for example, the finite saturation resistance r_{sat} and finite time between "on" and "off." The second effect is a result of the base charge changes to zero with a certain time delay τ_s. As a result, the base charge process rather than the appropriate loading network determines the collector current waveform during this transistion. For the equivalent circuit shown in Figure 6(a) with given supply voltage V_{cc}, output power P_{out} and a 50-percent duty cycle, the averaged dissipated power P_{sat} is [4]

$$P_{sat} \cong \frac{8}{3}\frac{r_{sat}P_{out}^2}{V_{cc}^2} \tag{23}$$

The losses at the active stage due to the finite time between "on" and "off" operation conditions described by the active phase loss power P_a are approximately [5]

$$P_a \cong \frac{\tau_a^2}{12} \qquad for\ \Delta\tau = 100 \div 260^\circ \tag{24}$$

where τ_a is the duration of the active stage shown in Figure 6(b). The loss at the active phase is generally

small. For example, for τ_a = 0.35 or 20 degrees, it is only 1 percent.

Typically, the intrinsic output device capacitance is nonlinear (see Figure 6(c)). If its contribution to the overall shunt capacitance is large, it is necessary to consider its nonlinear nature when specifying the breakdown voltage. In the case of an abrupt junction of the output capacitance rather than a linear junction, the maximum voltage can be increased by about 20 percent for a 50-percent duty cycle [10]. A further increase of 1.5 to 2 times can exist for longer $\Delta\tau \geq 210$ degrees [5]. The nonlinear nature of this capacitance should also be considered when determining the series inductance.

The second part of this article will address switching mode with parallel circuit, Class E with shunt inductance, broadband Class E and Class E with transmissions lines. ■

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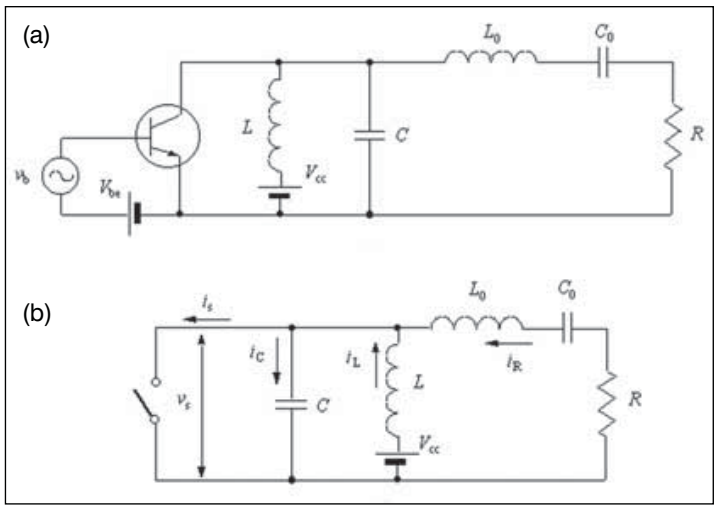
This part of this article will address switching mode amplifiers with parallel circuit, Class E amplifiers with shunt inductance, broadband Class E amplifiers and Class E amplifiers with transmission lines.

Switching mode with parallel circuit

In Figure 7(a), a switching-mode tuned power amplifier with parallel circuit is shown. For the theoretical analysis, it should replace the active device by the ideal switch (see Figure 7(b)) and a generalized approach given in [5] is followed. If we assume that losses in the reactive circuit elements are negligible, the quality factor of the loaded L_0-C_0 circuit is high and $i_R(\tau) = I_R \sin \tau$ is the fundamental current flowing into the load, when switch is on for $\tau_1 < \tau < \tau_2$,



▲ **Figure 7. Eqivalent circuits of Class E power amplifiers with a parallel circuit.**

$$i_s(\tau) = i_L(\tau) + i_R(\tau) = \frac{V_{cc}}{\omega L}(\tau - \tau_1) + I_R(\sin\tau - \sin\tau_1) \quad (25)$$

where

$$i_L(\tau) = \frac{1}{\omega L}\int_{\tau_1}^{\tau} V_{cc}\,d\tau + i_L(\tau_1) = \frac{V_{cc}}{\omega L}(\tau - \tau_1) - I_R \sin\tau_1$$

When the switch is off for $\tau_2 < \tau < 2\pi + \tau_1$, the current $i_C(\tau) = i_L(\tau) + i_R(\tau)$ flowing through the capacitance C is:

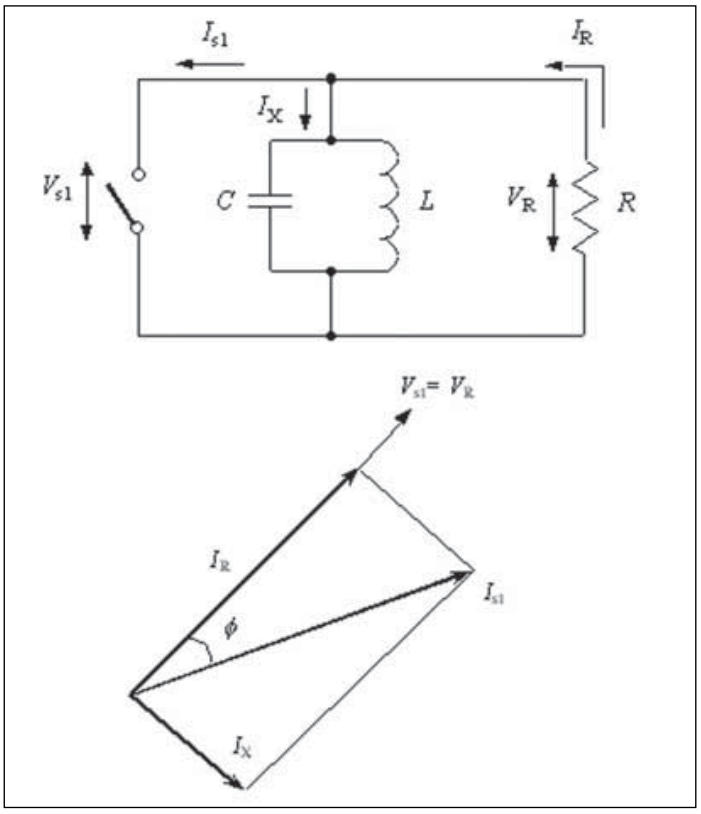
$$\omega C \frac{dv_s(\tau)}{d\tau} = \frac{1}{\omega L}\int_{\tau_2}^{\tau}\left[V_{cc} - v_s(\tau)\right]d\tau + I_R \sin\tau \quad (26)$$

under the initial conditions

$$v_s(\tau_2) = i_C(\tau_2) = 0,$$

$$i_L(\tau_2) = \frac{V_{cc}}{\omega L}(\tau_2 - \tau_1) - I_R \sin\tau_1$$

The solution for Equation (26) is given using



▲ **Figure 8. Phasor diagram corresponding to a Class E power amplifier with a parallel circuit.**

Laplace transform in the form shown in Equation (27) (below), where

$$q = 1/\omega\sqrt{LC}$$

The fundamental-frequency current $i_{s1}(\tau)$ flowing through the switch consists of two quadrature components. Their amplitudes can be found using Fourier formulas by

$$I_R = \frac{1}{\pi}\int_{\tau_1}^{\tau_2} i_s(\tau)\sin\tau\, d\tau, \quad I_X = -\frac{1}{\pi}\int_{\tau_1}^{\tau_2} i_s(\tau)\cos\tau\, d\tau$$

The normalized circuit parameters, which are functions of $\Delta\tau$, are

$$l = \frac{\omega L}{R} = \frac{1}{2}\frac{\omega L}{V_{cc}}\frac{I_R^2}{I_0} \qquad c = \omega CR = \frac{1}{l} - \tan\varphi$$

$$v_s(\tau) = V_{cc}\left[1-\cos q(\tau-\tau_2)\right] + qi_L(\tau_2)\omega L\sin q(\tau-\tau_2) + \frac{q^2}{1-q^2}I_R\omega L\left[-\cos\tau+\cos\tau_2\cos q(\tau-\tau_2) - q\sin\tau_2\sin q(\tau-\tau_2)\right]$$

▲ **Equation (27).**

where

$$I_0 = \frac{1}{2\pi}\int_{\tau_1}^{\tau_2} i_s(\tau)\,d\tau$$

is the DC component,

$$\phi = \tan^{-1}\frac{I_X}{I_R}$$

is the phase angle between fundamental-frequency voltage and current at switch terminal, and I_R is defined with idealized switching conditions as

$$I_R = \sqrt{2V_{cc}I_0/R}$$

To determine the preliminary unknown parameter τ_1, an additional equation is required. According to the phasor diagram shown in Figure 8, the fundamental voltage component V_{s1} applied to the switch terminals has the same phase as the current I_R, so the reactive component V_X should equal zero, i.e.,

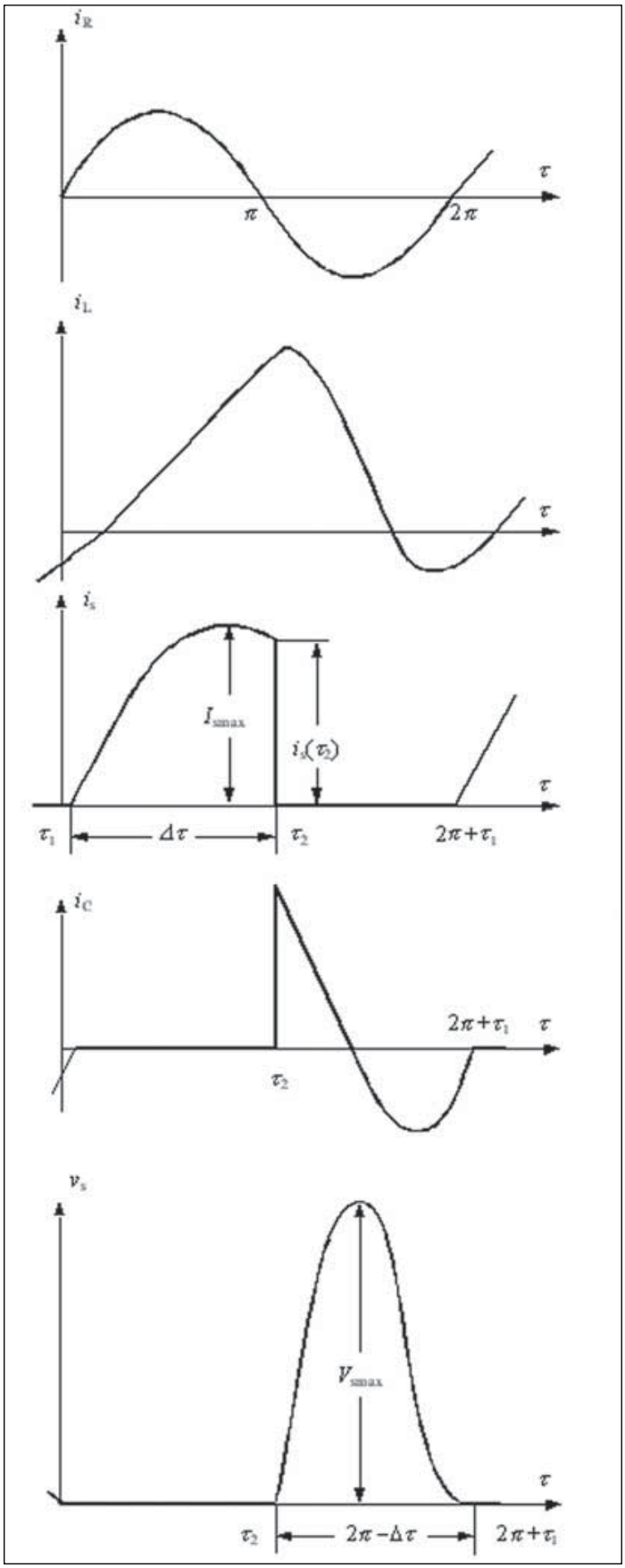
$$V_X = \frac{1}{\pi}\int_{\tau_2}^{2\pi+\tau_2} v_s(\tau)\cos\tau\, d\tau = 0$$

In Figure 9, the voltage and current waveforms for optimum operation with a parallel circuit are shown where the current flowing through the inductance L grows linearly when the transistor is turned on.

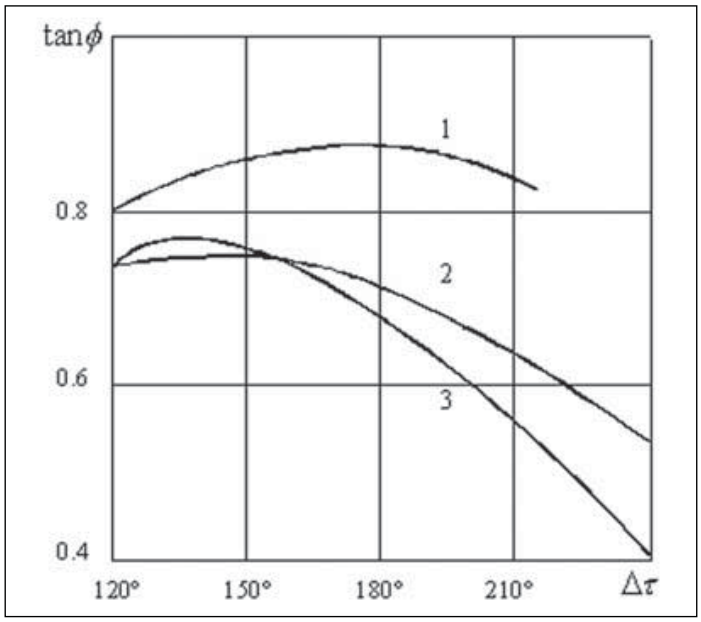
In Figure 10, the values of $\tan\phi$ for switching-mode tuned power amplifiers with shunt capacitance (curve 1 — without LC-filter, curve 2 — with LC-filter) and parallel circuit (curve 3) are given for different saturation time periods $\Delta\tau$ [5]. The similar phase angle ϕ for these different loading networks results from an optimum idealized operation mode, where the voltage waveforms are very similar and the current waveforms differ only slightly. Table 1 gives the normalized values of the circuit parameters for the different idealized loading networks [11].

Class E with shunt inductance

An alternate approach to the design of the Class E power amplifier with an efficiency of 100 percent under idealized operation conditions is to use shunt inductance [12]. Such a Class E power amplifier is similar to the Class E power amplifier with shunt capacitance but in this case the storage element is inductive. The basic circuit of a Class E power amplifier with shunt inductance is shown in Figure 11(a). The loading



▲ **Figure 9. Voltage and current waveforms for optimum Class E operation with a parallel circuit.**



▲ **Figure 10. Overall loading network phase angle for Class E tuned power amplifiers with shunt capacitance and a parallel circuit.**

circuit consists of the inductance L connected in parallel to the output active device terminals, the series capacitance C, the series filtering circuit L_0-C_0 tuned on the fundamental frequency

$$\omega_0 = 1/\sqrt{L_0 C_0}$$

and load resistance R.

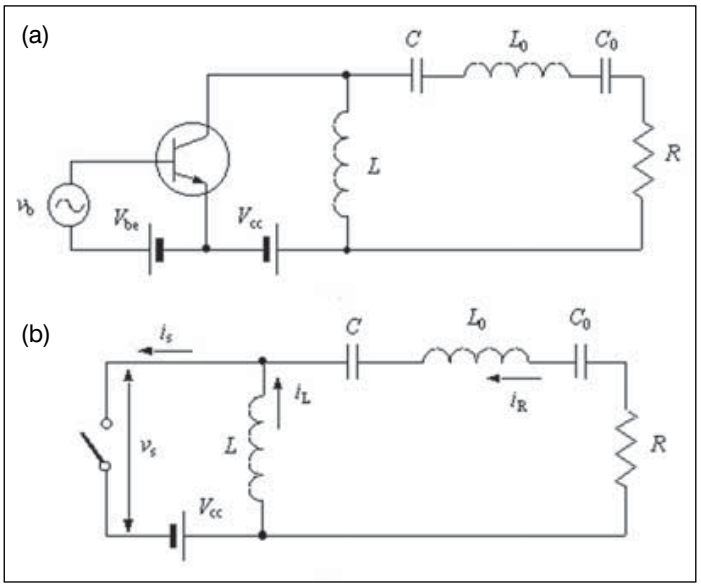
The Class E power amplifier with shunt allows us to eliminate power losses if the on-to-off state device current conditions are

$$\begin{cases} i_s(\omega t)\big|_{\omega t=2\pi} = 0 \\ \dfrac{di_s(\omega t)}{d(\omega t)}\Big|_{\omega t=2\pi} = 0 \end{cases} \tag{28}$$

when the transistor switches off at $\omega t = 2\pi$. These conditions are established with a proper loading network.

Loading network	Parameter	Duration of saturation period, $\Delta\tau$				
		120°	150°	180°	210°	240°
L-type	*c*	0.22	0.23	0.22	0.19	0.16
	l	3.17	2.28	1.83	1.39	1.13
L-type with filter	*c*	0.25	0.24	0.18	0.11	0.06
	l	2.15	1.55	1.14	0.86	0.63
Parallel with filter	*c*	2.12	1.27	0.67	0.32	0.15
	l	0.35	0.51	0.71	1.08	1.76

▲ **Table 1. Accurate values for inductance L_1.**



▲ **Figure 11. Class E power amplifiers (a) with shunt inductance and (b) equivalent power amplifier circuit.**

For the equivalent power amplifier circuit shown in Figure 11(b), the relationships between the voltages and current are

$$\begin{cases} i_s(\omega t) = i_L(\omega t) + i_R(\omega t) \\ v_s(\omega t) = V_{cc} - v_L(\omega t) \end{cases} \tag{29}$$

where the load current is sinusoidal and given by

$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{30}$$

with the parameters I_R and φ, which are to be determined.

Since when the switch is off and $i_s(\omega t) = 0$ for $0 < \omega t \le \pi$, then

$$i_L(\omega t) = i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{31}$$

and the voltage across the inductance L is given by

$$v_L(\omega t) = \omega L \frac{di_L(\omega t)}{d(\omega t)} = \omega L I_R \cos(\omega t + \varphi) \tag{32}$$

On the other hand, when the switch is on and $v_s(\omega t) = 0$ for $\pi < \omega t \le 2\pi$, then

$$v_L(\omega t) = V_{cc} \tag{33}$$

and the current flowing through the inductance L is

$$i_L(\omega t) = \frac{V_{cc}}{\omega L}(\omega t - \pi) - I_R \sin\varphi \tag{34}$$

As a result, the following normalized collector voltage and current waveforms are

$$\frac{i_s(\omega t)}{I_0} = \begin{cases} 0 \\ \pi\left[\omega t - \dfrac{3\pi}{2} - \dfrac{\pi}{2}\cos\omega t - \sin\omega t\right] \end{cases} \tag{35}$$

$$0 < \omega t \le \pi$$

$$\pi < \omega t \le 2\pi$$

$$\frac{v_s(\omega t)}{V_{cc}} = \begin{cases} \dfrac{\pi}{2}\sin\omega t - \cos\omega t + 1 \\ 0 \end{cases} \tag{36}$$

$$0 < \omega t \le \pi$$

$$\pi < \omega t \le 2\pi$$

when

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i_s(\omega t)d(\omega t) = \frac{V_{cc}}{\pi\omega L}$$

$$I_R = V_{cc}\frac{\pi}{2\omega L\sin\varphi} = \frac{\pi\sqrt{\pi^2+4}}{2} I_0$$

and the phase angle

$$\varphi = \tan^{-1}\left(\frac{\pi}{2}\right) = 57.518°$$

The loading network parameters are

$$\frac{\omega L}{R} = \frac{\pi(\pi^2+4)}{8} = 5.4466 \tag{37}$$

$$\omega CR = \frac{16}{\pi(\pi^2+12)} = 0.2329 \tag{38}$$

$$R = \frac{V_{cc}^2}{P_{out}}\frac{8}{\pi^2(\pi^2+4)} = 0.05844\frac{V_{cc}^2}{P_{out}} \tag{39}$$

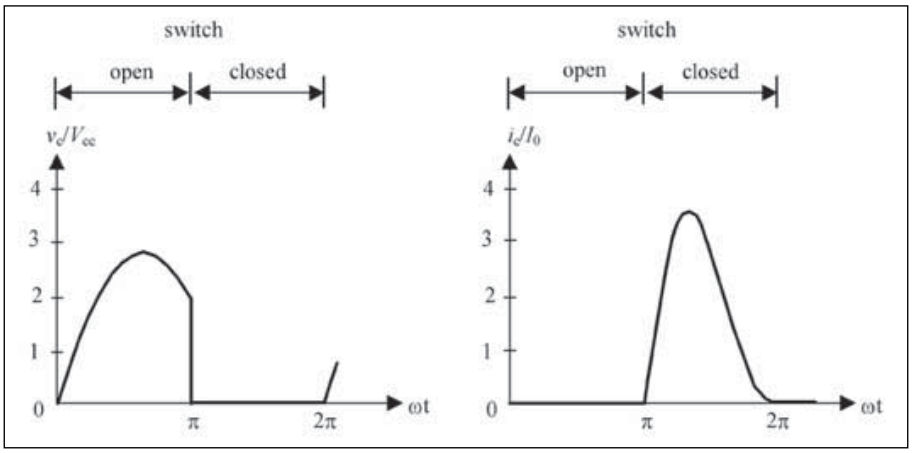
$$C_0 = \frac{1}{\omega R Q_L} \tag{40}$$

$$L_0 = \left[Q_L - \frac{\pi(\pi^2+12)}{16}\right]\frac{R}{\omega} = \tag{41}$$

$$(Q_L - 4.2941)\frac{R}{\omega}$$

where the optimum phase angle ϕ of the overall loading network with the shunt inductance and the series capacitance is calculated by using Equations (37) to (38) as ϕ = 35.945 degrees. Therefore, the input impedance of the loading network should be capacitive. The value of the quality factor QL is arbitrary but it should be greater than 4.2941.

From idealized voltage and current waveforms shown in Figure 12 it follows that, when the switch is open, the current through the device i_c is zero, and the current i_R is determined by the sinusoidal current i_L. However, when the switch is closed, the voltage v_c is zero and supply voltage V_{cc} produces the linearly increasing current i_L. The difference between the current i_L and current i_R flows through the switch.



▲ **Figure 12. Voltage and current waveforms for optimum Class E operation with shunt inductance.**

The previous analysis assumes zero device output capacitance. But at high frequencies, the effects of device capacitance are not negligible. In this case, the power amplifier operates in Class E with parallel circuit but the required idealized operations conditions must be realized with zero-current switching. However, the theoretical analysis given by [13] illustrates the infeasibility of a zero-current switching Class E power amplifier. This means that the harmonic impedance conditions should be different, being inductive for fundamental and capacitive for higher-order harmonics, which can be achieved only with zero-voltage switching conditions. Neverthe-less, such a Class E power amplifier with shunt inductance can be applied for RF power amplifiers when the device output capacitance is small.

Broadband Class E

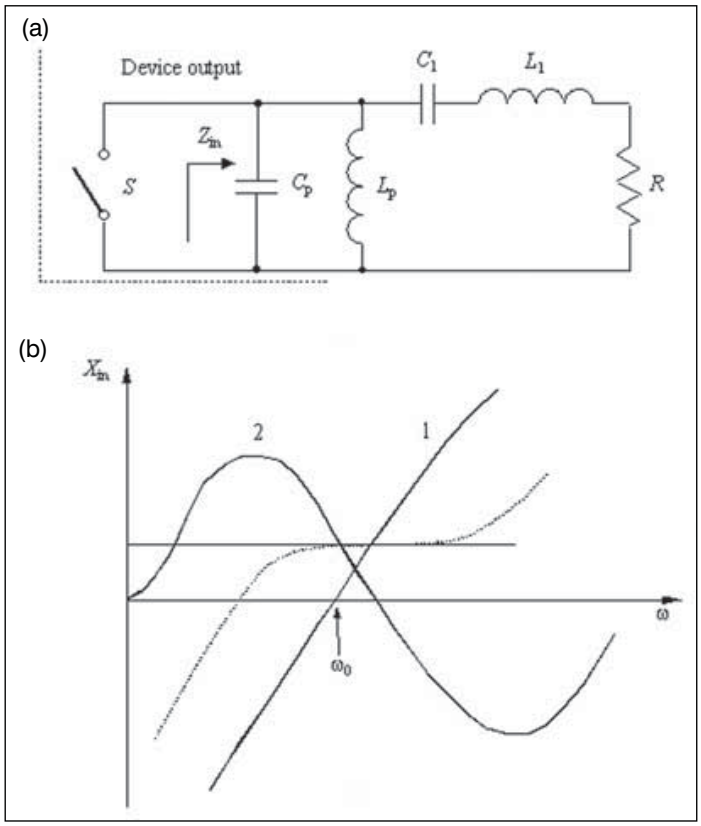
A high-efficiency broadband operation with the appropriate current and voltage waveforms requires a broadband loading network. For example, a simple loading network consisting of a series resonant LC circuit tuned on the fundamental and a parallel inductance provides a constant load phase angle in a frequency range of about 50 percent [14].

For example, consider the simplified equivalent loading circuit with a series L_1C_1 resonant circuit and a shunt L_pC_p circuit (see Figure 13(a)). The reactance of the series resonant circuit increases with frequency and decreases with frequency for the loaded parallel circuit near ω_0, as shown in Figure 13(b). By choosing the proper circuit elements, a constant load angle can be provided over a very large frequency bandwidth.

First, we define the required magnitude and phase angle of the loading network impedance at the device output terminals. For optimum Class E operation, the input impedance Z_{in} at resonant frequency with the shunt capacitance C_p and series L_s-L_0C_0-R resonant circuit in normalized form is

$$\frac{Z_{in}}{R} = \frac{1 + j\dfrac{\omega L_s}{R}}{1 + j\omega C_p R\left(1 + j\dfrac{\omega L_s}{R}\right)} \tag{42}$$

As a result, the magnitude and the phase of Z_{in} are



▲ **Figure 13. Single reactance compensation circuit and reactance compensation principle.**

$$\frac{|Z_{in}|}{R} = \frac{\sqrt{1+\left(\frac{\omega L_s}{R}\right)^2}}{\sqrt{\left(1-\frac{\omega L_s}{R}\omega C_p R\right)^2+\left(\omega C_p R\right)^2}} \quad (43)$$

$$\phi = \tan^{-1}\left(\frac{\omega L_s}{R}\right) - \tan^{-1}\left(\frac{\omega C_p R}{1-\frac{\omega L_s}{R}\omega C_p R}\right) \quad (44)$$

Since for ideal Class E operation with shunt capacitance, $\omega L_s/R = 1.1521$ and $\omega R C_p = 1/5.4466$, an optimum phase angle for the loading network is [15]

$$\phi = \tan^{-1}(1.1521) - \tan^{-1}(0.2329) = 35.945^\circ \quad (45)$$

The parameters of the series L_1C_1 resonant circuit are chosen to provide a constant phase angle of the loading network over a broadband frequency bandwidth. This bandwidth will be maximized if at resonance frequency ω_0

$$\left.\frac{dB(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0 \quad (46)$$

where $B(\omega) = -(1-\omega^2 L_p C_p)/\omega L_p$ is the loading network susceptance. As a result, the series capacitance C_1 and inductance L_1 are

$$L_1 = \frac{R}{\omega}\left(\tan 49.052^\circ - 0.5\tan 35.945^\circ\right) \quad (47)$$

$$C_1 = 1/\omega^2 L_1 \quad (48)$$

A wider bandwidth can be achieved using the double-resonant reactance compensation circuit shown in Figure 14, where L_1C_1 is the series resonant circuit and L_2C_2 is the parallel circuit. For circuit-loaded Q with values close to unity and higher, initial parameters of the series and shunt resonant circuits that are useful as a starting point for circuit optimization can be calculated from [15]

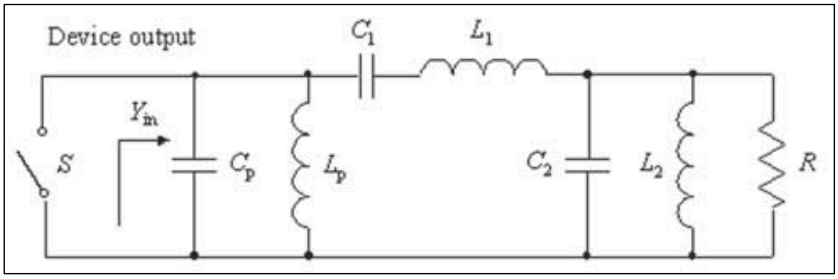
$$L_1 = \frac{2R}{\omega}\frac{\tan 49.052^\circ - 0.5\tan 35.945^\circ}{\sqrt{5}-1}$$
$$C_1 = \frac{1}{\omega^2 L_1} \quad (49)$$

$$C_2 = \frac{L_1}{R^2}\frac{3-\sqrt{5}}{2} \qquad L_2 = \frac{1}{\omega^2 C_2} \quad (50)$$

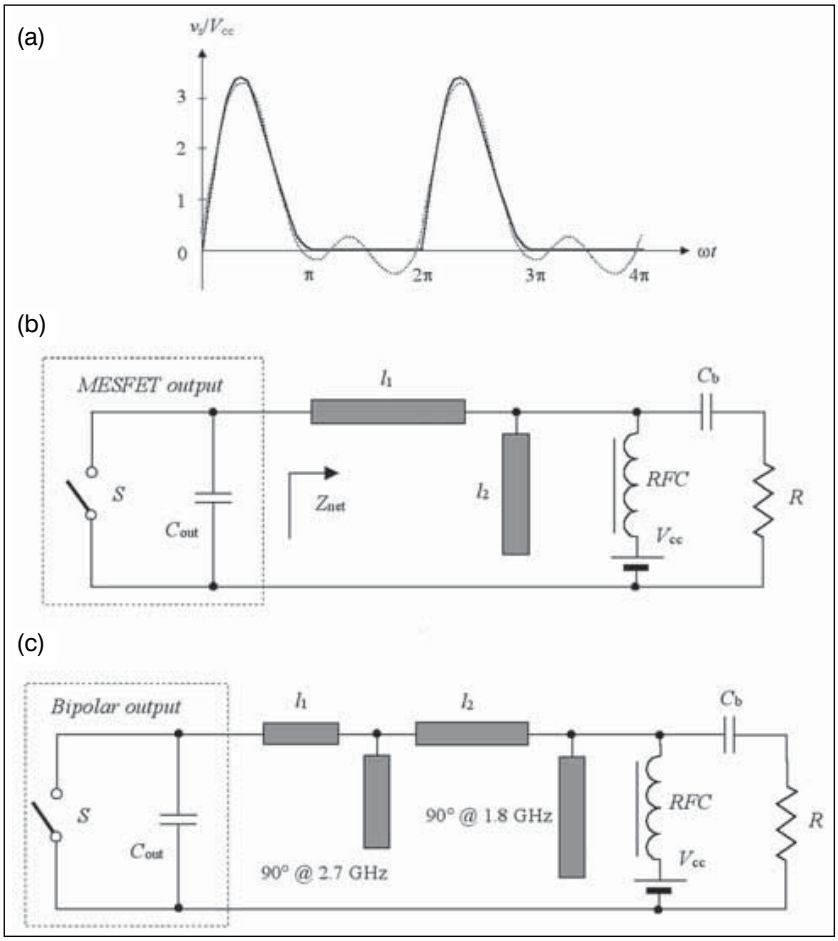
Equations (47) and (49) used the results of analysis of the L-type loading network. They serve as a good starting point for a further optimization of practical broadband Class E tuned power amplifiers.

More accurate values for inductance L_1 are obtained using Table 1 or more accurate procedures presented in [16].

Another approach for broader bandwidth



▲ **Figure 14. Double-resonant reactance compensation circuit.**



▲ **Figure 15. Two-harmonic voltage waveform and equivalent circuits of Class E power amplifiers with transmission lines.**

is to use the methods of broadband matching, for example, using low-pass Chebyshev filter-prototypes [8]. The third-order loading network with two parallel and one series resonant circuits shown in Figure 14 can be considered as the broadband matching circuit. In this case, for a given device output capacitance C_p, it is possible to determine the value of

$$g_1 = c(\Delta\tau)\left(\sqrt{K_\omega} - \frac{1}{\sqrt{K\omega}}\right) \tag{51}$$

where $K_\omega = \omega_{max}/\omega_{min}$, ω_{max} is the upper bandwidth frequency and ω_{min} is the lower bandwidth frequency. The remaining coefficients are taken from well-known tables or optimized numerically for minimum amplitude ripple. At higher operating frequencies when the influence of the device output lead inductance is significant, the Norton transform [16] may be used.

Loading network	Parameter	Duration of saturation period, $\Delta\tau$				
		120°	150°	180°	210°	240°
L-type	*c*	0.22	0.23	0.22	0.19	0.16
	l	3.17	2.28	1.83	1.39	1.13
L-type with filter	*c*	0.25	0.24	0.18	0.11	0.06
	l	2.15	1.55	1.14	0.86	0.63
Parallel with filter	*c*	2.12	1.27	0.67	0.32	0.15
	l	0.35	0.51	0.71	1.08	1.76

▲ **Table 1. Accurate values for inductance L_1.**

Class E with transmission lines

For microwave power amplifiers, inductances in the output matching circuit can be realized by transmission lines to reduce power loss. The transmission-line loading network should satisfy the required idealized optimum impedance at the fundamental frequency given by

$$Z_{net1} = R(1 + j\tan 49.052°) \tag{52}$$

Equation (52) is obtained from Equation (42) with zero parallel capacitance using Equations (19) and (20) for idealized Class E operation with shunt capacitance. Open-circuited conditions should be realized at all higher-order harmonics. However, as determined by Fourier analysis, a good approximation to Class E mode is obtained with only two harmonics (fundamental and the second) of the voltage waveform across the switch [17].

In Figure 15(a), the voltage waveform containing two harmonics (dotted line) is plotted along with the ideal waveform (solid line). Applying this approach, a Class E power amplifier with series microstrip line l_1 and open-circuited stub l_2 with equivalent circuit is shown in Figure 15(b). This amplifier was designed for microwave applications. The electrical lengths of lines l_1 and l_2 are chosen to be of about 45 degrees at the fundamental to provide an open circuit condition at the second harmonic and their characteristic impedances are calculated to satisfy the required inductive impedance at the fundamental. The output lead inductance of the packaged device is accounted for by a shortening the length of l_1.

The collector efficiency is improved by controlling the load impedance at the second and third harmonics [18]. This network consists of separate open-circuited quarter-wave stubs at both the second harmonic and third (see Figure 15(c)). The third-harmonic quarter-wave stub is located before the second-harmonic stub. It is possible to achieve very high collector efficiency even with values of device output capacitance higher than conventionally required, at the expense of lower output power. As a result, maximum collector efficiencies over 90 percent for power amplifiers with an output power of 1.5 watts can be realized at 900 MHz. ■

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