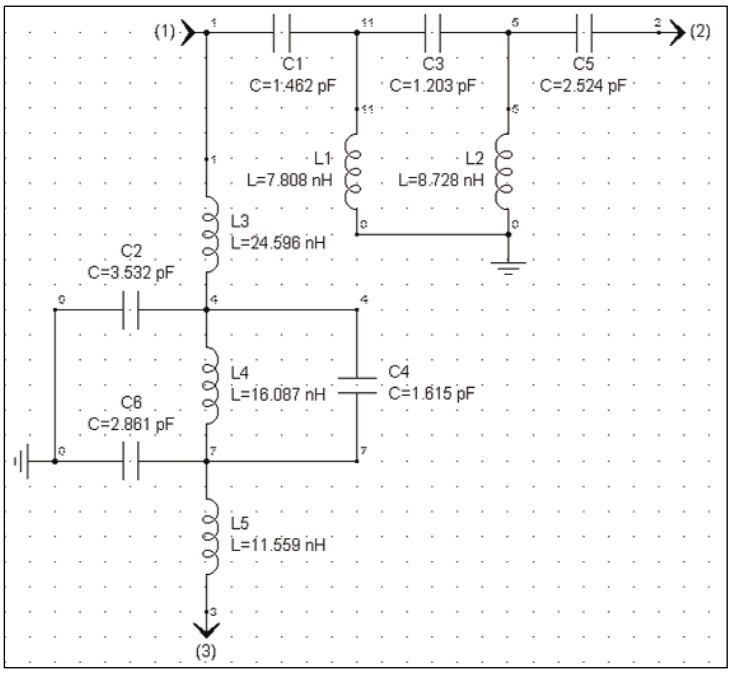
A Diplexer Using Meander Lines

By Peter Nordquist
MicroSignals, Inc.

Editor's note: This article describes the empirical development of a compact hybrid diplexer. The author aptly begins his engineer to engineer story with the quote, "A journey of a thousand miles begins with a single step."

As a filter engineer at MicroSignals since 1991, I have had a hand in designing, prototyping and manufacturing various passive components, such as couplers, filters and splitters. The project described here is the development of a hybrid (chip capacitor/distributed inductor) diplexer utilizing a one-sided construction technique. The project began with a customer request and specifications for a high-pass/low-pass diplexer. This 75-ohm, three-port device has a high-pass output, a low-pass output and a common port. The low pass covers 400 to 700 MHz, and the high pass covers 950 to 2150 MHz. The diplexer application was in the intermediate frequency (IF) of a local multipoint distribution service (LMDS) system.



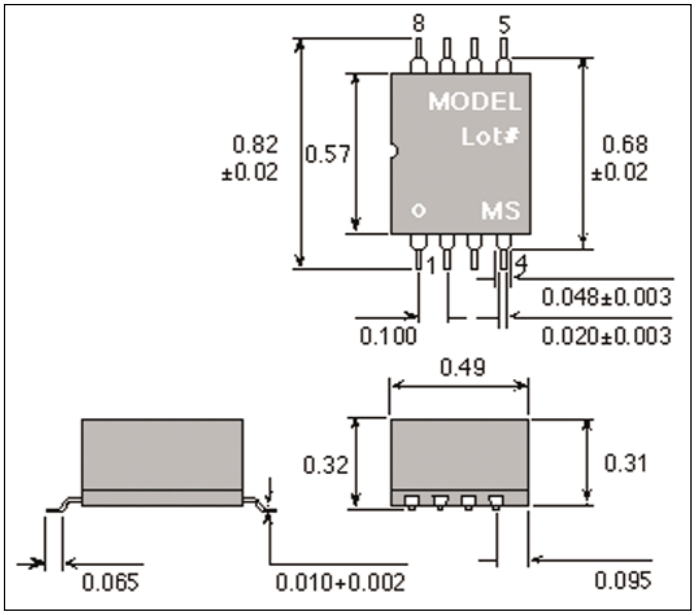
▲ **Figure 1. Schematic design generated on Eagleware's GENESYS version 7.52 software.**

An initial design

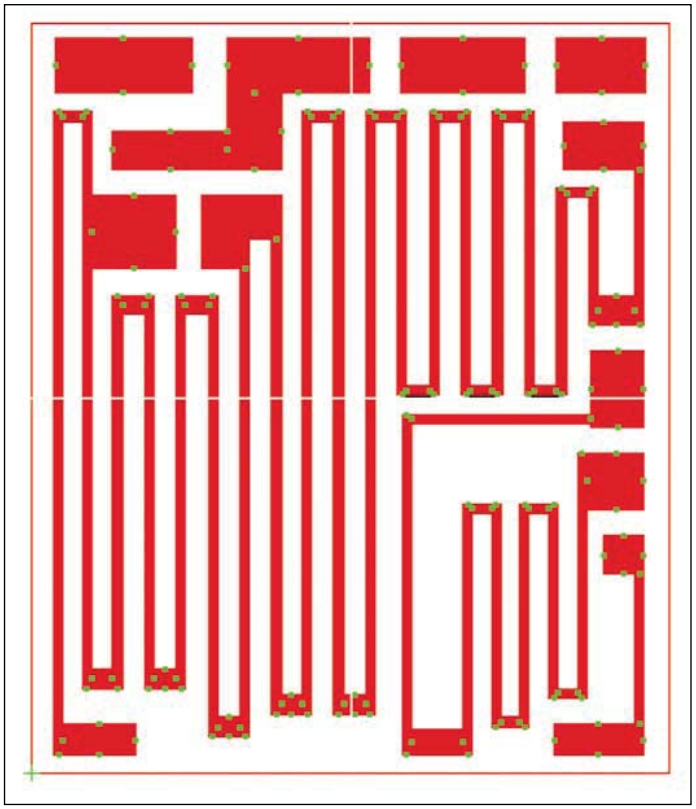
In this case, fifth order for both the high-pass and low-pass sections was sufficient to meet the required shape factor and specifications. The initial target specifications were 1 dB maximum loss in the pass bands and 30 dB minimum attenuation in the stop bands. The stop bands were above 700 MHz for the low pass and below 950 MHz for the high pass.

MicroSignal's senior engineer, Michael Magnin, designed a lumped-element version with the schematic given in Figure 1, confirmed that the responses met the required specifications using Eagleware's GENESYS Version 7.52 and provided a physical prototype.

The next task was to improve manufacturability and reduce cost. To reduce cost, the tuning time had to be minimized. I began experimenting with microstrip to eliminate the need for value-sensitive and hard-to-handle, wire-wound toroid, small air core or chip inductors. Using software simulation, we developed a microstrip equivalent to the lumped-element design but



▲ **Figure 2. The case/package.**



▲ **Figure 3. Finished trace layout.**

the low-pass section alone was seven inches long. We verified the design with a prototype on 0.032 inch thick circuit board, but it was too big.

Shrinking the design

In the next version, chip capacitors were substituted for the wide line microstrip "capacitors" and the narrow line microstrip "inductors" lines were meandered into a tighter space, with the goal of fitting in a 0.400 by 0.470 inch package space. Rather than prototyping a new printed wiring board (PWB) for every potential change in inductor geometry, I experimented with different lengths and gauges of wire, adjusting the lengths and coupling of the wires to attain an approximation of trace length, width and position on the finished circuit board. The case/package is shown in Figure 2. I switched to 0.062-inch FR4 board because it was sturdier when attaching 75-ohm connectors for measuring the response.

In an effort to crunch the low pass into an ever smaller space, I reduced the width and spacing of the meander line traces to the minimum that our prototyping equipment would accommodate, or about 0.008 inches on the line width and 0.012 inches on the line spacing. At this point, the PWB fit in the package and I began measuring responses with the circuit in an 8-pin surface-mount package mounted on a test jig consisting of 75-ohm traces and connectors on a 62 mil thick FR4 PWB.

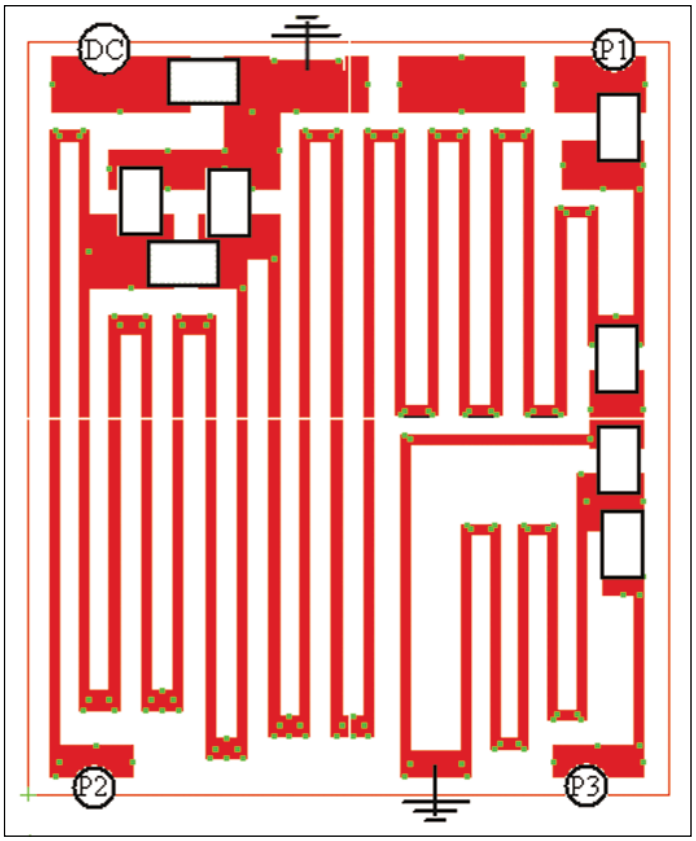
As an experiment, I removed the copper from the bottom side of the circuit and discovered little change in response and, thereafter, dispensed with it. After experimenting with numerous geometry changes and corresponding PWBs, I achieved a diplexer with adequate impedance matching on all three ports, with no copper on the bottom side of the board. The finished trace layout is shown in Figure 3.

The fact that removing the circuit ground-plane had little effect is surprising and further experimentation is required to investigate this. One might argue that the ground is being supplied by the ground of the impedance matched jig. Also, to a certain extent, coplanar grounds are provided by metal associated with the grounded capacitors and the grounded high pass meander inductors of the circuit.

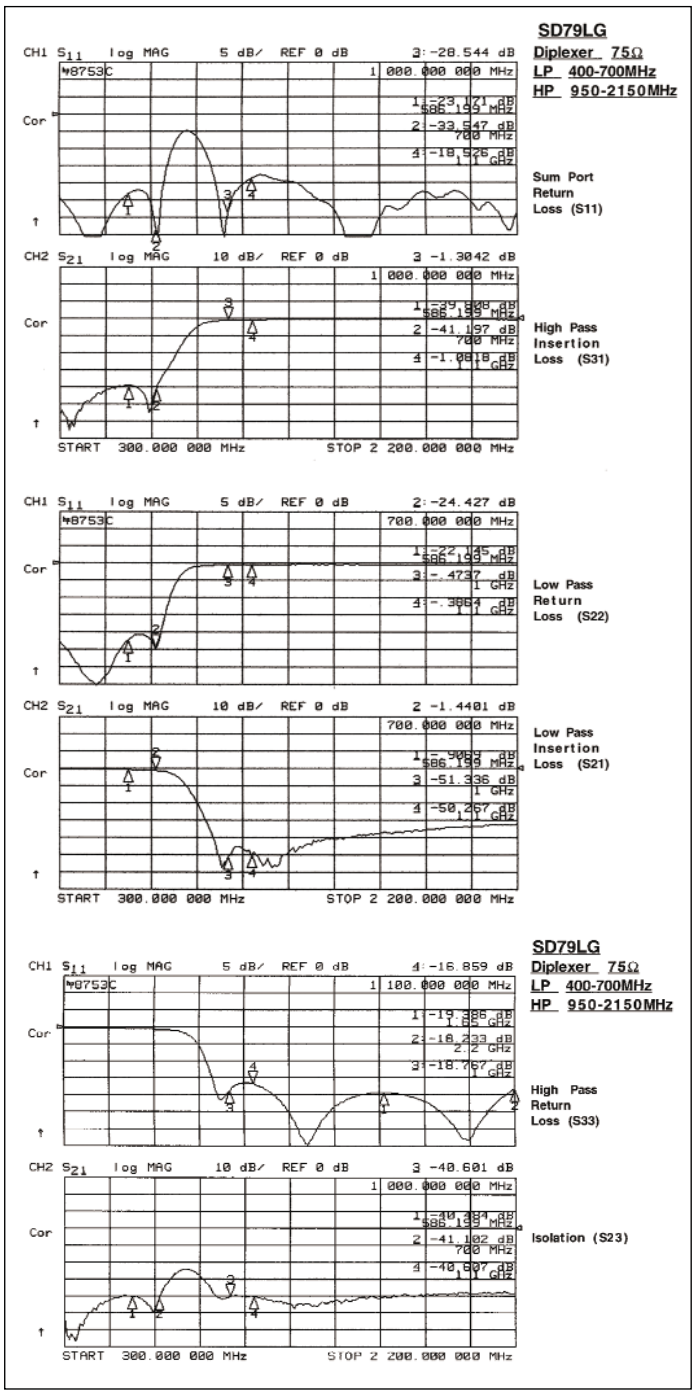
When I tried to crunch more inductance into a smaller space using thinner traces and smaller spacing between the meander line traces, I found a limit where there was not more inductance but less inductance and more capacitance between the end points of that meander line inductor. The middle inductor of the low pass has a capacitor in parallel to create a transmission zero in the stop band of the low pass. The frequency of this zero reveals the effect of changes in width and spacing on the inductance and capacitance values of the meander line. The self-capacitance of the meander line was adequate to replace a small value capacitor in parallel with a series inductor in a higher frequency filter application.

From prototype to production

Once a prototype that met specification was created



▲ **Figure 4. Finished trace layout with capacitors.**



▲ **Figure 5. Actual network analyzer plots of the SD79LG.**

in-house, we then had the problem of transferring the design to a layout for the board manufacturer. We laid out an array of 15 by 15 boards on a sheet of 0.062-inch, one-sided FR4 quarter ounce copper circuit board material, which was V-scored for separation. The final layout including lumped capacitors is shown in Figure 4. Typical tolerance on the dimensional accuracy of commercial FR4 PWB manufacture is ± 0.5 mils. One option for copper surface treatment is high temperature solder reflow, but this adds to the thickness of the traces and, thus, reduces the inductance of the lines. A second option is electroplating the traces. This does not reduce inductance and prepares for component pick and place using reflow with eutectic high-temperature solder. To achieve the required diplexer specifications for both processes, we found it necessary to use different capacitor sets for each process. Network analyzer plots are shown in Figure 5.

We found that high-quality engravers (www.Anders-Engraving.com) and PWB manufacturers can maintain prototype and high-volume dimensional tolerances of 0.5 mils. We use capacitors as small as 0402 using no solder mask, since there is almost zero incidence of capacitor tomb-stoning. Larger capacitors provide a higher unloaded *Q* but they require valuable board space. We have had good results with Johanson chip capacitors with a tolerance of plus or minus 0.1 pf. The reality, however, is that an even tighter tolerance of plus or minus 0.05 pf is required to ensure repeatability of response. Fortunately, a reel of 10,000 chip capacitors from Johanson will not only meet the specified tolerance but usually the entire reel will have a much higher tolerance on part to part variation.

The populated circuit board in Figure 4 has an additional direct current (DC)-block capacitor and a bias-T capacitor. Missing from this diagram is a wire-wound toroid inductor for the bias-T. The addition of a bias-T

causes a slight degradation in the passband. Isolation between high pass and low pass is typically –35 dB. The final capacitor values were determined empirically and vary somewhat from the values in the initial lumped-element design. The final values for this design are C1 = 1.5, C3 = 1.8, C5 = 2.0 for the high pass, and C2 = 2.7, C4 = 1.5, C6 = 2.0 for the low pass. The DC block and bias-T capacitors are 220 pf.

Conclusion

A design process that began with a lumped-element model was transferred to an equivalent distributed design using software. It was then completed using empirical methods to develop a cost-effective diplexer solution with good performance. This distributed meander line/lumped capacitor hybrid achieves a very compact design and is suitable for high volume manufacture for wireless systems, in this case up to 2200 MHz. ■

Acknowledgement

The author would like to acknowledge the assistance of Michael Magnin, senior engineer at MicroSignals, Inc., in Palisades Park, NJ. He graduated from Grenoble University Electronic Institute and has been working in the radio frequency (RF) and microwave component and systems design since 1984.

References

1. R. E. Collins, *Foundations for Microwave Engineering*, New York: McGraw-Hill, 1992.

Author information

Peter Nordquist attended Rensselaer Polytechnic Institute in Troy, NY, for a year, then became a missionary for 10 years. He then trained as a computer numerical control (CNC) machinist, Pascal CAM software programmer and RF component engineer. He is a filter engineer at MicroSignals, Inc. He may be reached via E-mail: NordaVinci@aol.com; Tel: 201-363-0951; or Fax: 201-363-0955.